Challenges in Modeling and Verification of 2.5D/3D and FOWLP

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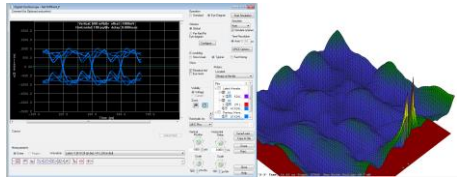
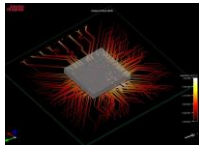
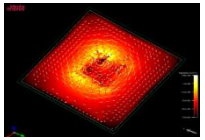
EDA Challenges in Modeling and Verification

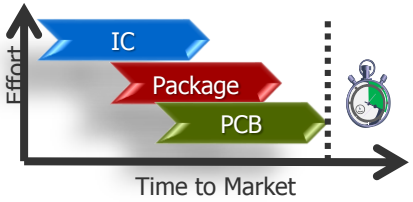
- **Modeling**
  - Different phenomena: electrical, thermal, mechanicals;
  - Interaction modeling
  - Tradeoff between needed accuracy and model complexity and flow integration
  - Consistency between different levels of abstraction

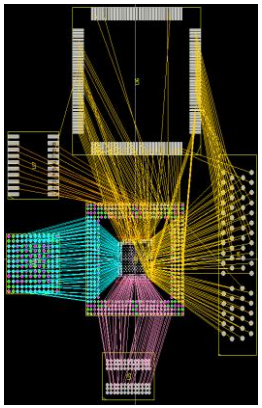






- **Verification**
  - Cross-domain integration
    - ICs, Interposer, Package , Board

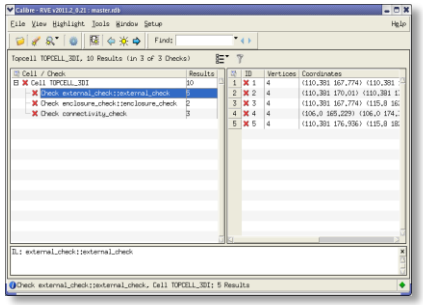


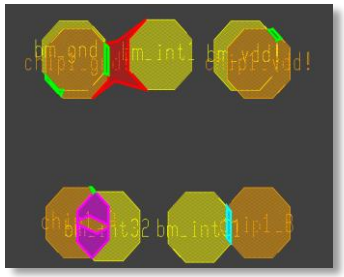


  - Resolving issues related to multiple disconnected tools with no standard methodology/flow to synchronize and transfer design data between design disciplines and abstraction levels
  - Standards needed for tool interfaces and data exchange format

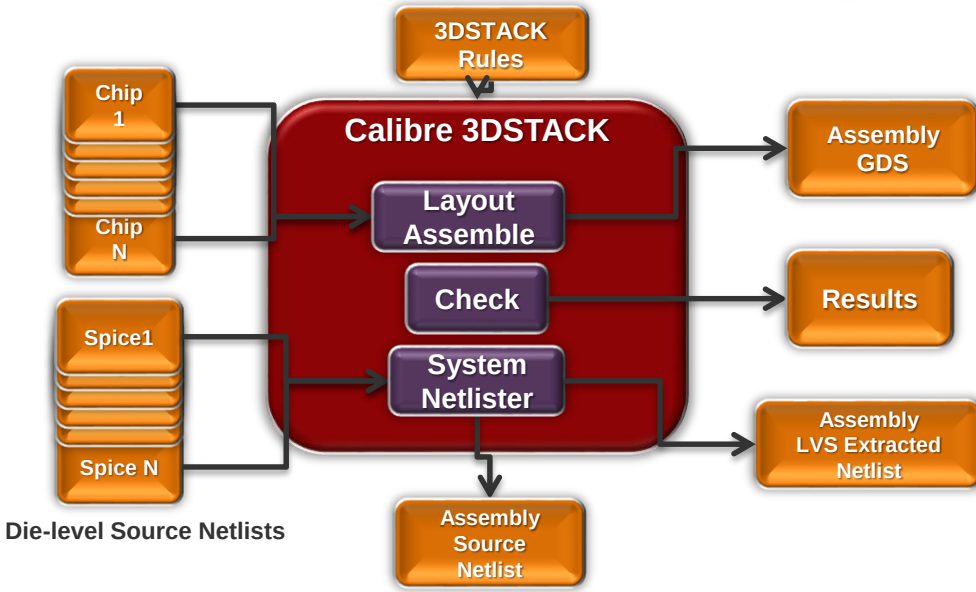
Stack Verification and Extraction

- 3D Stack Verification Flow

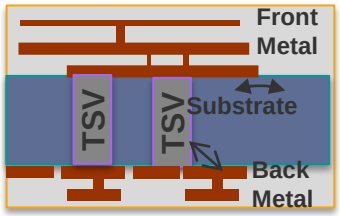


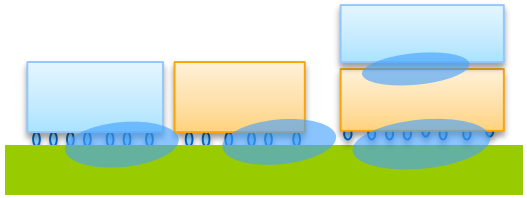


- Verify with micro-bumps are physically aligned
- Verify proper electrical connectivity through die2die and die2interposer interfaces



- Extract parasitics of the Dies and Interposer interconnects
- Insert provided TSV circuit into integrated parasitics/TSV netlists, or extract TSV
- Intra Die Component Interactions and Extraction
  - TSV to TSV
  - TSV to RDL
- Inter Die/Interposer Component Interactions
  - Analysis of die-to-die , die-to-interposer die-to-package coupling





Impact of Inter-die Extraction Methodology

F2F bonded dies

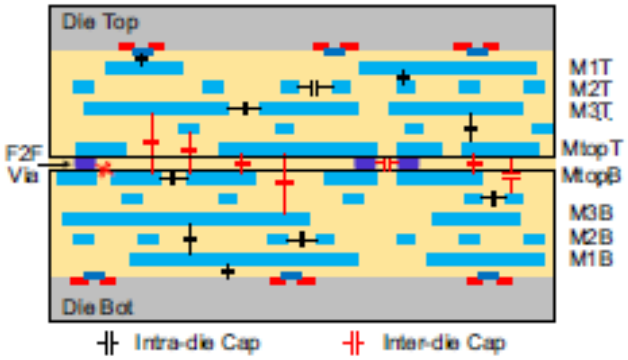
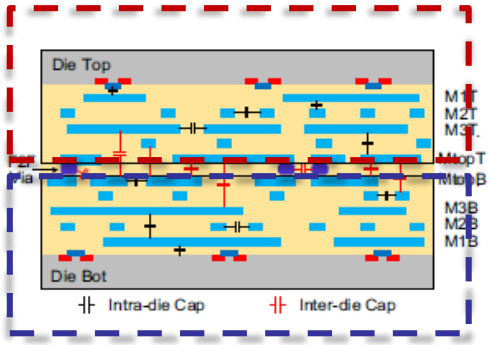


Fig. 1. Cross-sectional view of a F2F-bonded 3D IC structure with interconnect parasitics.

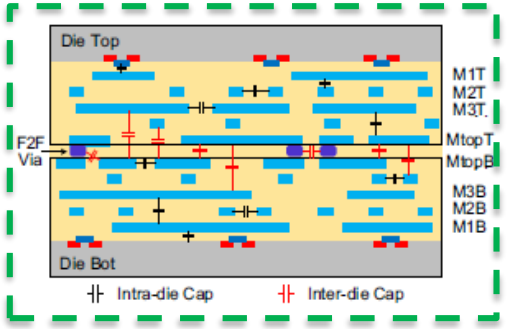
TABLE IX
FULL-CHIP COMPARISON OF DIE-BY-DIE (D-D), HOLISTIC (HOLI), AND IN-CONTEXT (IN-C) EXTRACTION WITH ONE INTERFACE LAYER PER DIE.

metric	Holi	D-D	Err%	In-C	Err%
Longest path delay (ns)	3.90	3.66	-6.2%	3.83	-1.8%
3D nets switching power (mW)	1.05	1.01	-3.5%	1.04	-0.4%
Total switching power (mW)	12.1	11.9	-1.7%	12.0	-0.8%
Total coupling cap on 3D nets (fF)	4.37	2.96	-32%	4.21	-3.7%
Total wire cap on 3D nets (fF)	10.8	9.35	-13%	10.7	-1.1%
Average aggressor # on 3D nets	285	200	-30%	253	-11%
Max noise on 3D nets (mV)	41.3	30.40	-26%	38.8	-6.1%

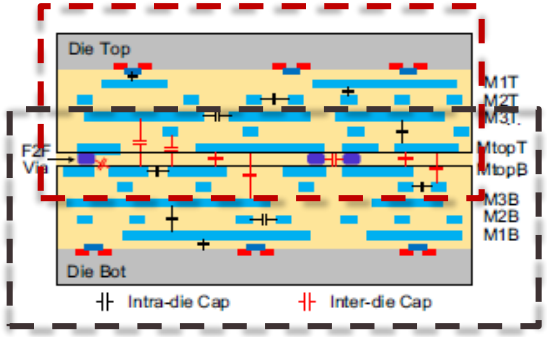
"die by die"



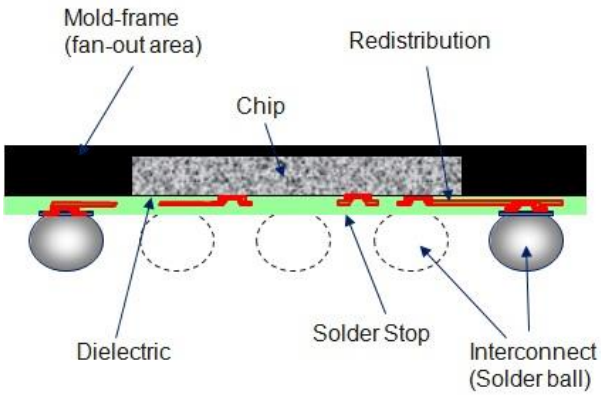
"holistic"

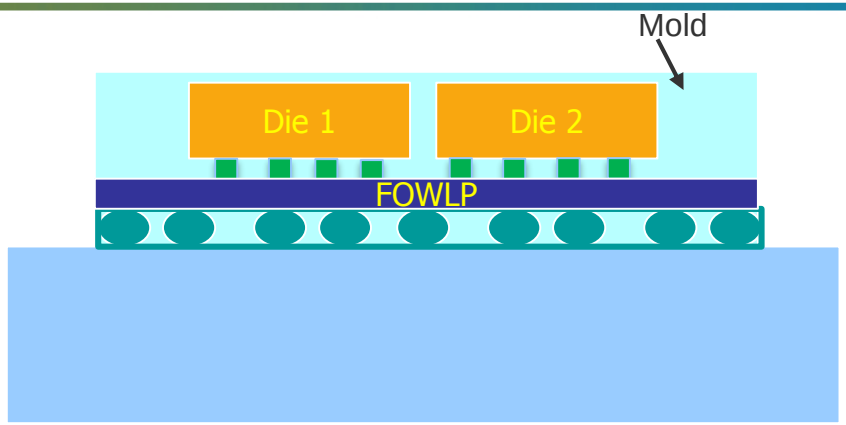


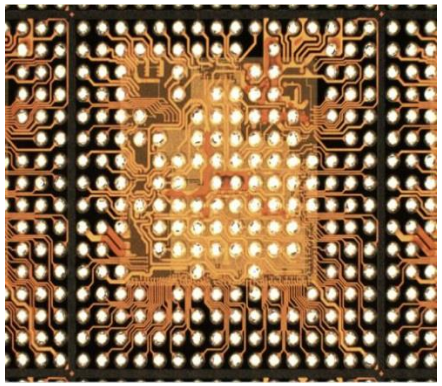
"in-context"



Typical FOWLP Structure and Layout





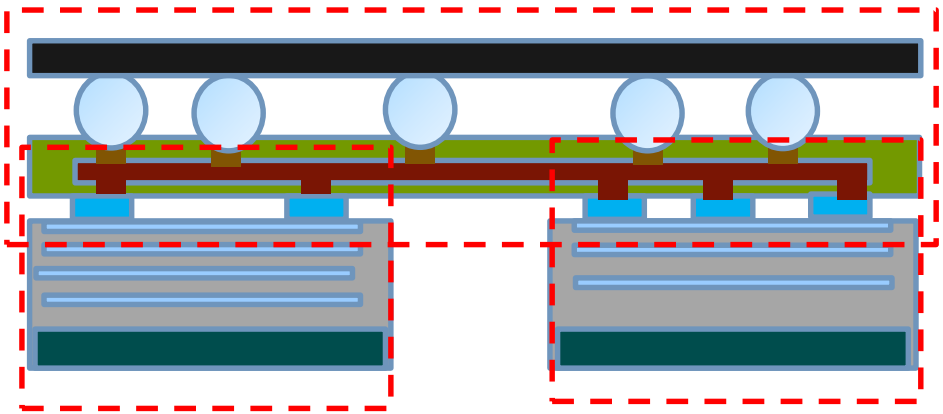


- Better Electrical Performance
  - No bumps, wire-bonds and substrate
  - Shorter interconnects
  - Fine Line Width/Space; Finer pad pitch on die
- Thin package, Smaller Form Factor
- High integration
- Potential SiP, Multi-die, 3D Solution
- Heterogeneous chips + passives

FOWLP Parasitic Extraction

- Is there significant interaction between the die and package ?
- Is there any inductive interaction/impact?
- What tool should be used for extraction of the interface and die package interaction?
  - Board/package tools have complexity/run-time issue
  - IC tools might not be accurate enough

- One of F2F methodologies can be applied



"In Context" Extraction Methodology

- Extract the dies "in context"
- Extract the package "in context" with the ground assumed at the board level
- Netlisting
  - Do not netlist couplings; Fold them into top level capacitances; Stitch the netlists
  - Netlist the couplings

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