SYNOPSYS®
Silicon to Software™

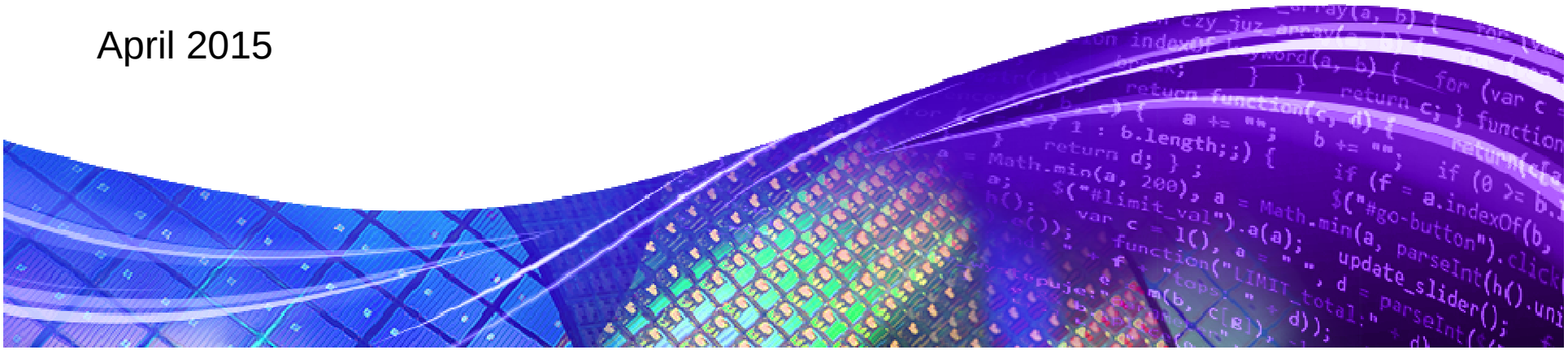
Power Aware Architecture Design for Multicore SoCs

EDPS Monterey

Patrick Sheridan

Synopsys Virtual Prototyping

April 2015

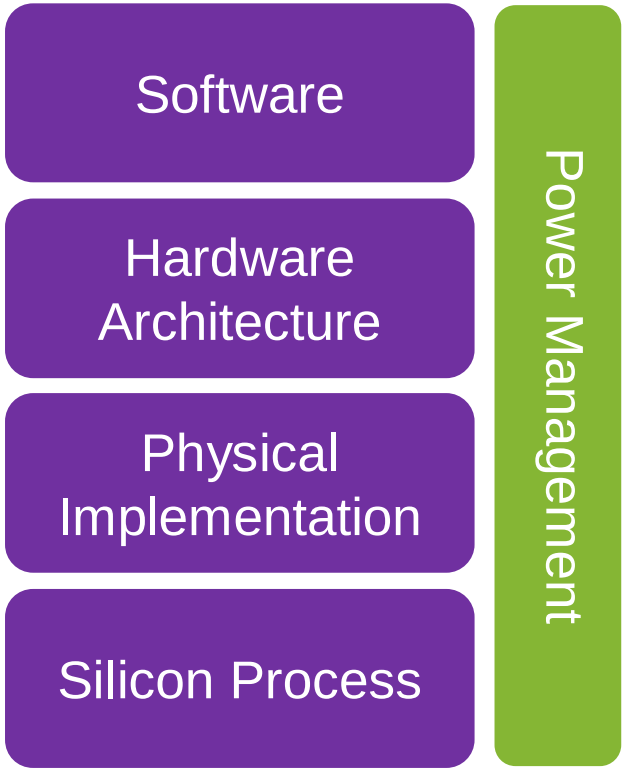


Low Power SoC Design

- Multi-disciplinary system problem
- Must manage energy consumption from software through to silicon

Power Aware Architecture Design for Multicore SoCs

- User Persona: Architect
- Uses virtual prototyping to enable intelligent trade-offs between power and performance early in the design cycle

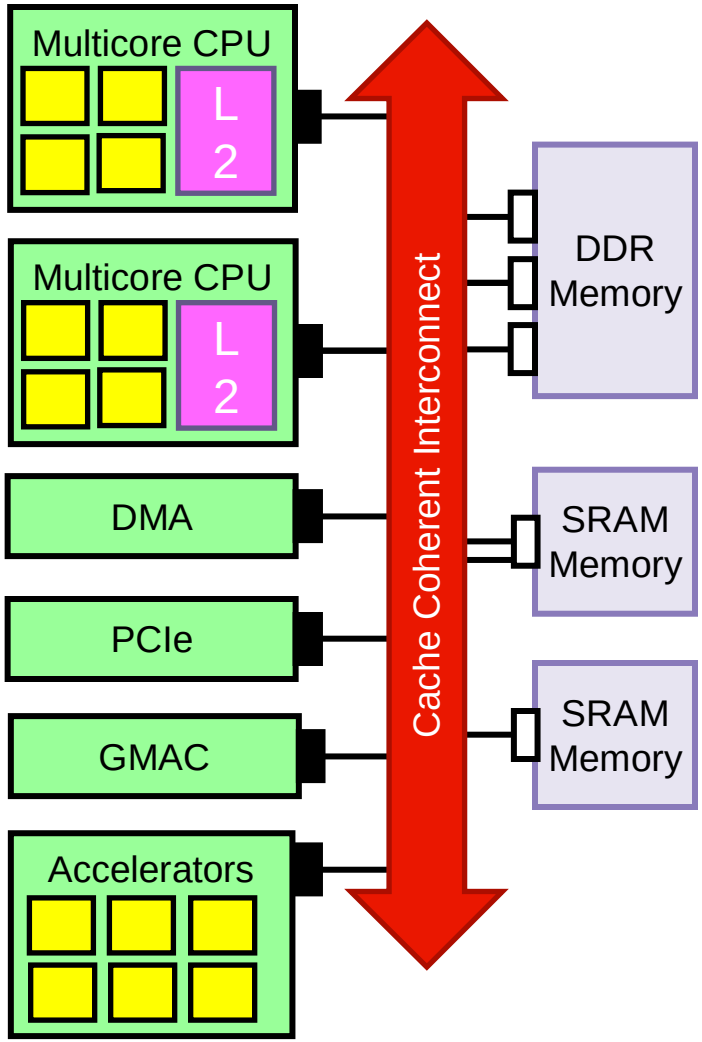


SoC Power Analysis

How does architecture affect energy consumption?

***Architecture Decisions** (examples)*

- **HW/SW partitioning**
- **Best cache size and organization?**
- **How to achieve low latency without starvation?**
- **How to avoid page misses?**

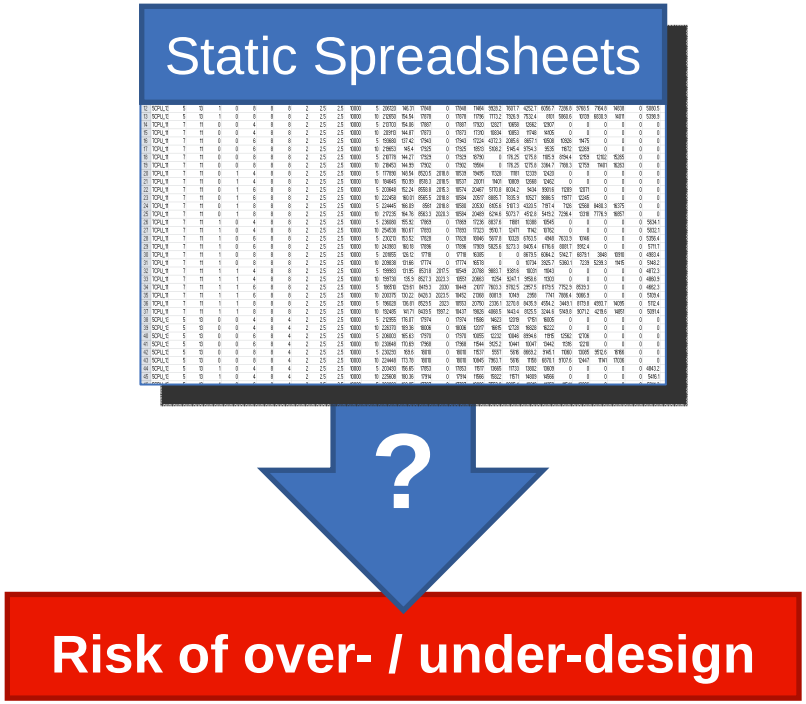


***Power Management Decisions** (examples)*

- **Power domain per core or entire CPU?**
- **Run fast and stop or DVFS?**
- **Turn off when idle?**
- **Timeout for moving to low power states?**

Problems with Spreadsheets

Static calculations don't reflect multicore behavior

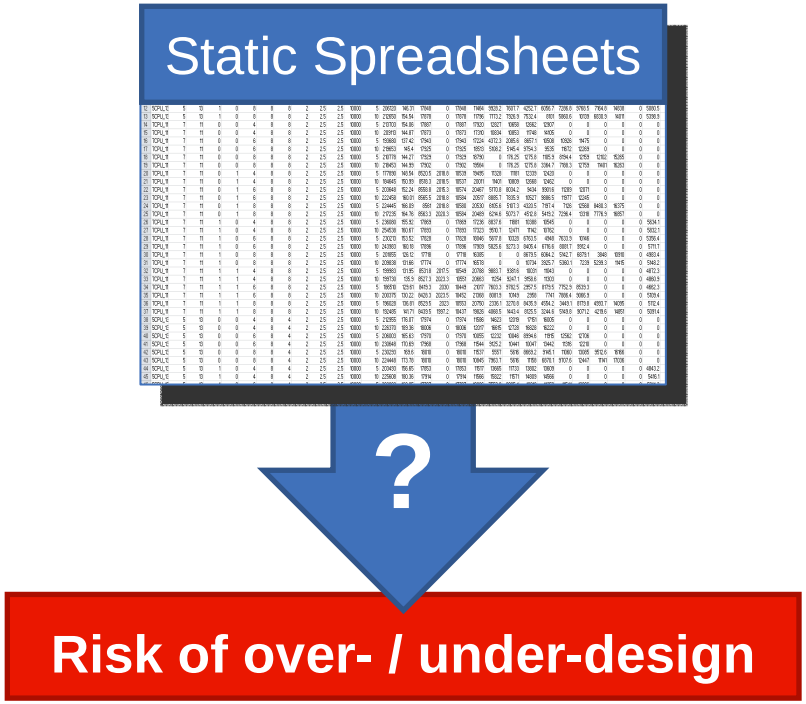


- Very large and complex
- Only average values for a complete use-case sequence
- Manual identification of worst-case scenarios
- Limited set of scenarios

- **No dynamic interaction** of system activity, architecture performance, and power management

Problems with Spreadsheets

Static calculations don't reflect multicore behavior



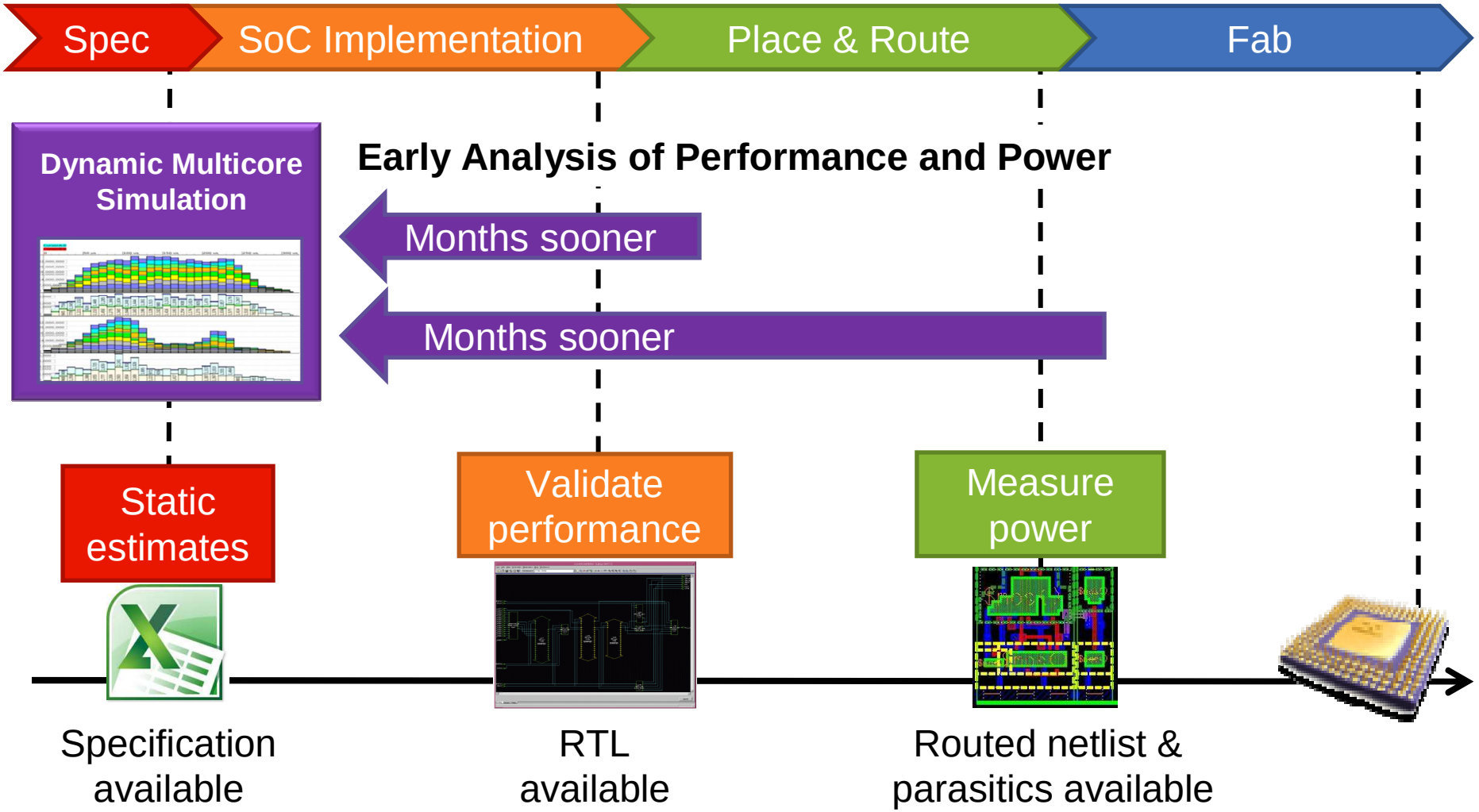
Under-design → Performance issues

- Fix by increasing the clock rate?
- Schedule impact? (timing closure, verification issues)
- Energy consumption? (power issues)

Over-design → Power, Cost issues

- Fix with more expensive package?
- Re-spin? Cancel project?

Power Aware Architecture Design for Multicore SoCs



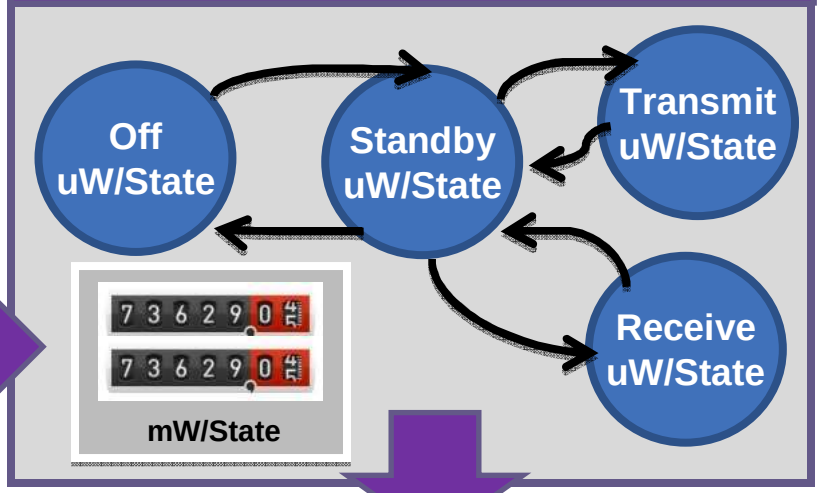
Virtual Prototype and Power Model

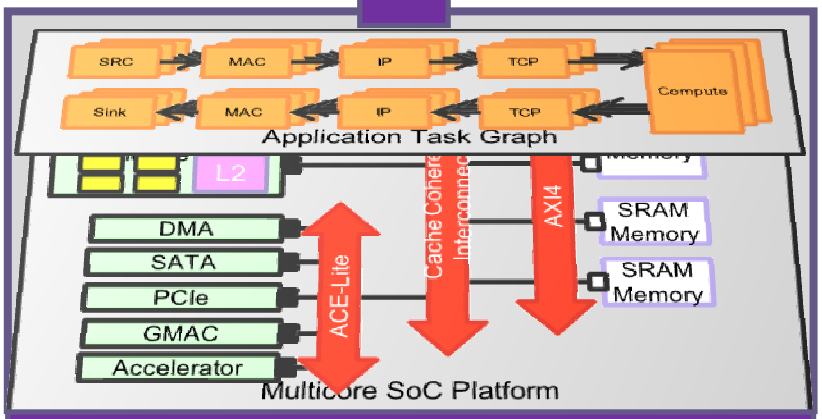
Visible Events in Virtual Prototype

Voltage/frequency
Signal access
Register/memory access
TLM port access
Events/counters/statistics
Static and dynamic parameters
Self-timed state transition
Function calls

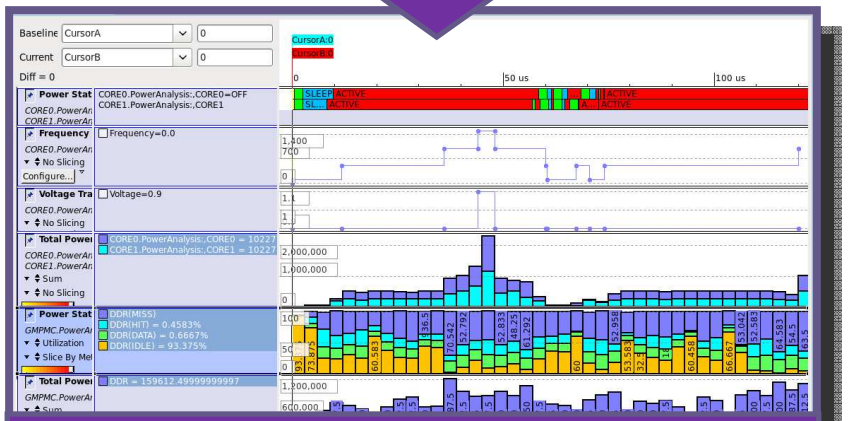
trigger

Power State Machine (overlay)



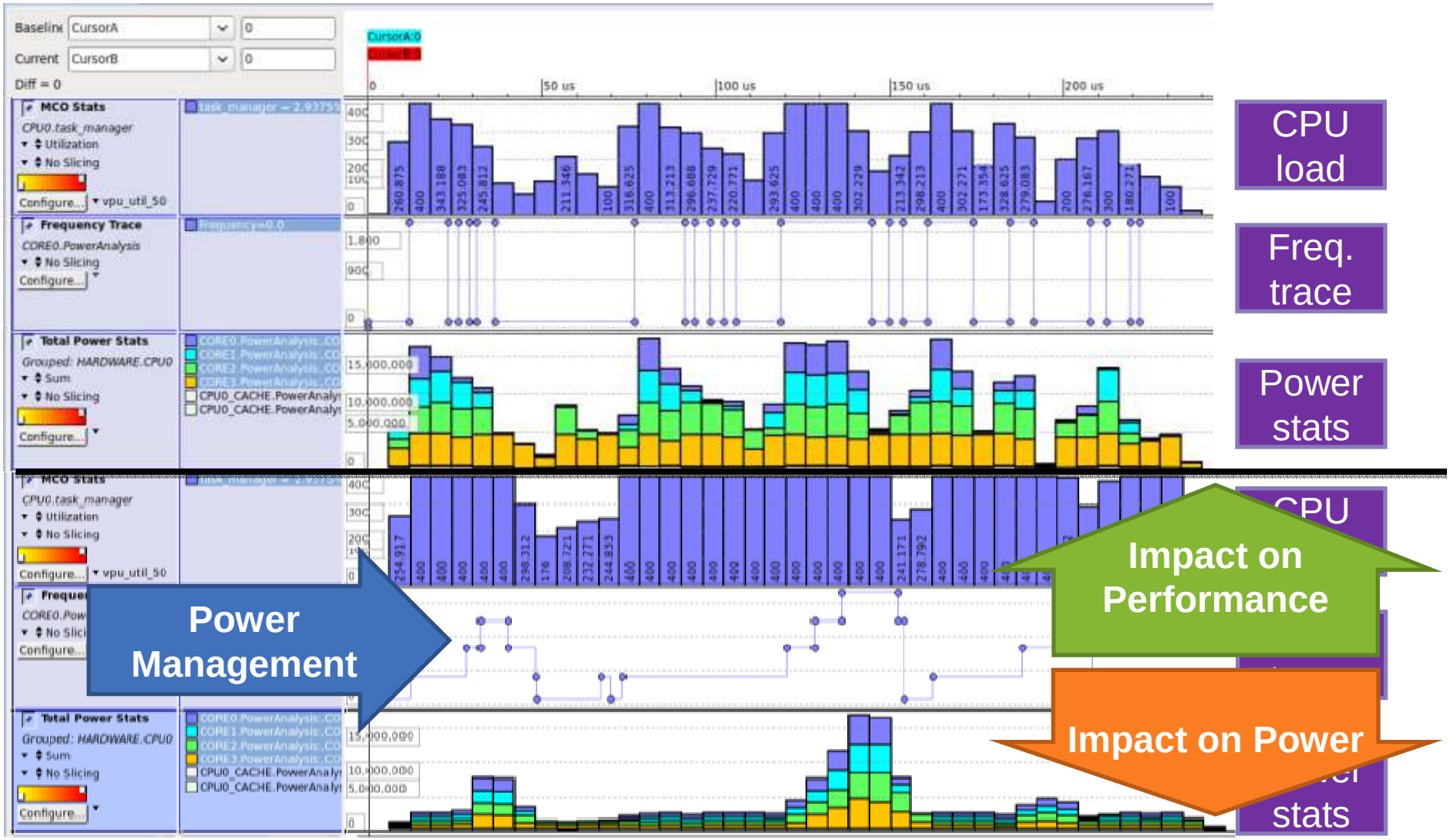


Virtual Prototype Performance Model



Performance and Power Analysis

What-If Power Analysis

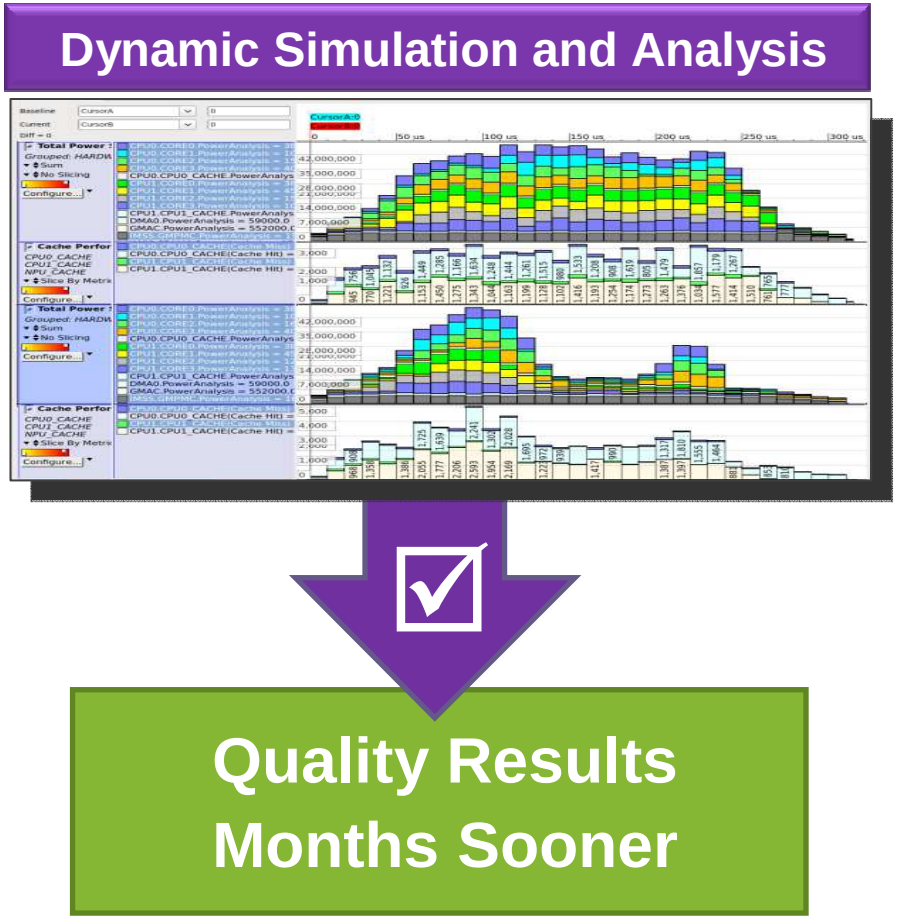


IEEE Standardization

Goal: Interoperable IP Power Models

- Extend 1801 UPF for system level design
  - Dedicated System Level Power Modeling sub-group
  - System and power architecture, EDA and IP representation
- Targeting IEEE 1801 “UPF 3.0” release in 2015
- Visit
  - http://standards.ieee.org/develop/wg/UPF.html
  - http://www.p1801.org/
  - http://semiengineering.com/system-level-power-modeling-activities-get-rolling/

Power Aware Architecture Design for Multicore SoCs



- Uses virtual prototyping to enable intelligent trade-offs between power and performance early in the design cycle
- Non-intrusive overlay approach, leveraging existing IP power information
- Unified view of activity, performance, and power
- Aligned with emerging IEEE standards

SYNOPSYS®
Silicon to Software™

Thank You