Power: What's the problem?

Industry trends and solutions in low power design

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Systems Verification Group

April 2015

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Agenda

- Industry Trends
- Power: what's the problem
- The problem: it's not just power
- Power challenges: is not the performance, it's the thermal
- Use case and scale challenge
- Cadence technologies
- Summary

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Industry trends

Drivers of design change

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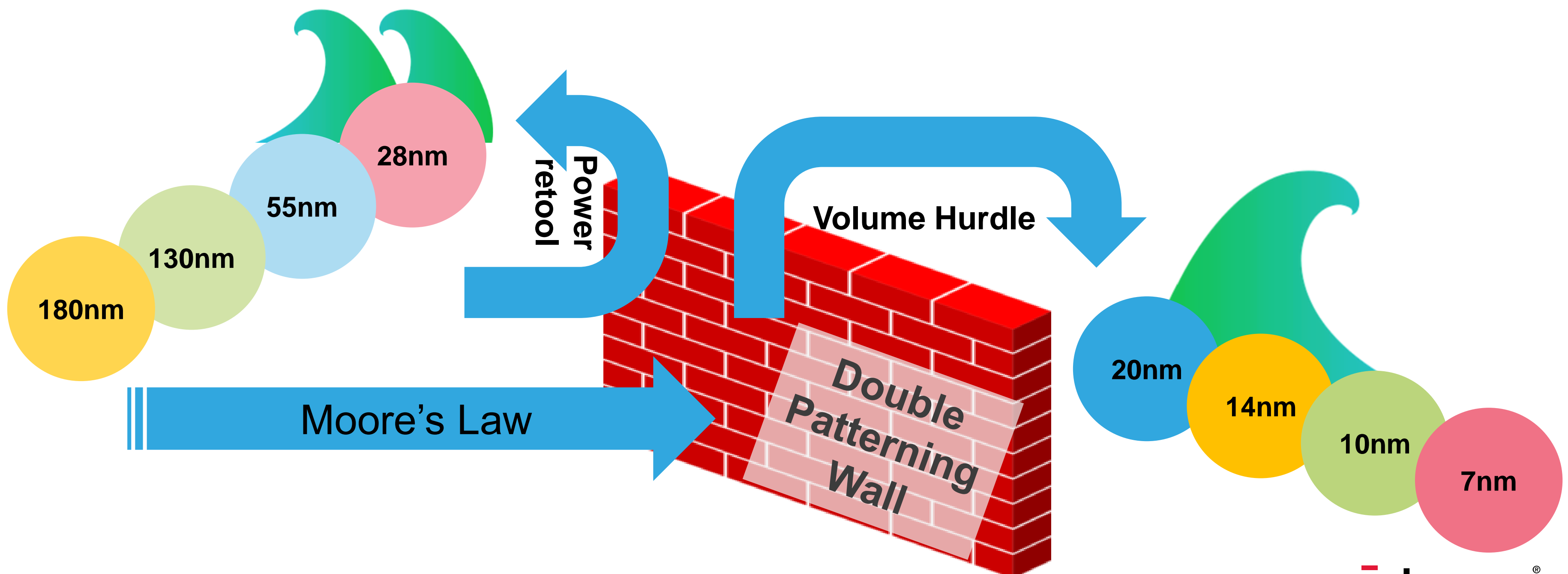
Moore's Wall

Macro trend bifurcates miniaturization roadmaps

- Mature nodes evolved
  - Lower and lower Vdd
  - Re-design memories, analog IP, etc.
  - Add LP cells for PSO, MSV, etc.
  - Thermal/performance issues at near threshold Vdd values
  - MEMs sensors, energy harvesting, RF
- Advanced node
  - Very high volume drivers jump the hurdle
  - Multi-patterning
  - New materials/devices
  - Power and thermal issues hamper architectural performance gains



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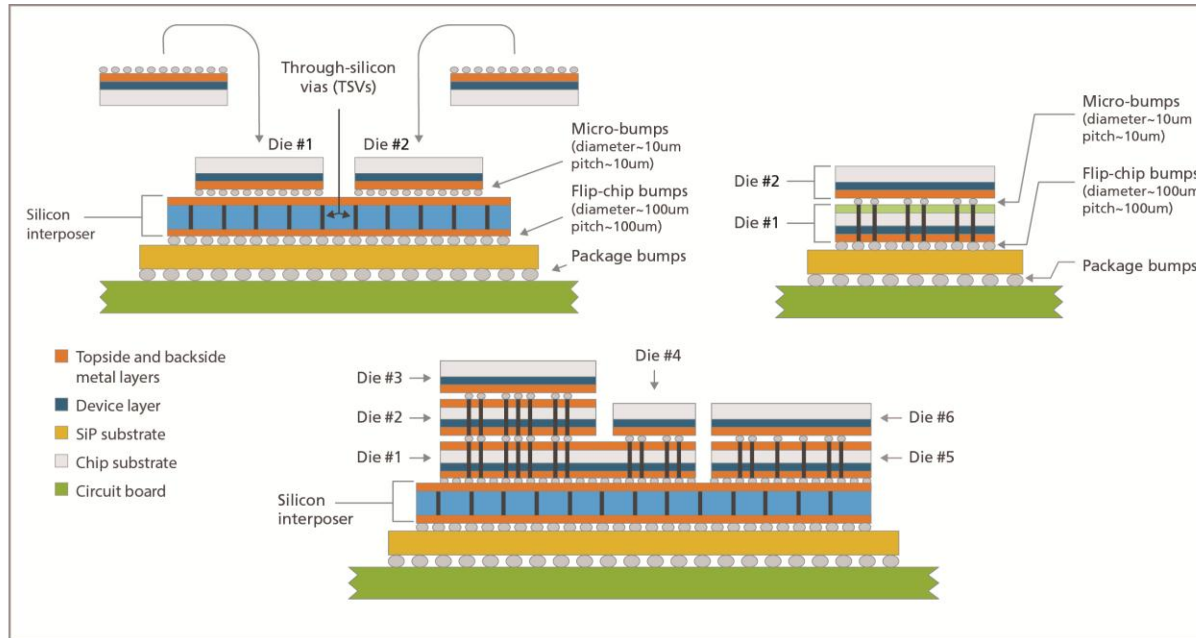
Packaging innovation
Miniaturization innovation beyond Moore



- Foundries drive Si interposer and stacking technologies
- OSATs investing in fine geometry organic substrates
- PCB embedded die

Product designers: litany of new choices; customization flourishes

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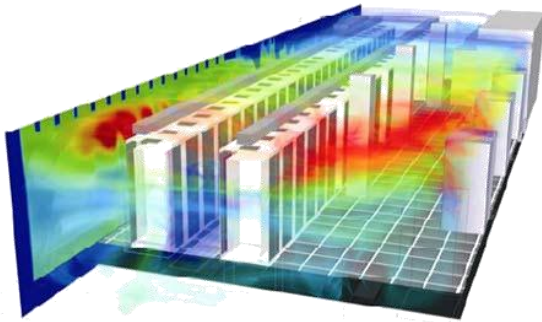
Cooling: remote to local, materials

Virtuous circle of reduction

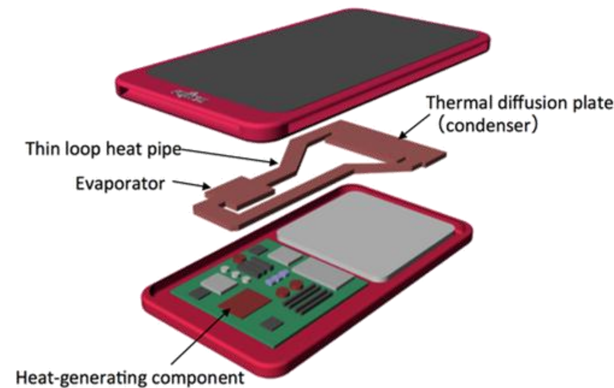
Remote: cool rooms

Local: cool chips

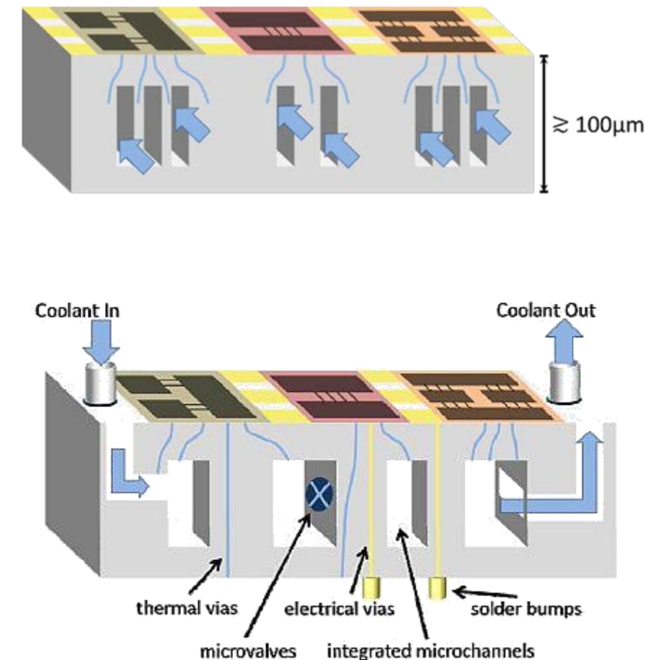
Data center



Product



PCB/MCM/3DIC



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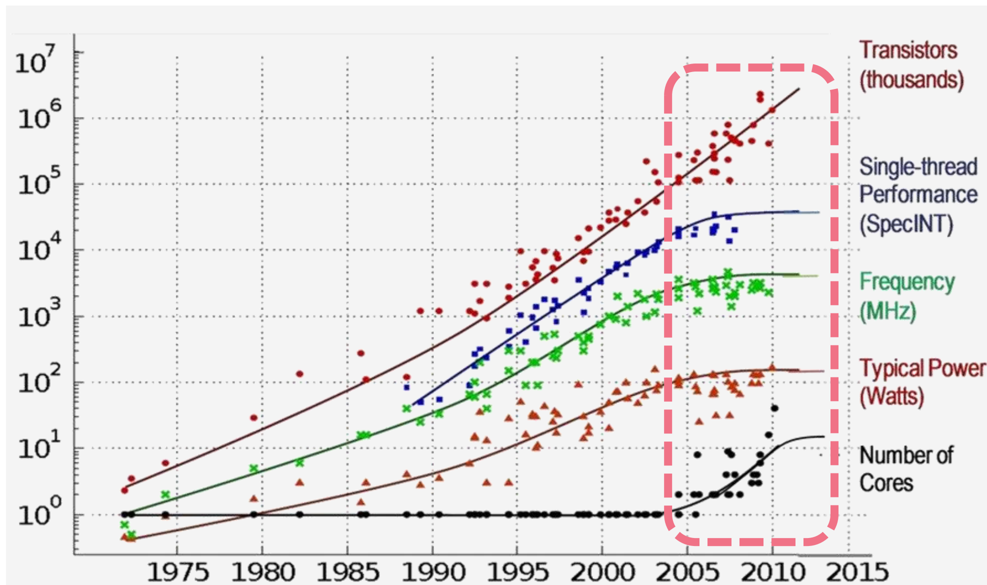
10 year trend summary

Physics, architecture, manufacturing changed shape



- Frequency wall based on power limit
  - Single thread performance stall
- Performance gains through multi-core
  - Heterogeneous cores to optimize performance-energy
- Thermal wall based on parallel execution limits
  - “Dark silicon” becomes pervasive

- Complex orchestration of execution units to maximize performance and stay within thermal limits
- Simultaneous need to task energy efficiency
  - Battery life in mobile
  - Power/cooling cost in data center

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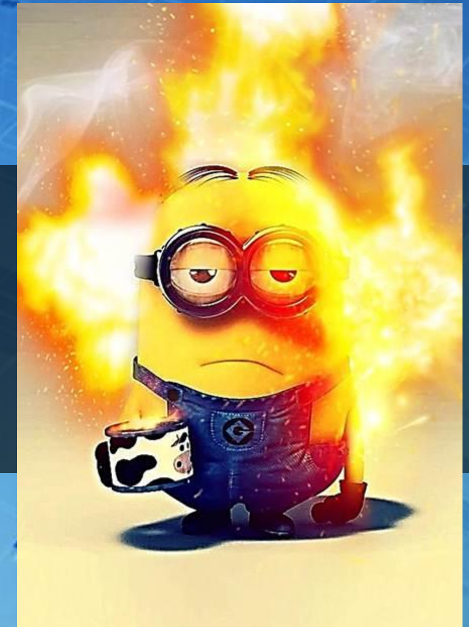
Power: what’s the problem?
Hot topic



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Power verification: why the surprises

- It's simple:
  - UPF/CPF provide specification
    - Switches, isolation, retention, modes, …
- It's complicated:
  - Which voltage level? 3 or more
  - Which frequency? 3 or more
  - Which corner? 12 to 100
  - Which voltage domain? 100 or more
  - Which use case? Billions of clock cycles

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Complementary LP Verification Solutions

LPV App, Incisive LP Simulation & Conformal Low Power

Verification

Formal

- Comprehensive LP assertion support
- LP functional checks
- Power-aware SEC
- Provides LP-awareness for other apps (XPROP, FPV, CONN, CSR…)

- Basic LP assertions
- Power-aware debug
- LP XPROP analysis

- Elaborate power-aware design from RTL + UPF/CPF
- Models isolators, state retention
- Basic power-aware "lint"
- Static analysis of power format

Simulation/Emulation

- Static code analysis (lint) in PSO
  - Disable corruption of certain datatypes
  - Replay initial blocks at power-up
- Power aware sim
  - Find design and power sequence errors including incorrect isolation values, initialization problems, incomplete state retention, etc

LEC/LP

- Logical/physical netlist structural checks
- Level-shifter, power switch checks
- Cell mapping & library checks
- Power-aware LEC
- PG connection & layout checks
- Supports custom & MS macros

- Power-aware gate-level verification
- Liberty support

Synthesis/ Implementation

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The problem: it's not just power

Interrelated design criteria

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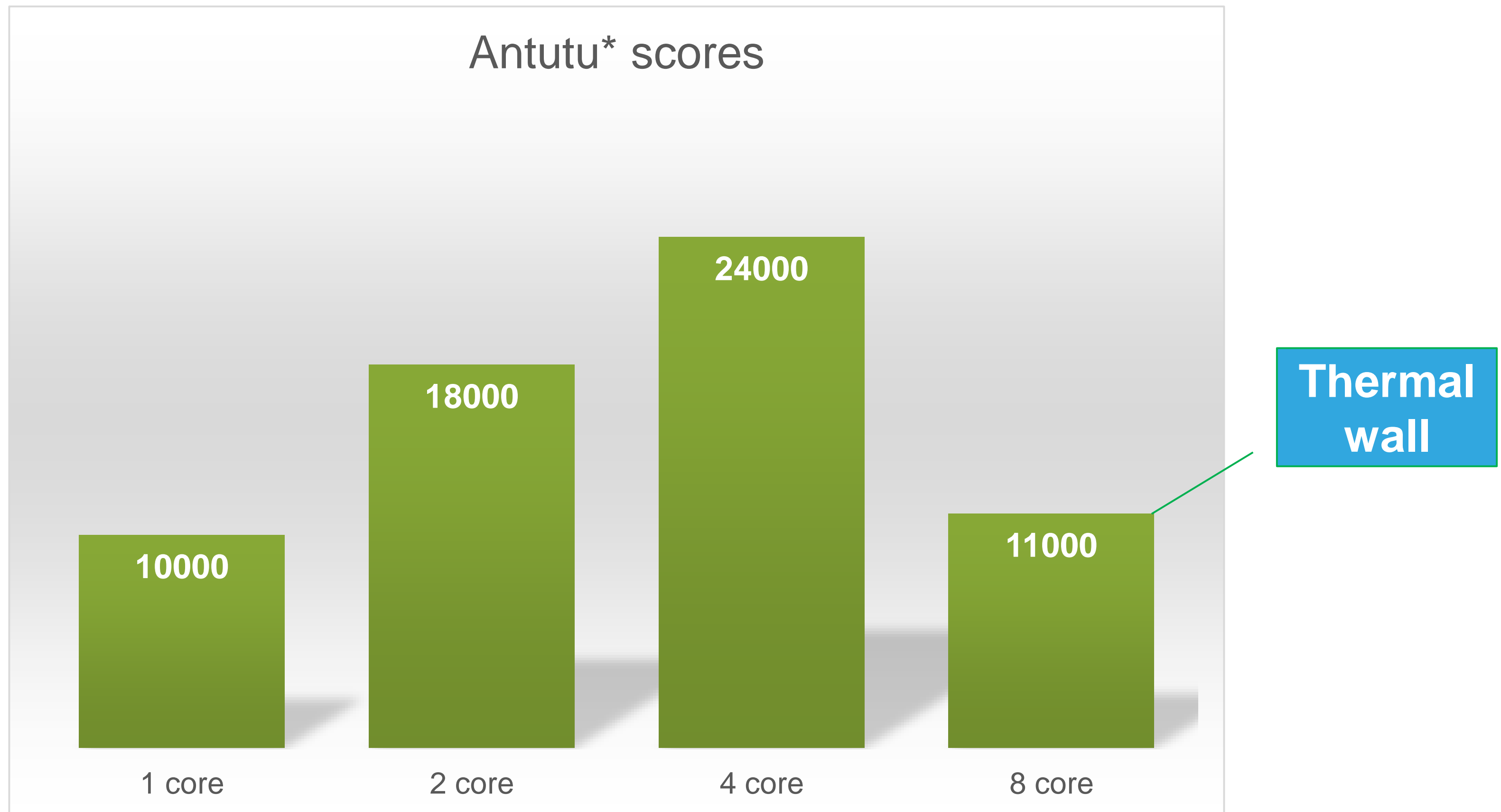
Example: mobile processor SoC

Thermal issues diminish architectural performance potential



***Antutu Android benchmark (www.antutu.com)**

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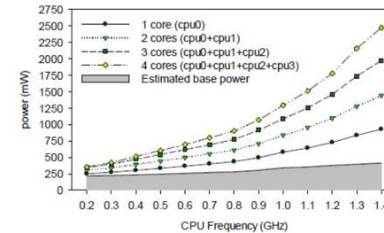
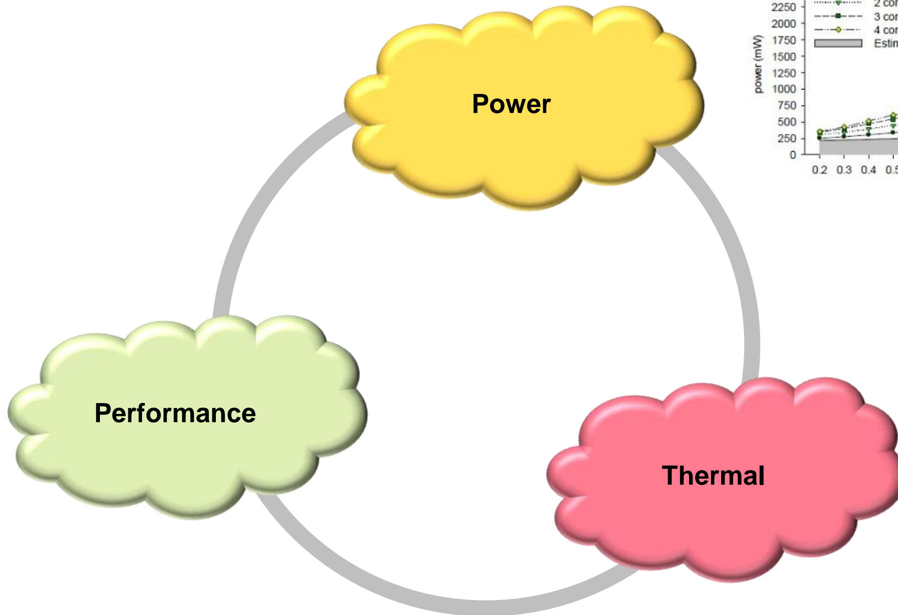
Performance-Thermal-Power

Domain connections

Must balance performance & power to control heat





Performance is critical purchase criteria

Cranking up clock heats up device

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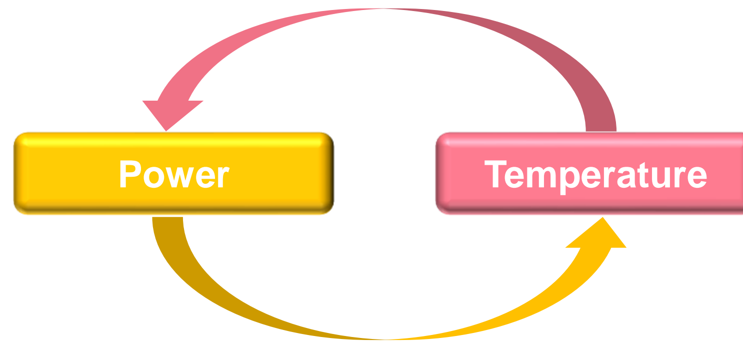
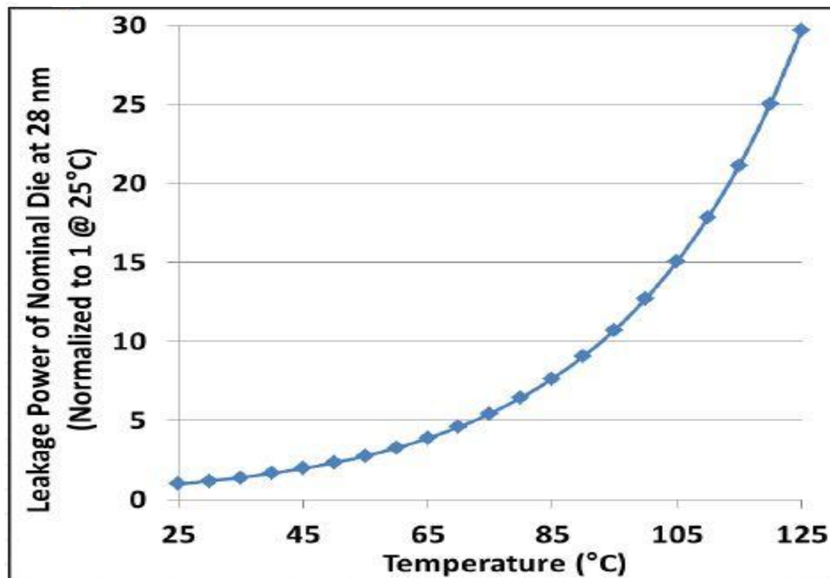
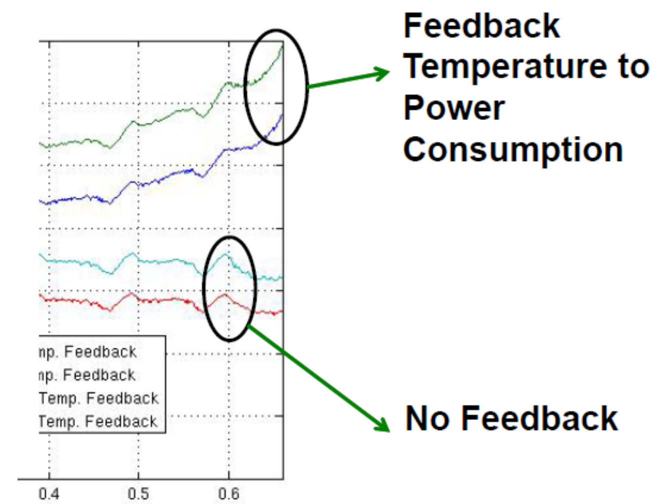
Power ⇔ Temperature

Mutual dependence ⇔ nonlinear behavior







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Power challenges

It’s not the performance, it’s the thermal

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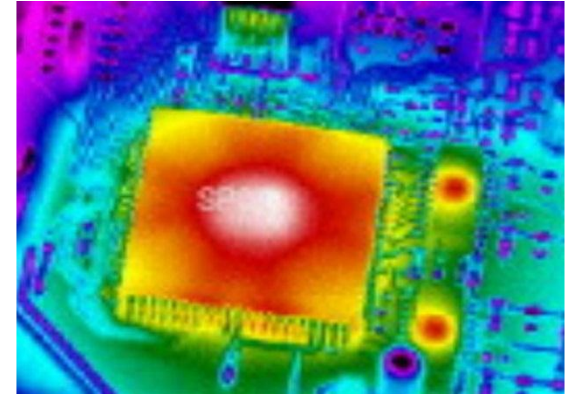
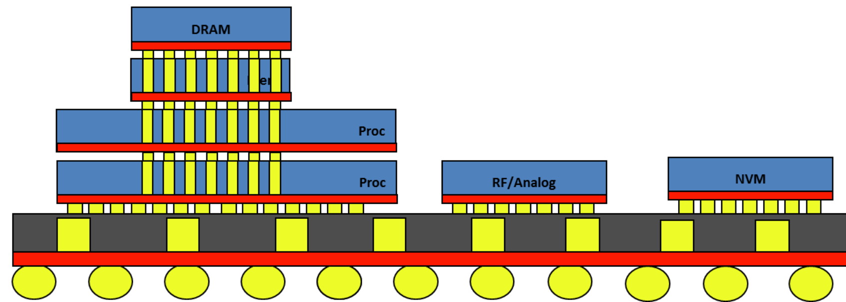
Thermal issues in modern SoCs



- Growing thermal issues
  - Technology scaling => higher power density
  - 3D stacking with TSV => greater thermal issues



- Temperature impacts
  - Power consumption
  - Peak performance
  - Ageing/reliability
  - Package costs
- MP SoC architectures
  - Dynamic applications, variable execution time
  - Power management solutions (DVFS), can even worsen thermal properties!

➔ ***Thermal mitigation schemes must be proposed at design time***

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Thermal mitigation landscape

From system to sign-off

Applications/OS/system

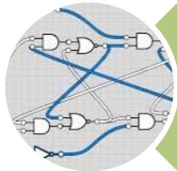
- Which applications are critical to product success? Desired user experience: speed, battery life, form factor, cost?

- Thermal-aware OS features
- Register re-mapping
- Thread migration
- Weighted task scheduling

Architecture

- What computation elements needed to achieve performance/efficiency/cost?

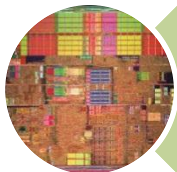
- Processor choice(s), IP selection
- Hard-wired versus programmable
- Voltage/power domains
- Package/enclosure selection



Design

- How to link modules, create micro-architecture, drive mapping to process?

- Micro-architecture optimization
- Power management
- Power optimization
- Clock gating



Implementation

- Which node, what library, what flow, which tools, … ?

- Lower local layout density
- Spread hot units far apart
- Interconnect pitch control
- Power optimization

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Use case & scale challenge

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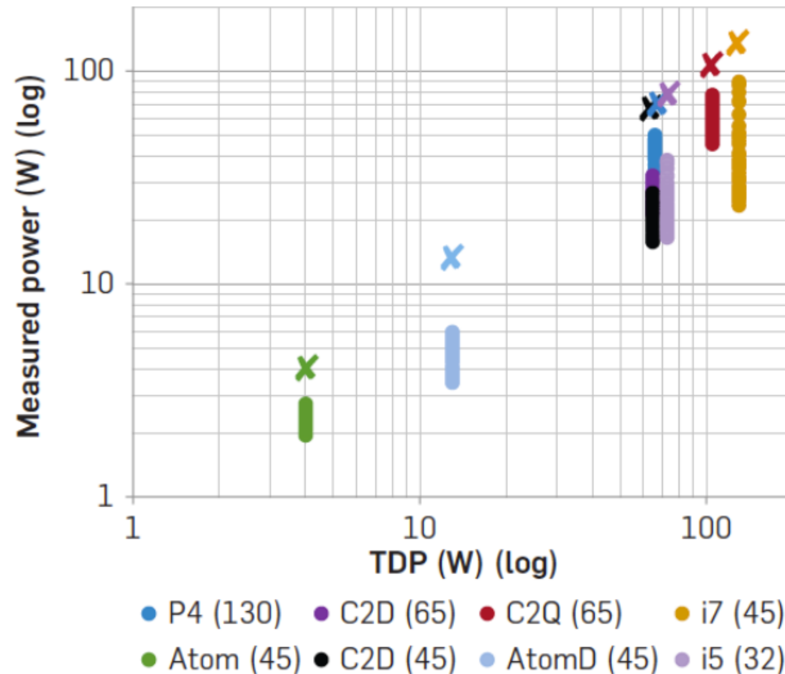
Use case challenge: huge dependency
Performance benchmarks vary 8-10X

Measured power for each processor running 61 benchmarks. Each point represents measured power for one benchmark. The "*X*"s are the reported TDP for each processor.

Finding: power is application dependent



Cao et al, CACM 2012

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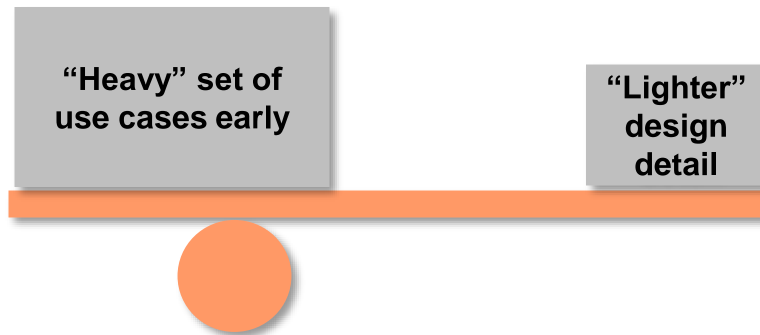
Early power visibility

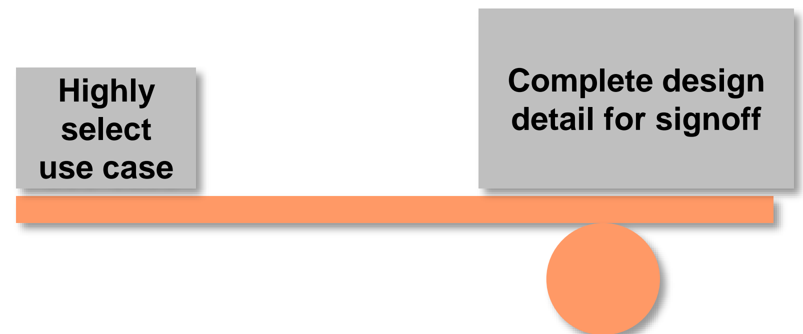
Abstraction hinders and helps

- Abstraction of design <u>hinders</u> accuracy
- Abstraction of design <u>helps</u> processing more use cases



- Need for massive use case analysis
  - Power behavior debug
  - Determination of final use cases for detailed power and thermal analysis

- Need complete design detail
  - Power/IR drop analysis
  - Signoff across growing MMMC space



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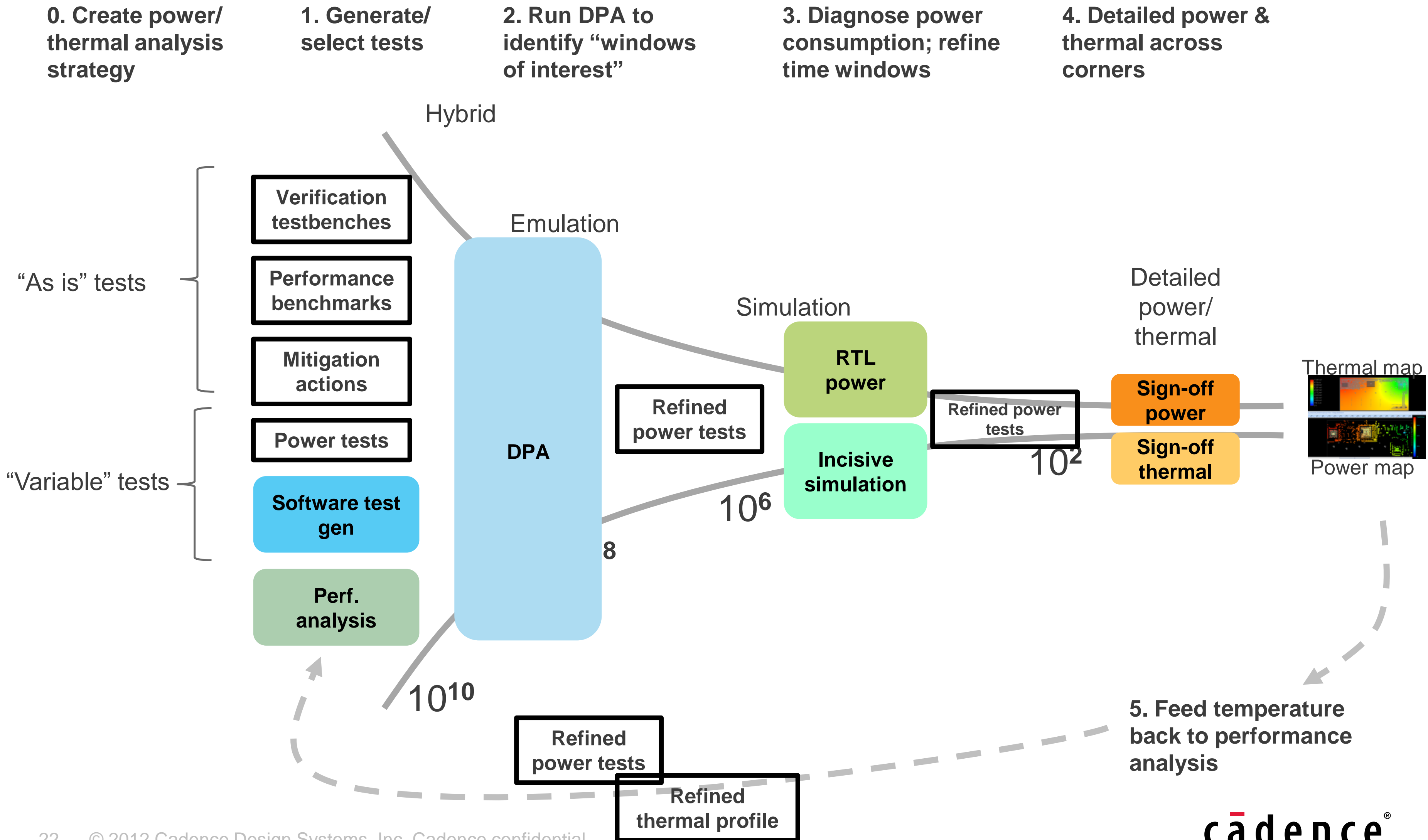
High-level view of flow

Use case "funnel" drives flow



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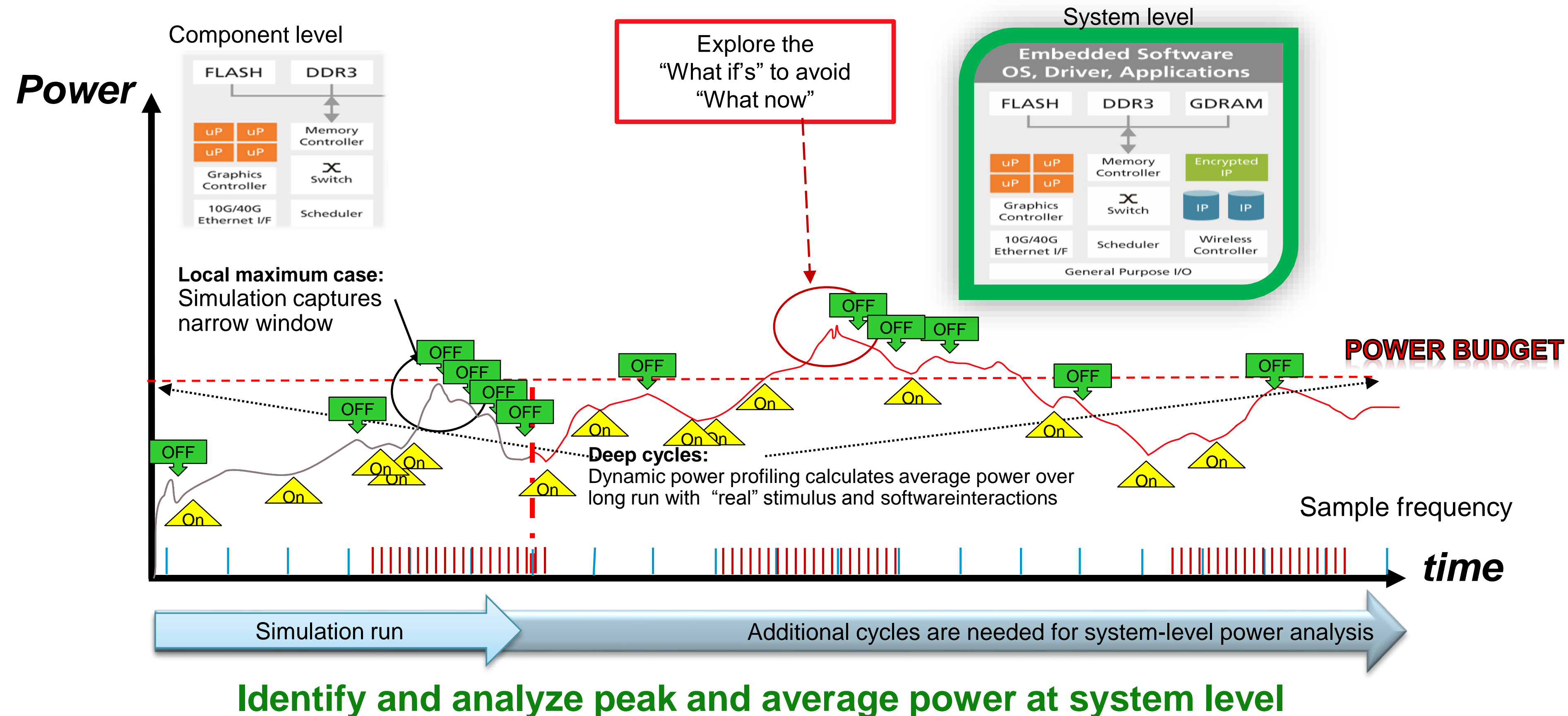
SoC power analysis requires "deep" cycles

At 100MHz for 10 seconds => 1 billion cycles



Identify and analyze peak and average power at system level

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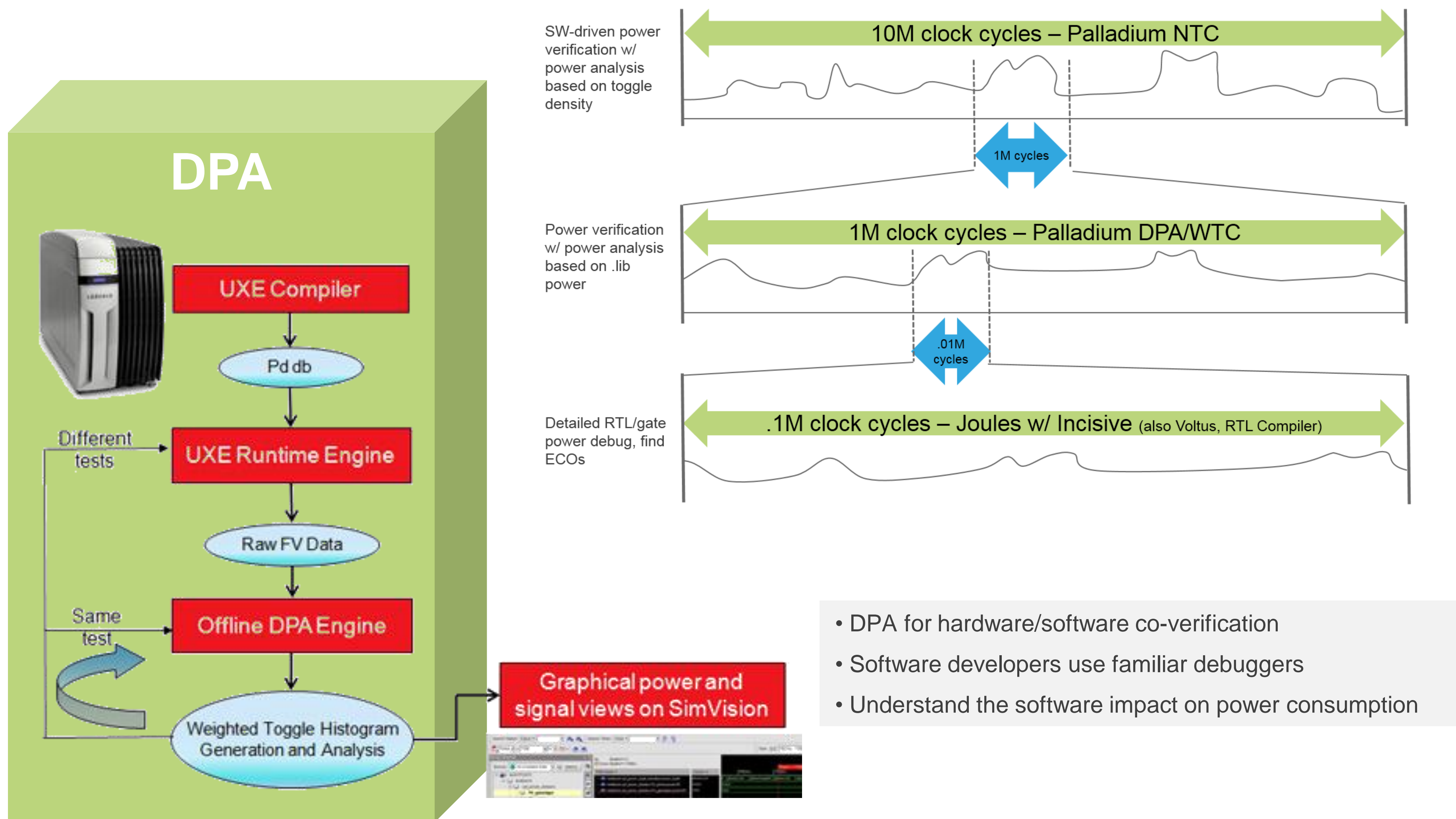
Power analysis: Emulation DPA (dynamic power analysis)
RTL & gate power w/ "deep cycles" capability



- DPA for hardware/software co-verification
- Software developers use familiar debuggers
- Understand the software impact on power consumption

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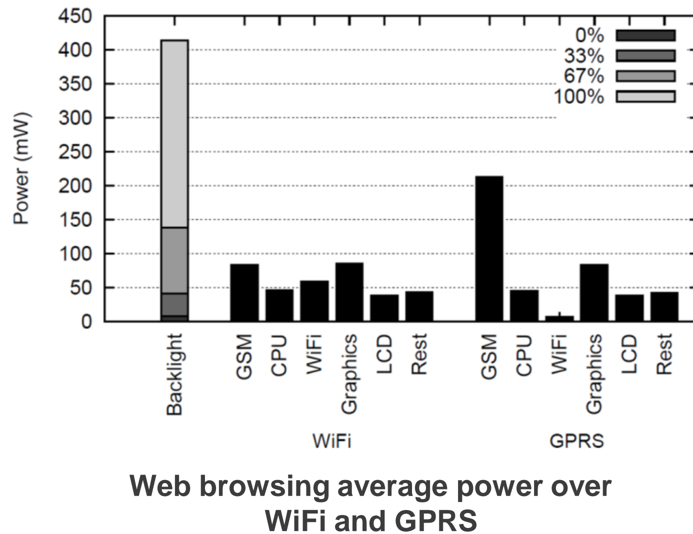
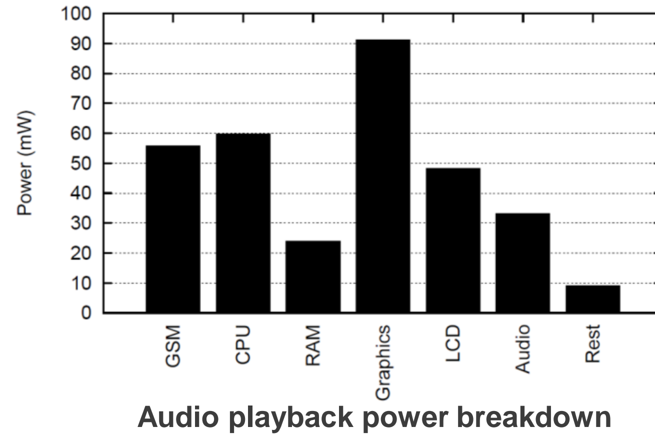
Characterize, virtualize

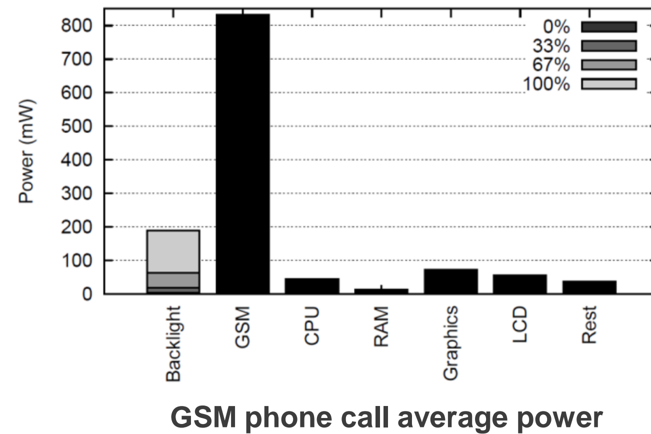
Case for hybrid model – many use cases are not CPU-dominated



Web browsing average power over WiFi and GPRS



Audio playback power breakdown



GSM phone call average power

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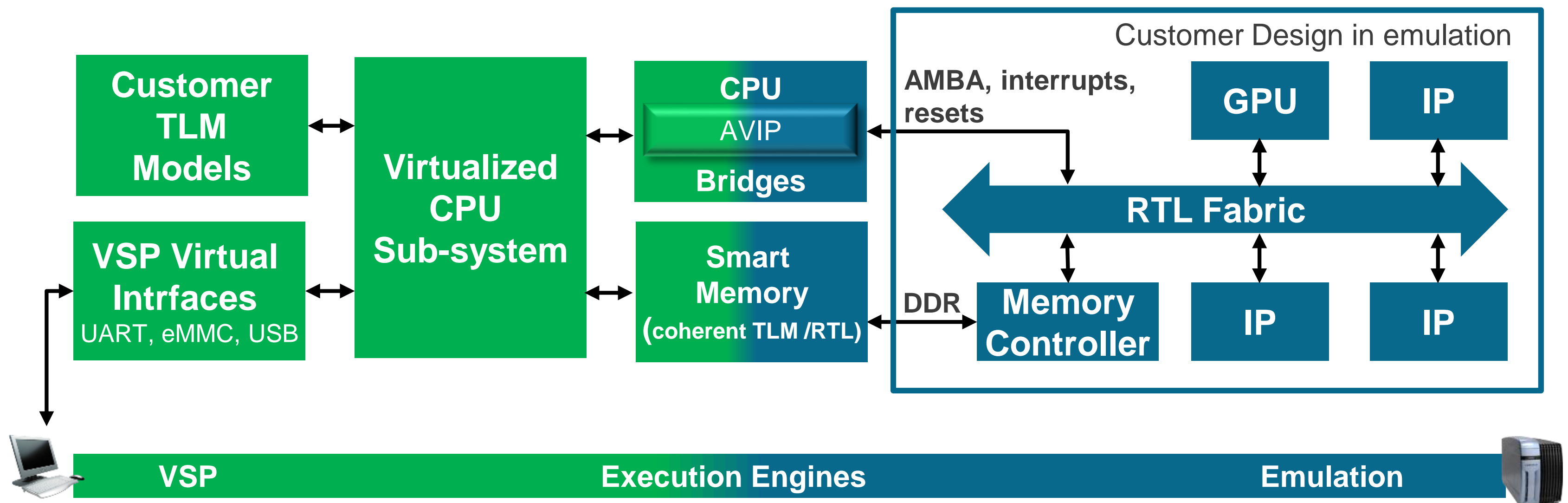
The emulation/VSP hybrid solution

- Bring-up SW early, finish by Tapeout
  - Bring-up and test Linux and drivers days after first RTL drop
  - Bring-up and test Android weeks before tape-out
  - Complete Linux / Android-based SoC testing by tape out
- Accelerate SW-driven SoC verification
  - 100X faster boot
  - 4X Faster OGL tests
  - Full HW/SW debug



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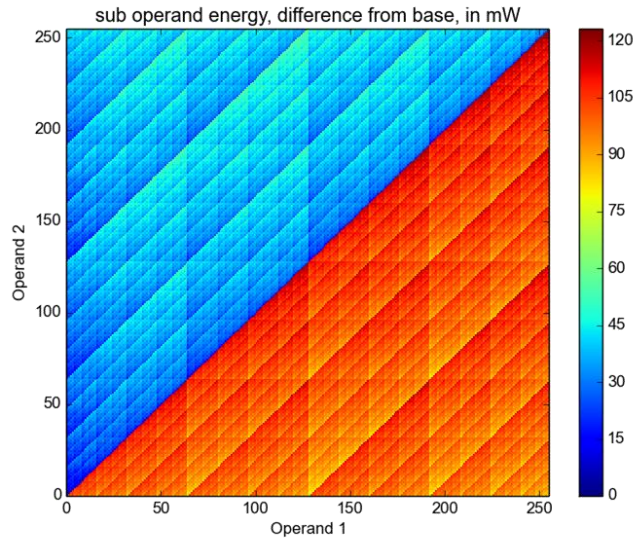
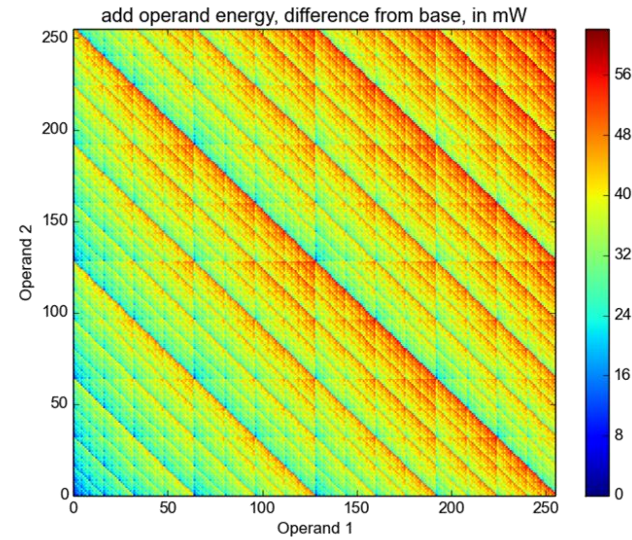
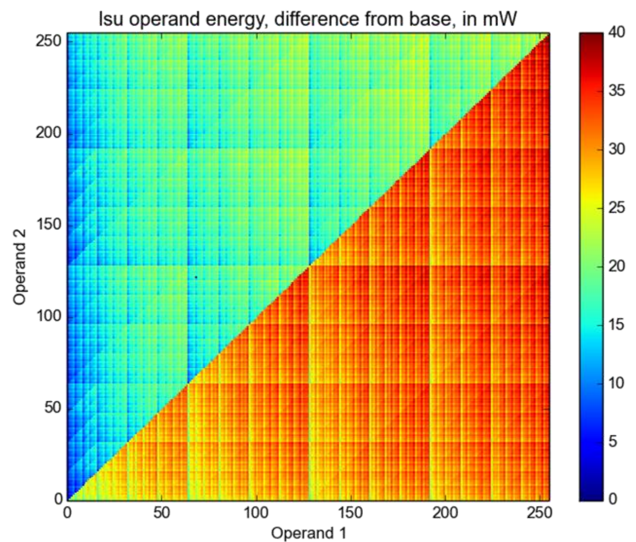
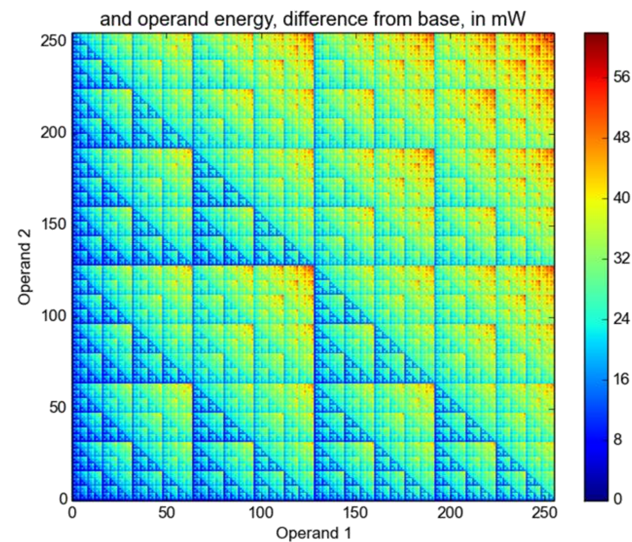
Data dependency: 10X difference per operation

Statistical distribution assumptions become important









Eder et al, Univ Bristol, 2015

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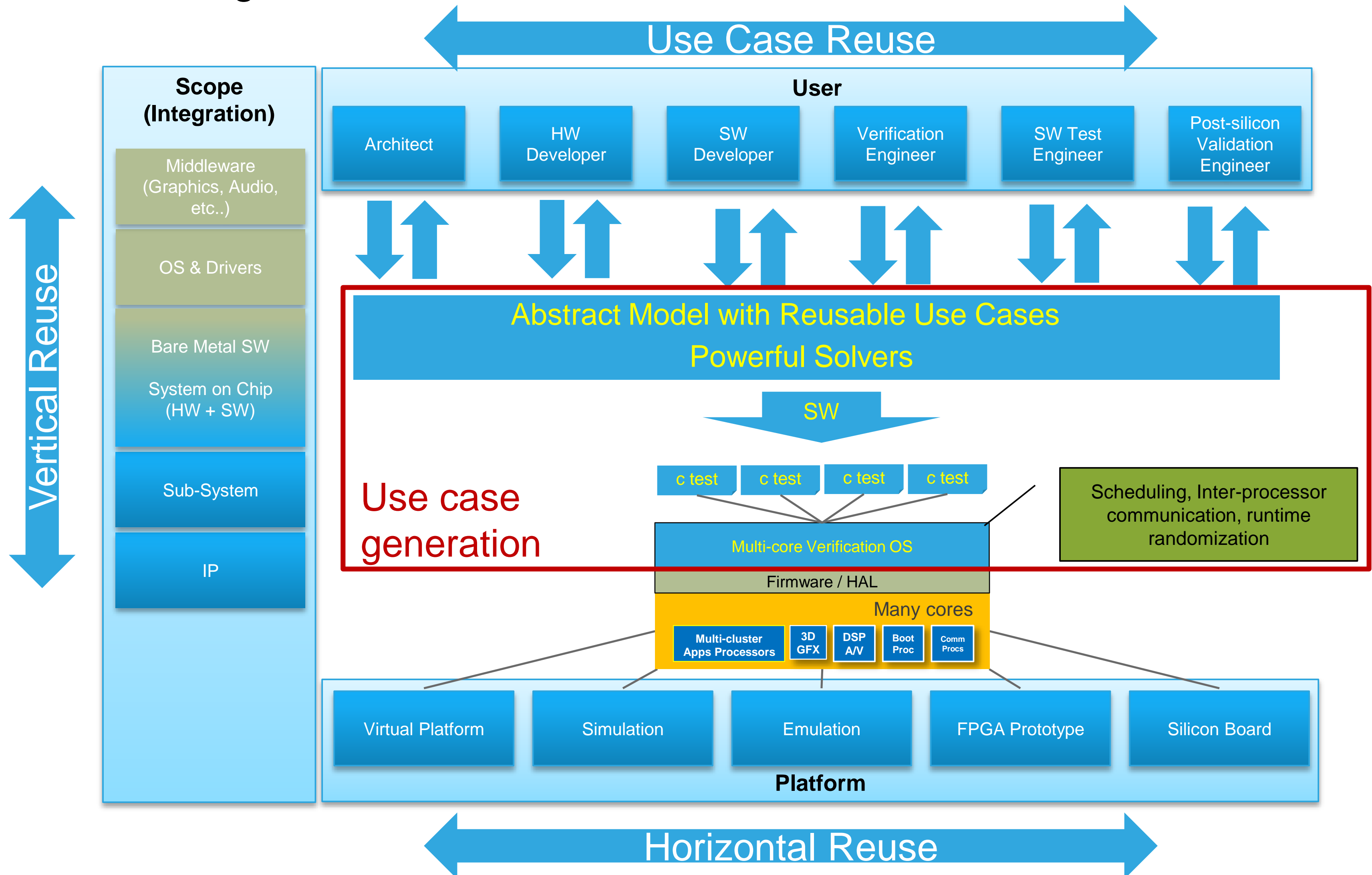
The Solution: Automated use case generation
Software test generation



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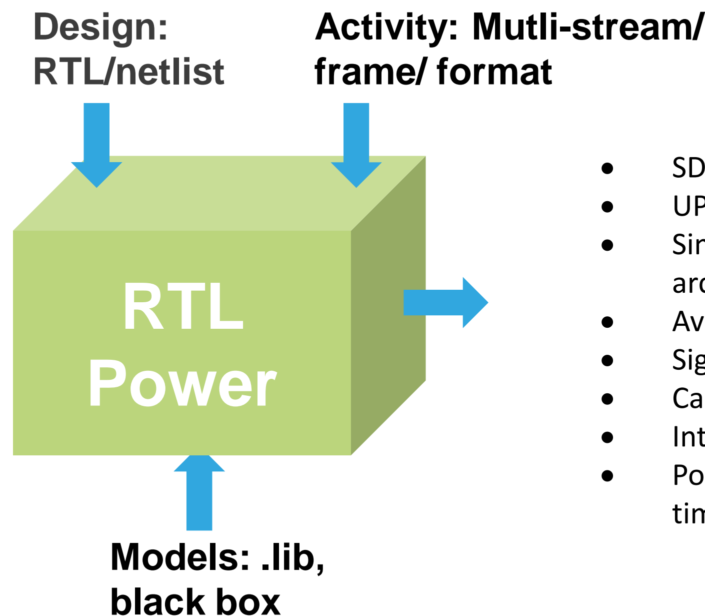
Power Analysis
RTL and gate power based on .lib models



Engine:
- Read design
- Quick synthesis
- Model process
- Activity prop
- Report gen
- Data export

- SDC compliant synthesis engine
- UPF/CPF support
- Simultaneous multi stimuli and frame based architecture for time-based power
- Average, time based, and incremental power
- Signoff calibrated power computation engine
- Calibrated clock tree and data buffer estimation
- Integration with emluation
- Powerful data mining including activity, power, timing, and area data

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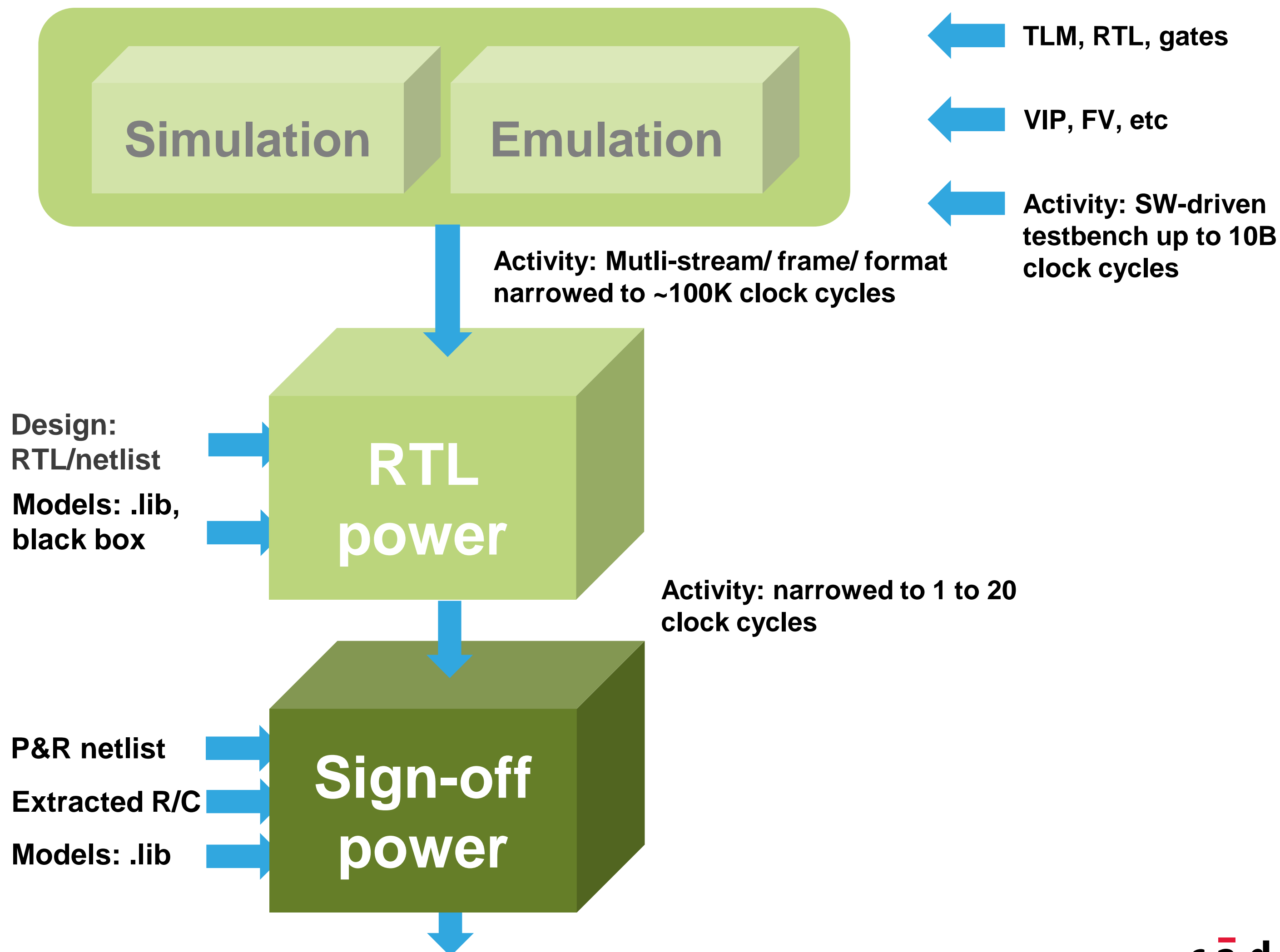
Power Analysis: Joules & Voltus progression
RTL and gate power based on .lib models



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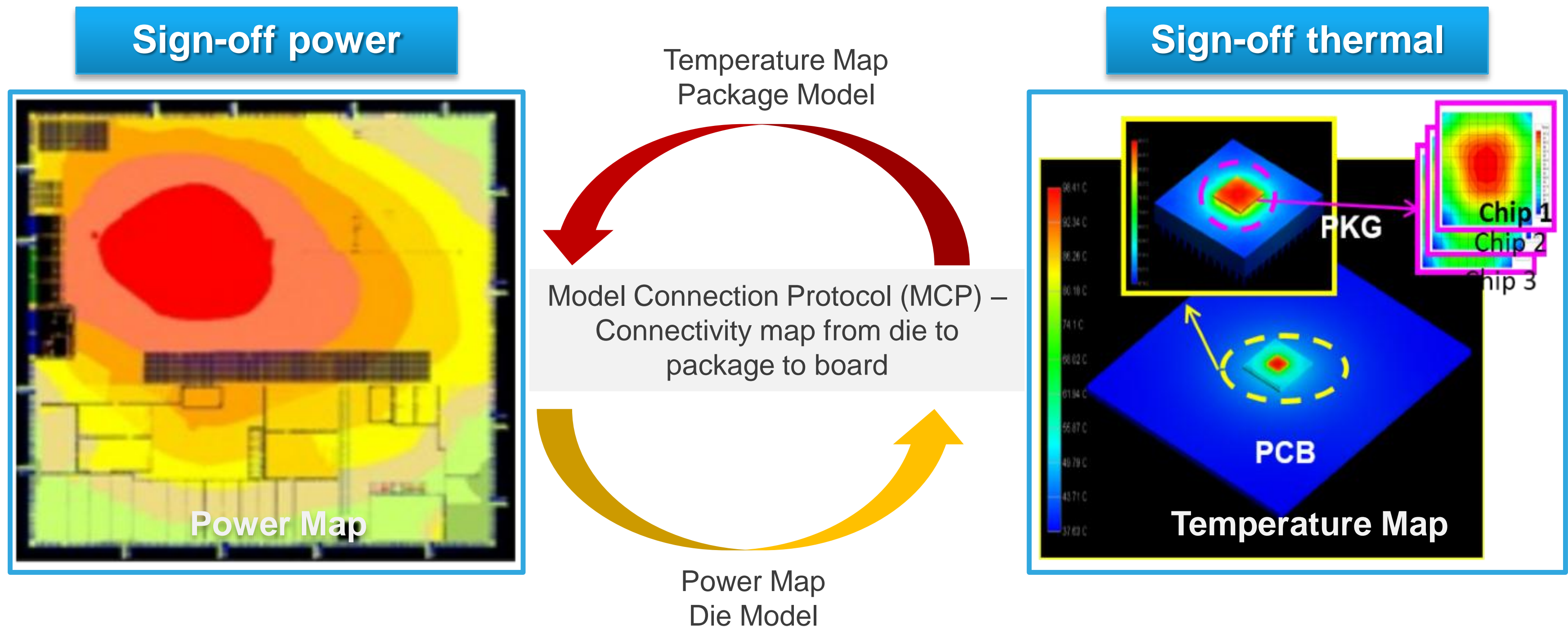
Chip-package-board thermal co-simulation



- Thermal computes Temperature map including chip, package and board
- Power computes temperature dependent power map of die
- Co-simulation until results converge

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Summary

- Power: is it a problem?
  - Verification technologies and methodologies are deployed
  - Analysis needs to migrate forward and encompass more use cases
- Power: it's not just about power
  - Performance and thermal are intimately interrelated to power
  - Need to progress towards holistic P-T-P solution
- Technologies
  - Verification technologies applicable for performance/thermal/power
  - Full suite across fabrics for design and analysis
- Power: No problem ! ☺

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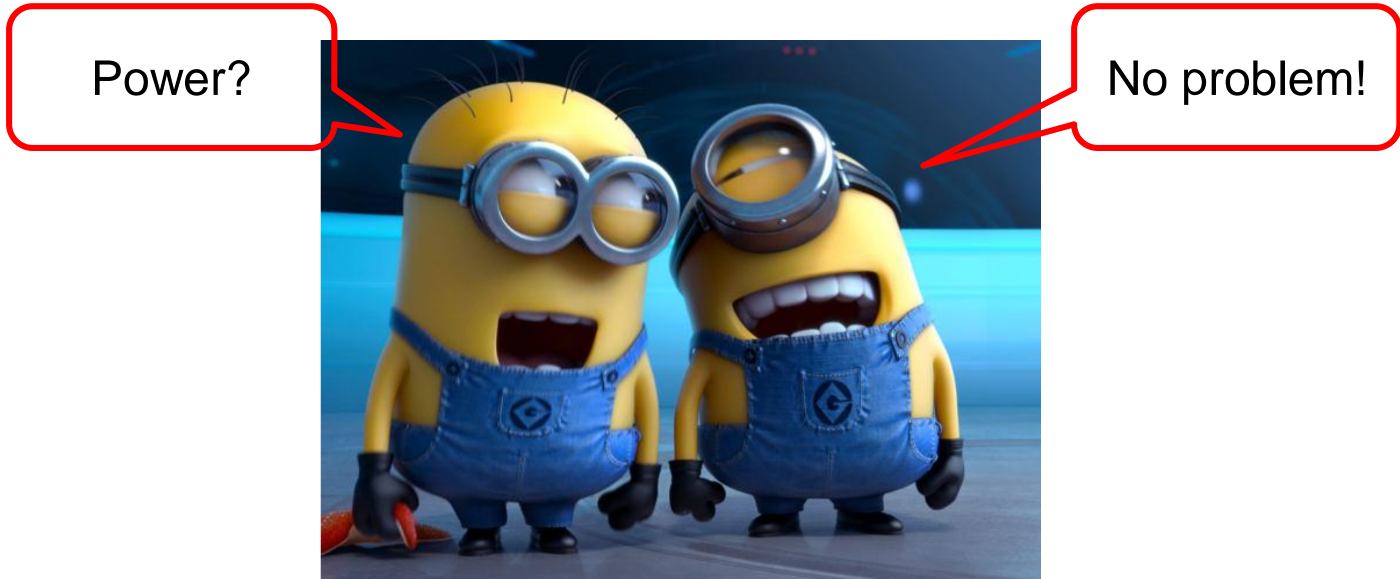
Thank You



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