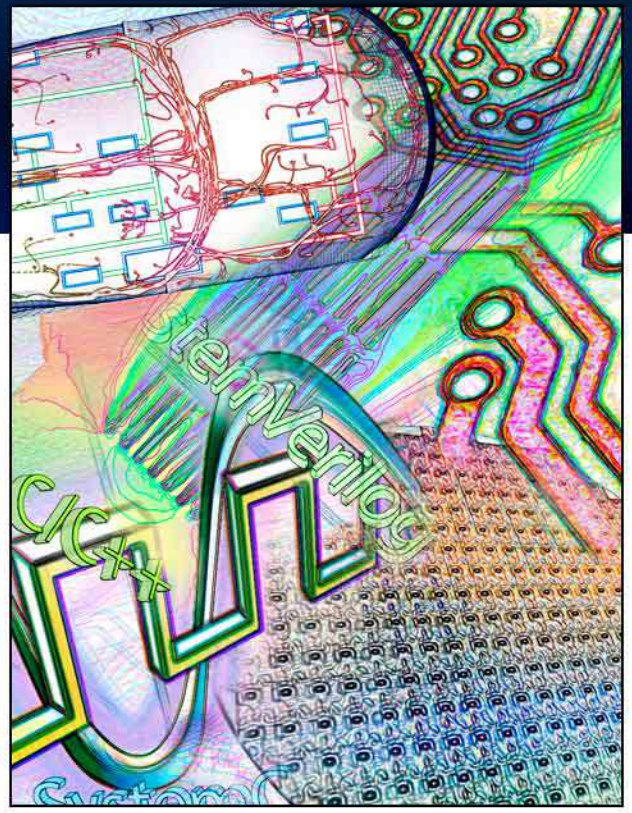


The need for Speed "Hybrid-emulation"

Russell Klein

Mentor Emulation Division

Electronic Design Process Symposium - 2015

Mentor Graphics®

"Software is Eating the World"

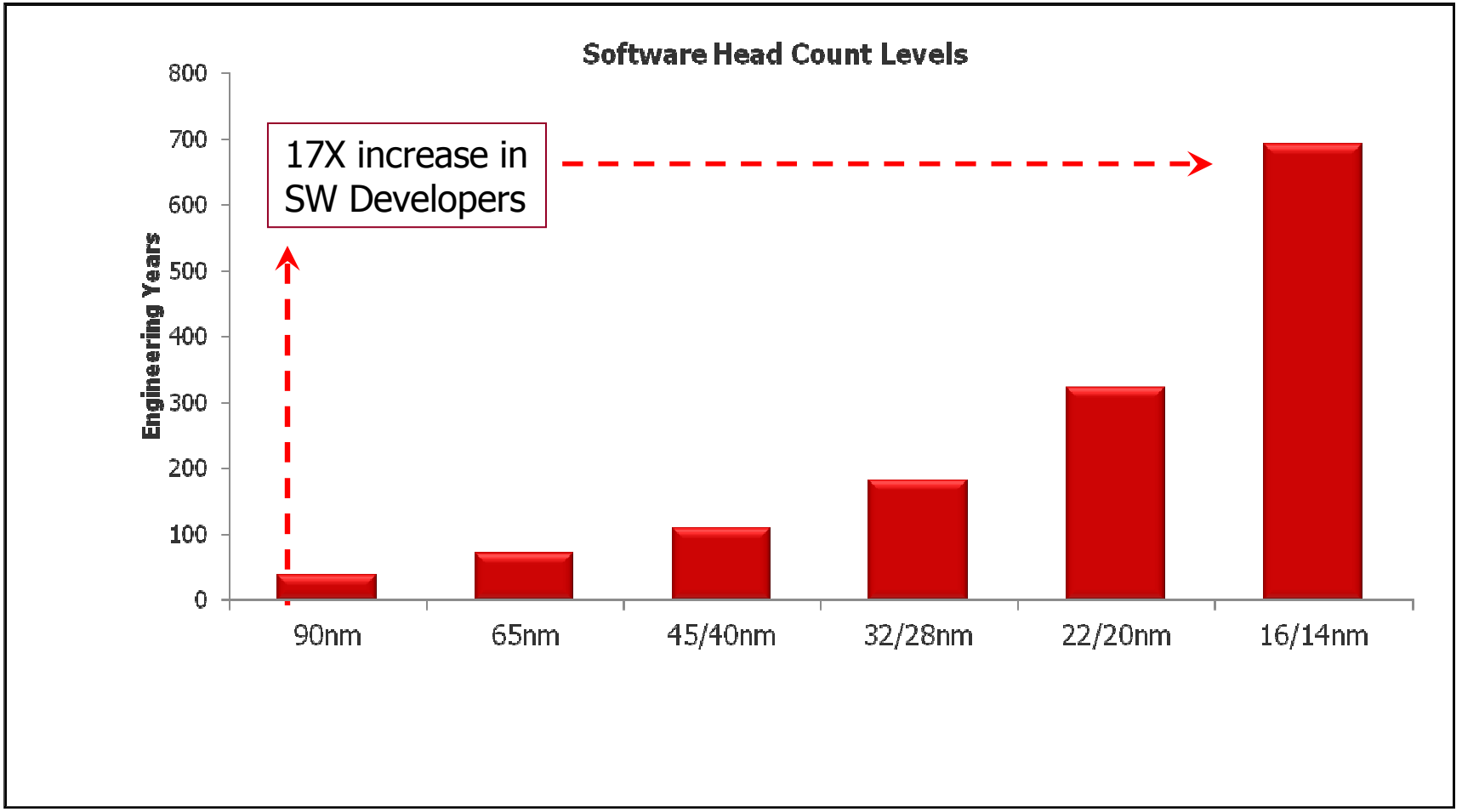
Marc Andreessen

Delivering an SoC is no longer just delivering silicon. It requires drivers, middleware, protocol stacks, and SDKs.

More functionality of systems is moving to software

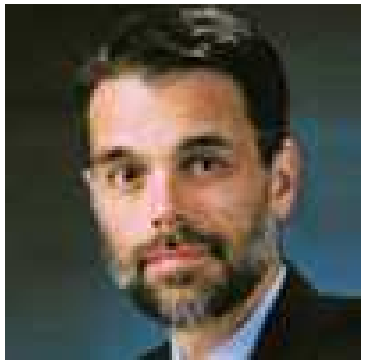
No one gets paid until the [device] drivers are done

Embedded Software Development Headcount Surges with Every Node



Source: IBS, 2013

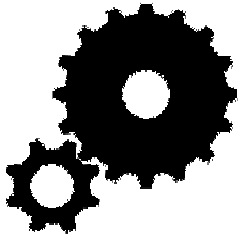
Widdoes Law



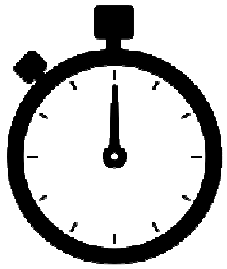
Dr. Curt Widdoes

- If you don't test it, it won't work
  - Applies to both hardware and software

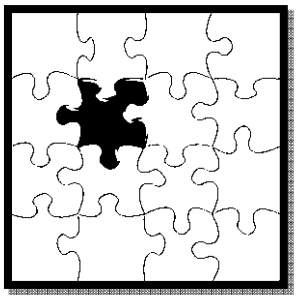
What does "work" mean?



- Functionally correct
  - Produces the right answer or behavior



- Fast enough
  - Meets performance requirements
  - Satisfies response times
  - Delivers on throughput

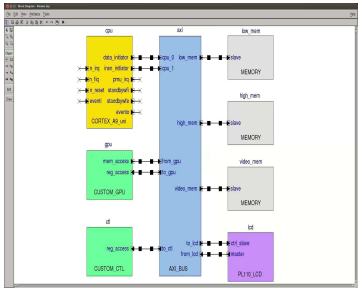


- Integrated
  - Functions correctly in the complete system
  - Does not interfere with other components

How do we test all that software?

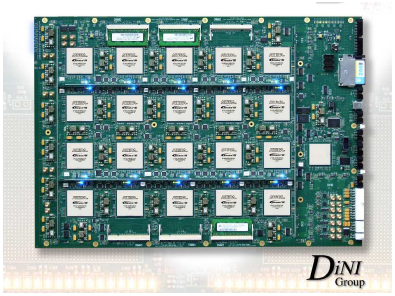
Before silicon is available…

Development board



Virtual Prototype

Veloce

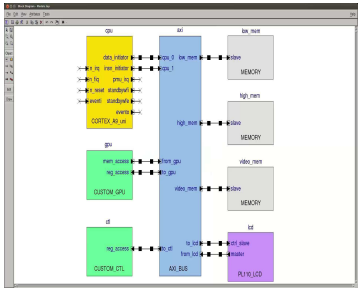


FPGA Prototype

How do we test all that software?

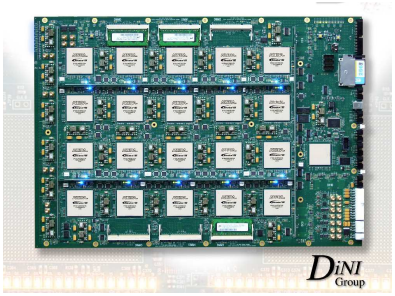
Before silicon is available…

Development board



Virtual Prototype

Veloce



FPGA Prototype

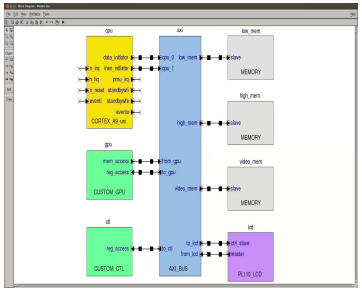
- Fastest – real time speed
- Accurate – for the processor
- Good SW debug capabilities

- No good way to model new hardware
- No HW visibility

How do we test all that software?

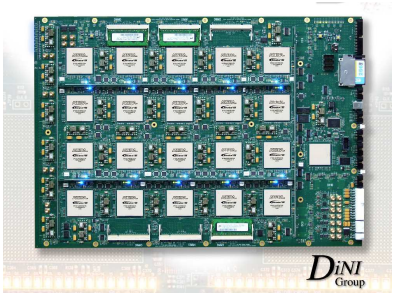
Before silicon is available…

Development board



Virtual Prototype

Veloce



FPGA Prototype

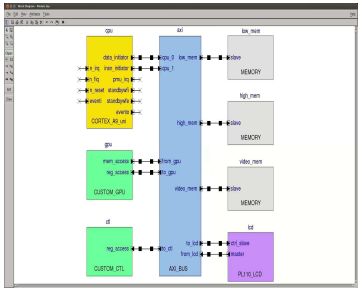
- Fast – ~100 MHz
- Functionally accurate
- Great SW debug capabilities

- May require significant modeling effort
- Limited timing accuracy

How do we test all that software?

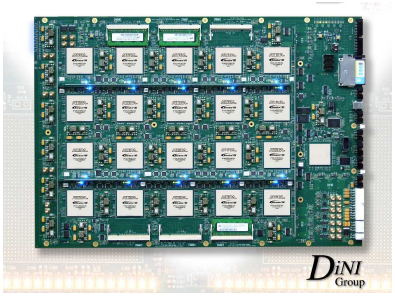
Before silicon is available…

Development board



Virtual Prototype

Veloce



FPGA Prototype

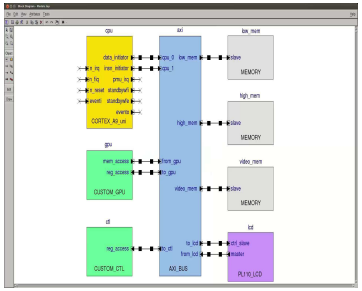
- Very Accurate – functional and timing
- Great SW debug capabilities
- Great HW debug capabilities

- Slow – for SW execution and debug

How do we test all that software?

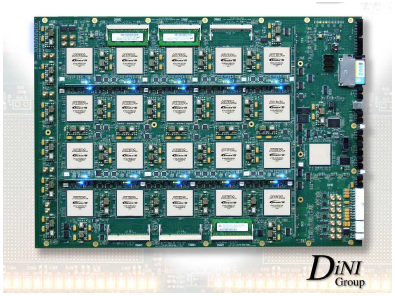
Before silicon is available…

Development board



Virtual Prototype

Veloce

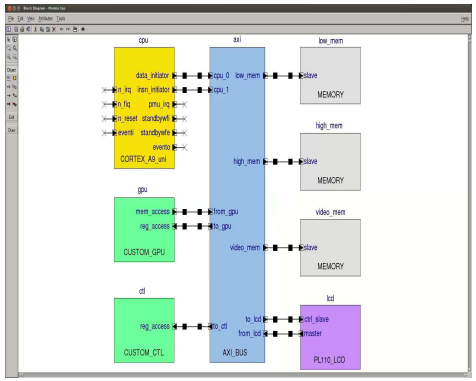


FPGA Prototype

- Faster than emulation
- Very Accurate
- Good SW debug capabilities

- Limited HW debug
- Limited capacity
- May involve significant porting effort

The best of both worlds



Virtual Prototype

Veloce

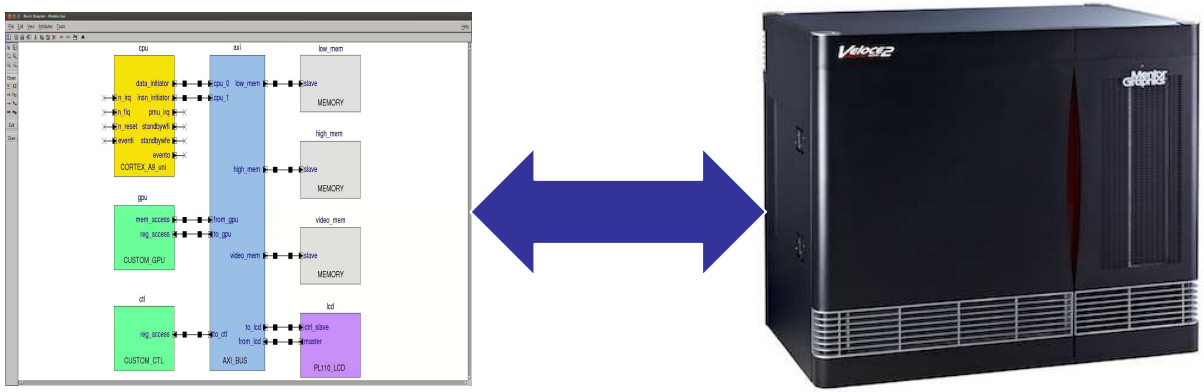
- Fast – ~100 MHz
- Functionally accurate
- Great SW debug capabilities

- May require significant modeling effort
- Limited timing accuracy

- Very Accurate – functional and timing
- Great SW debug capabilities
- Great HW debug capabilities

- Slow – for SW execution and debug

The best of both worlds

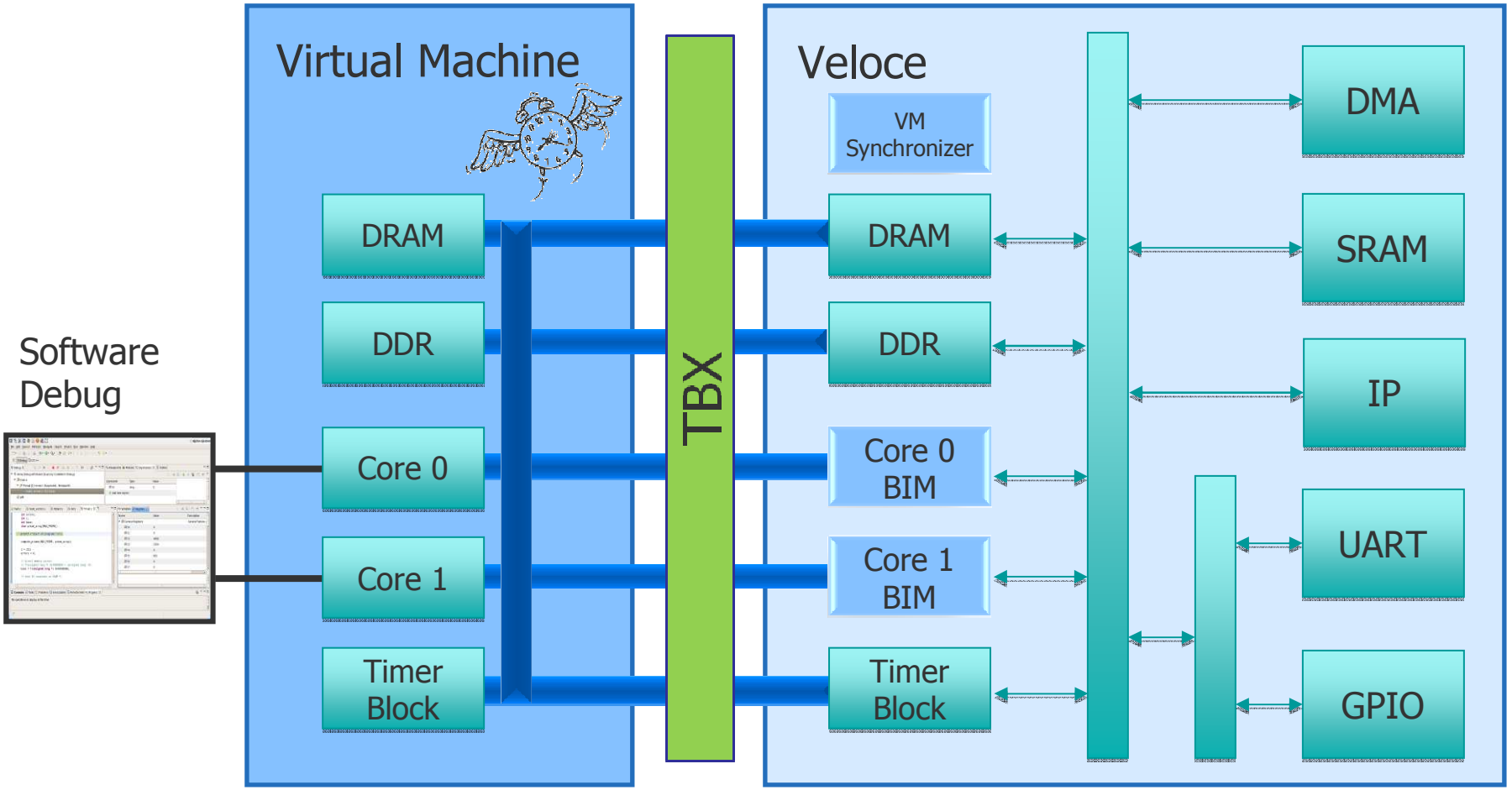


Virtual Prototype

Veloce

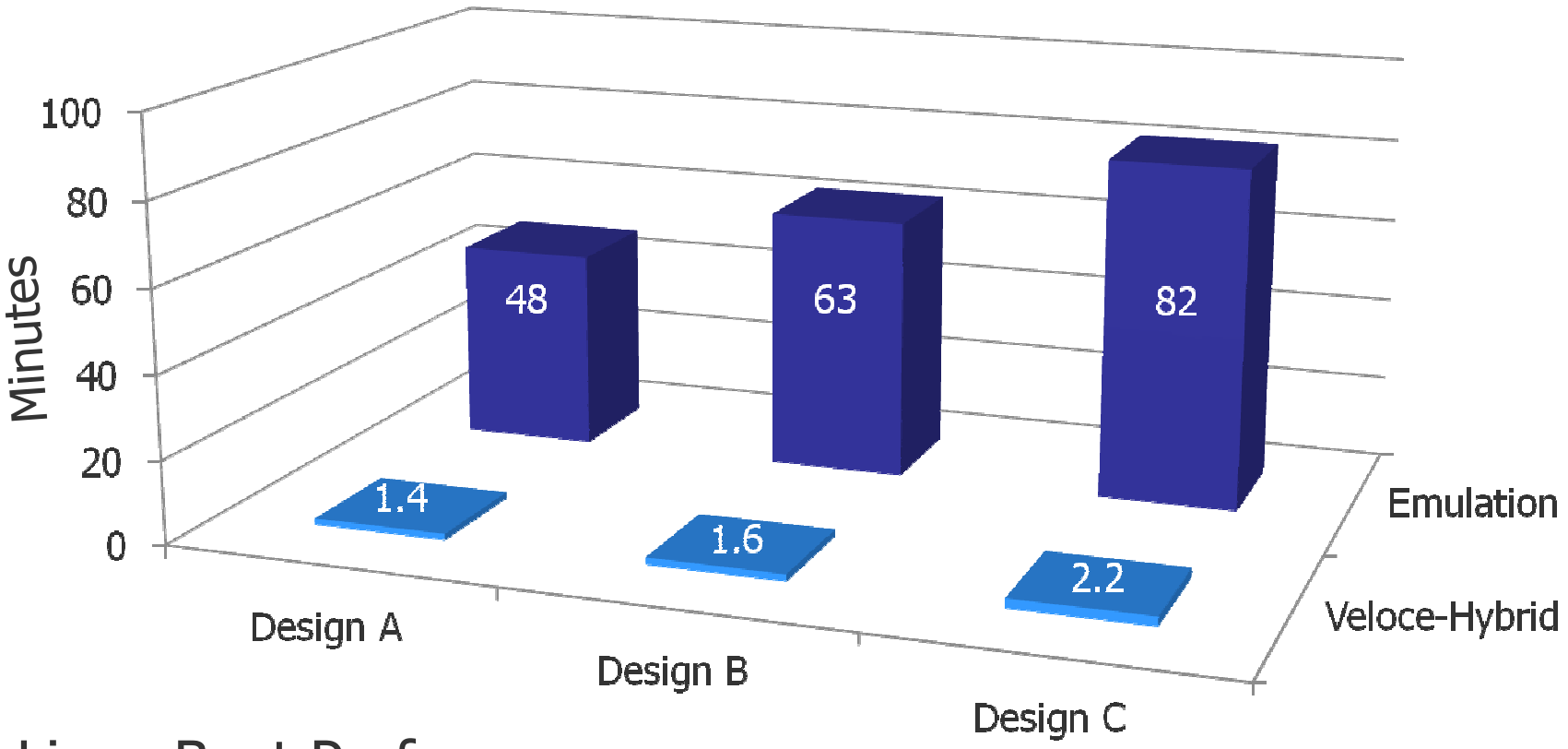
- Fast – ~50 MHz
- Great SW debug capabilities
- Great HW debug capabilities
- Very Accurate (for RTL) – functional and timing

Hybrid Emulation



- Moves CPU/memory subsystem from the emulator into a virtual machine

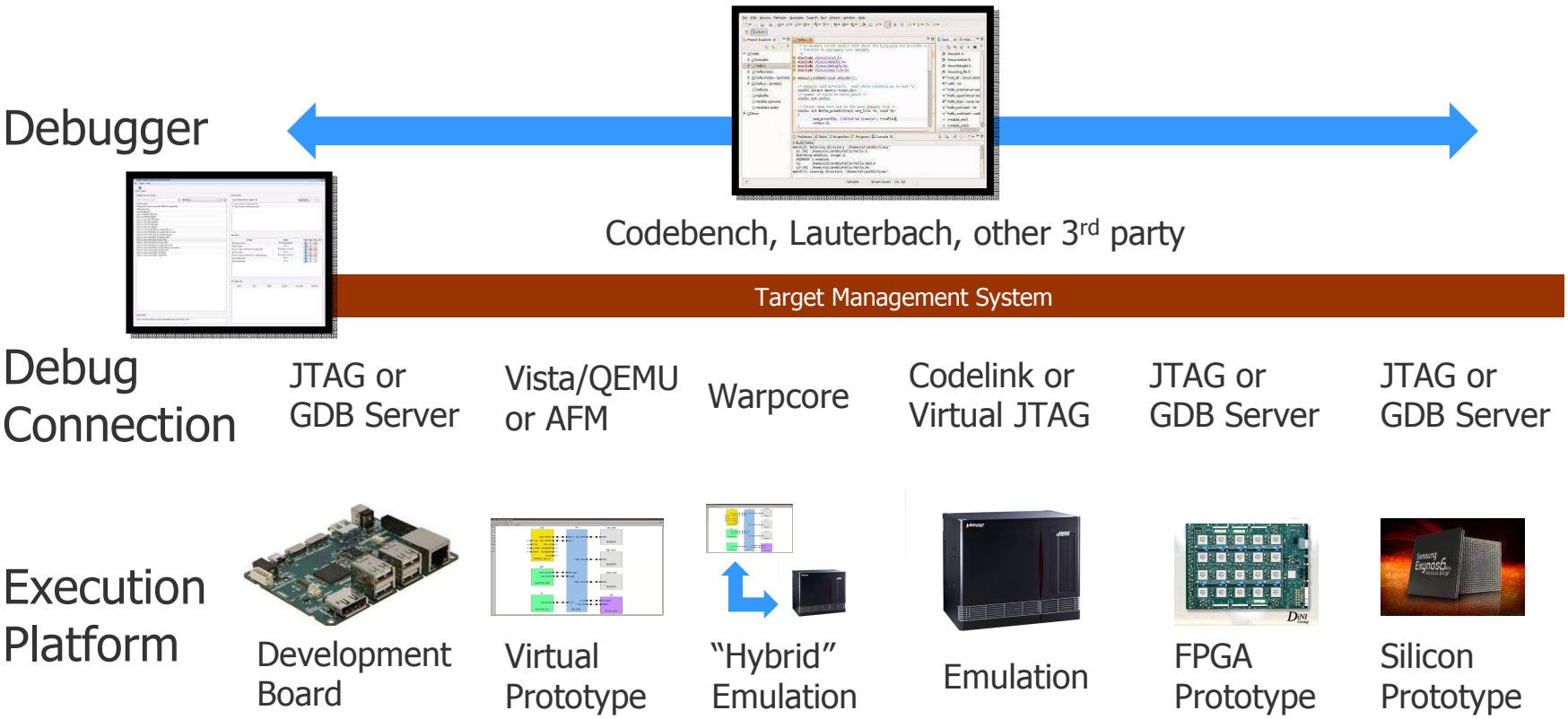
Real World Results



Linux Boot Performance

Often, the interesting things happen after the OS boot

Common Debug across the continuum



Hybrid Emulation

- Software is an increasing part of SoCs
  - And it all needs to be verified
  - Finding bugs early impacts schedules and costs less
- Emulation provides a great platform for software debug and development, except that it runs too slowly
- Virtual Machines integrated with Veloce provides the performance needed for more software debug tasks than emulation alone
  - Needs to be used as part of a set of approaches which deliver the right mix of performance and detail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