Stop Abstracting!
Use the Real Design Earlier for Software Verification Using Hybrid Approaches

Frank Schirrmeister
EDPS 2015
Monterey

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Confessions of a ESL-holic:
I used to think it is all about abstraction…

News & Analysis

Cadence adds system-level design tool to EDA flow

Cadence adds system-level design tool to EDA flow

Michael Santarini
1/10/2000 04:17 PM EST
Post a comment

NO RATINGS
LOGIN TO RATE

News & Analysis

Cadence Partners With Electronics Innovators To Accelerate Delivery Of NewEnvironment For Software And Hardware System Design

Cadence Partners With Electronics Innovators To Accelerate Delivery Of NewEnvironment Fo Software And Hardware System Design

EE Times
12/2/1997 08:00 PM EST
Post a comment

NO RATINGS
LOGIN TO RATE

News & Analysis

Cadence halts sales of Cierto VCC co-design tool

Cadence halts sales of Cierto VCC co-design tool

Michael Santarini
3/19/2002 05:18 PM EST
Post a comment

NO RATINGS
LOGIN TO RATE

Cadence Issues Blueprint to Battle 'Profitability Gap'; Counters Semiconductor Industry's Greatest Threat

Expanded Collaboration and New Product Family Enable Customers to Battle Growing Threat to Future of Innovation in Electronics

SAN JOSE, Calif., 27 Apr 2010

Cadence Announces Breakthrough in System Development to Meet Demands of 'App-driven' Electronics

Industry-first Suite Approach Bridges Hardware and Software, Reduces System Integration Time by Up to 50 percent

SAN JOSE, Calif., 03 May 2011

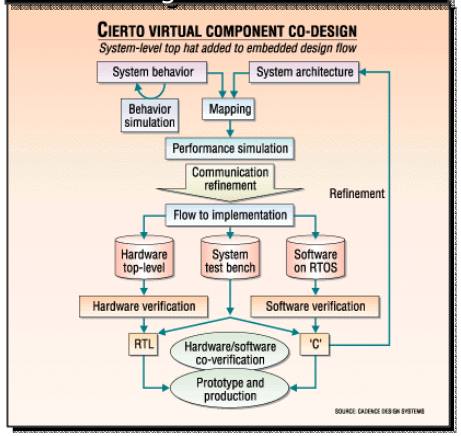
Cadence Design Systems, Inc. (NASDAQ: CDNS), a leader in global electronic design innovation, today announced a

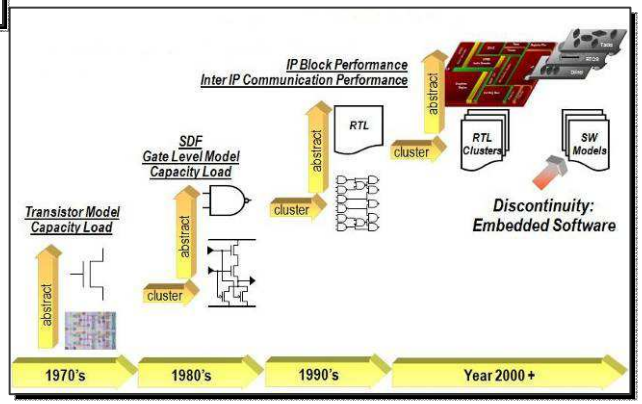
DAC 2014—ESL Design Is Dead... Long Live ESL!

Comments(0)

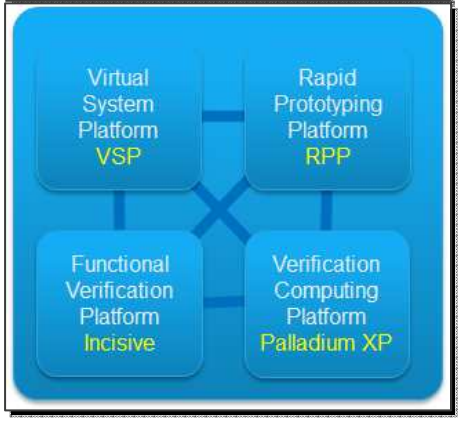
Next week the EDA industry is getting together in San Francisco for Design Automation Conference 2014. As I pointed out in a recent blog called "Confessions of an ESL-Aholic", the scope of electronic system level (ESL) design has changed quite a bit over the last 15 years, but there is still a lot of promise, and a lot to come. The basic premise of my soberness on classic ESL is that the basic momentum upwards in abstraction continues—as indicated in my graph dated ca. 2001 below—raising the level of abstraction from transistors to gates to RTL and inevitably above RTL.

2000: Cadence adds system-level design tool to EDA flow





2011 – System Development Suite Vision



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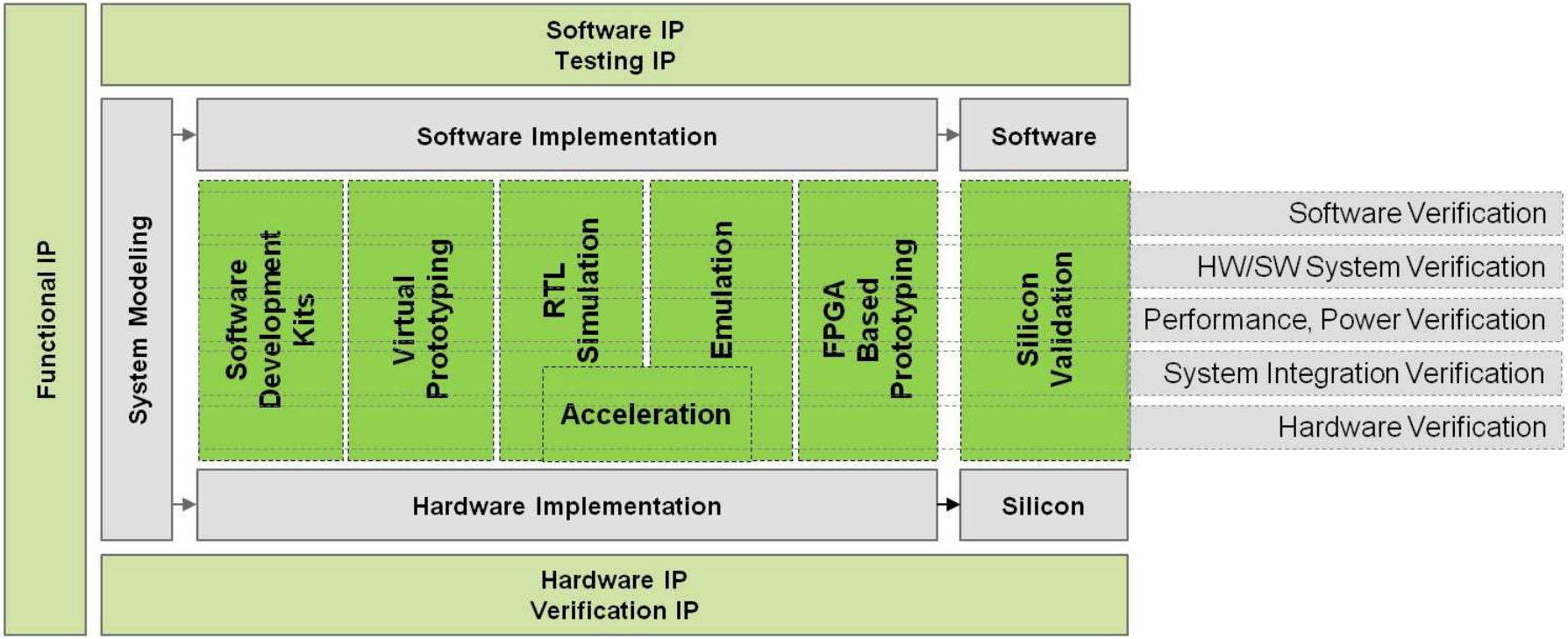
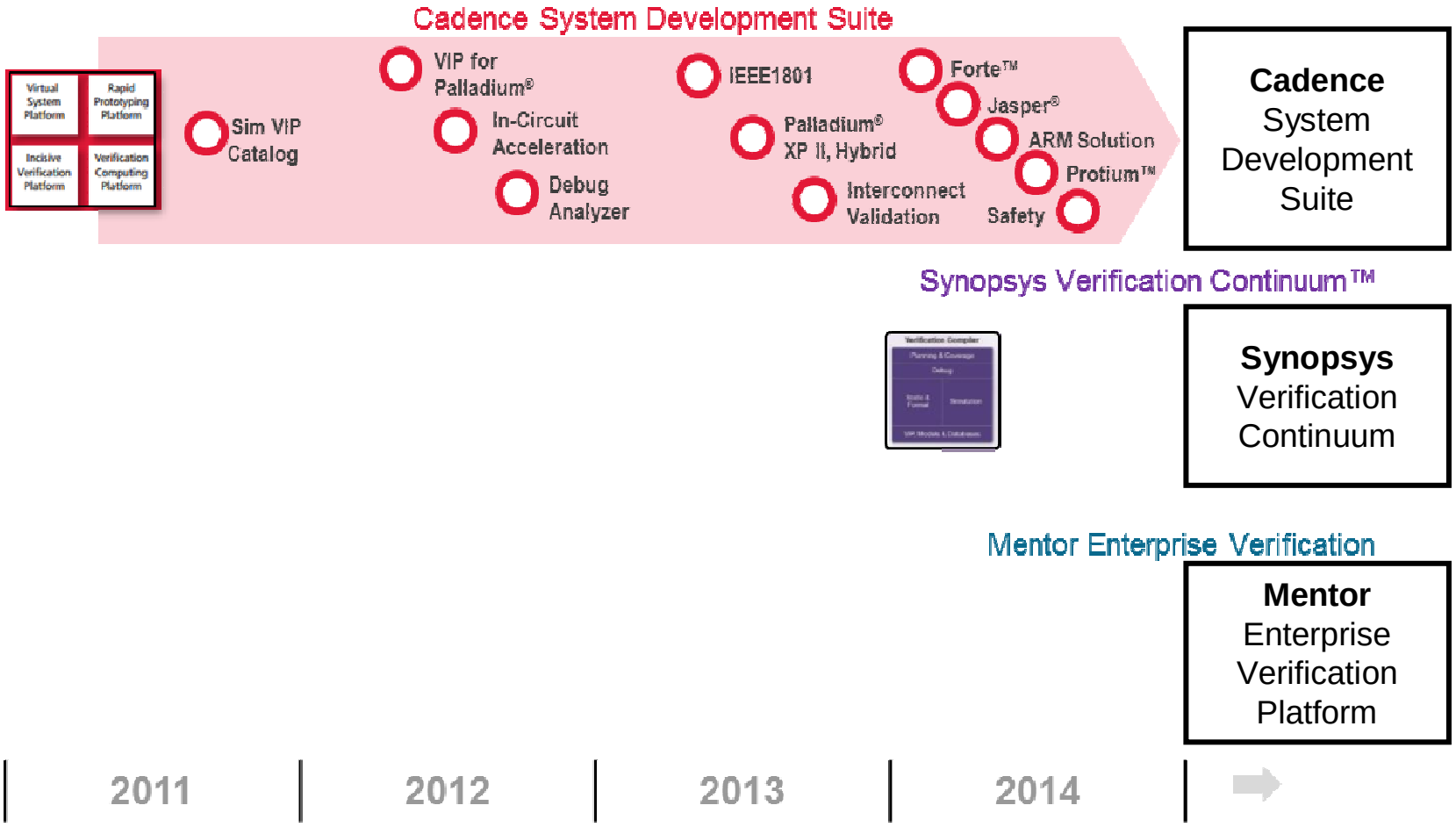
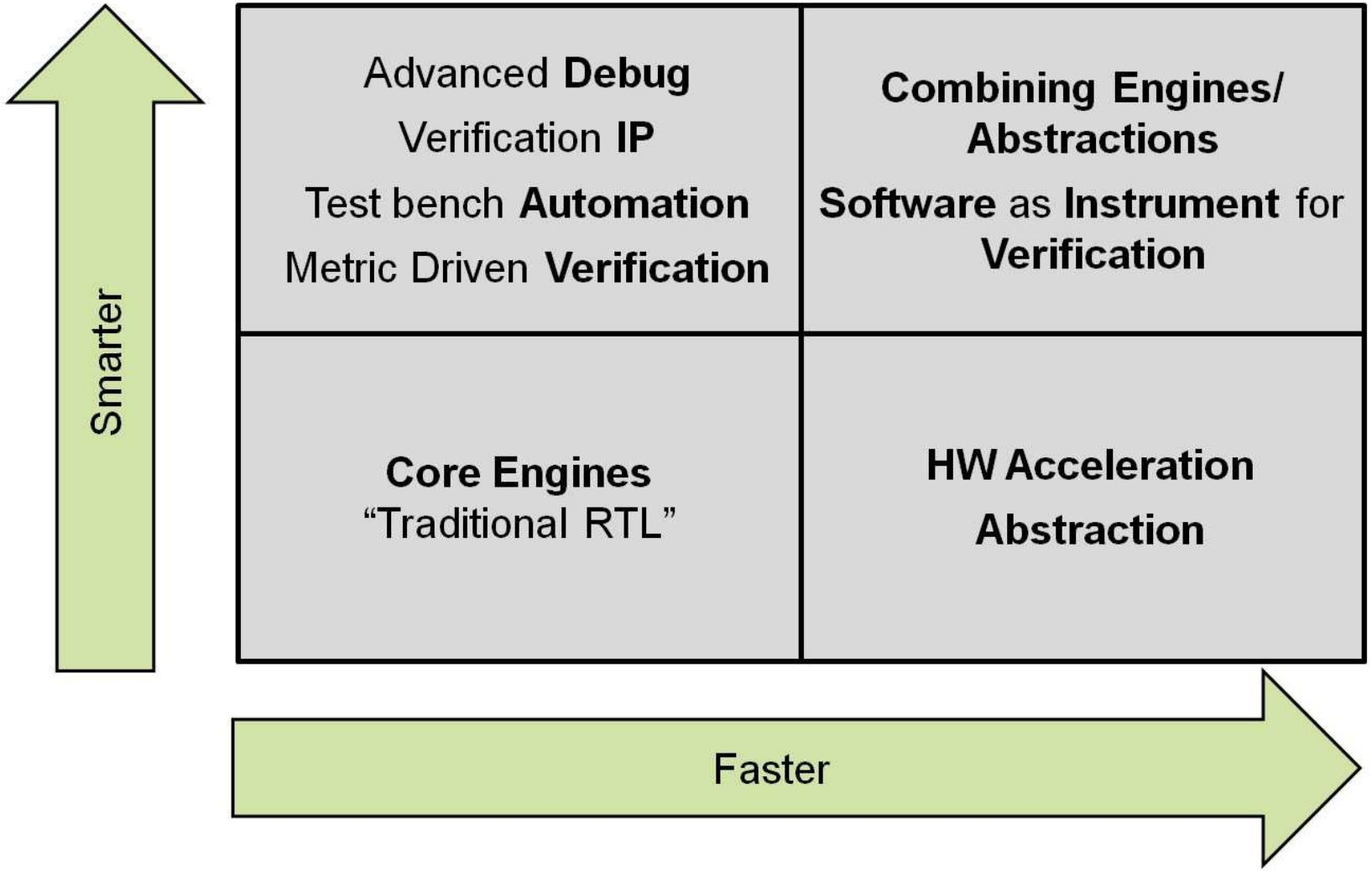
Well, It's not …
It's about the Continuum of Engines …



Unusual Agreement within EDA

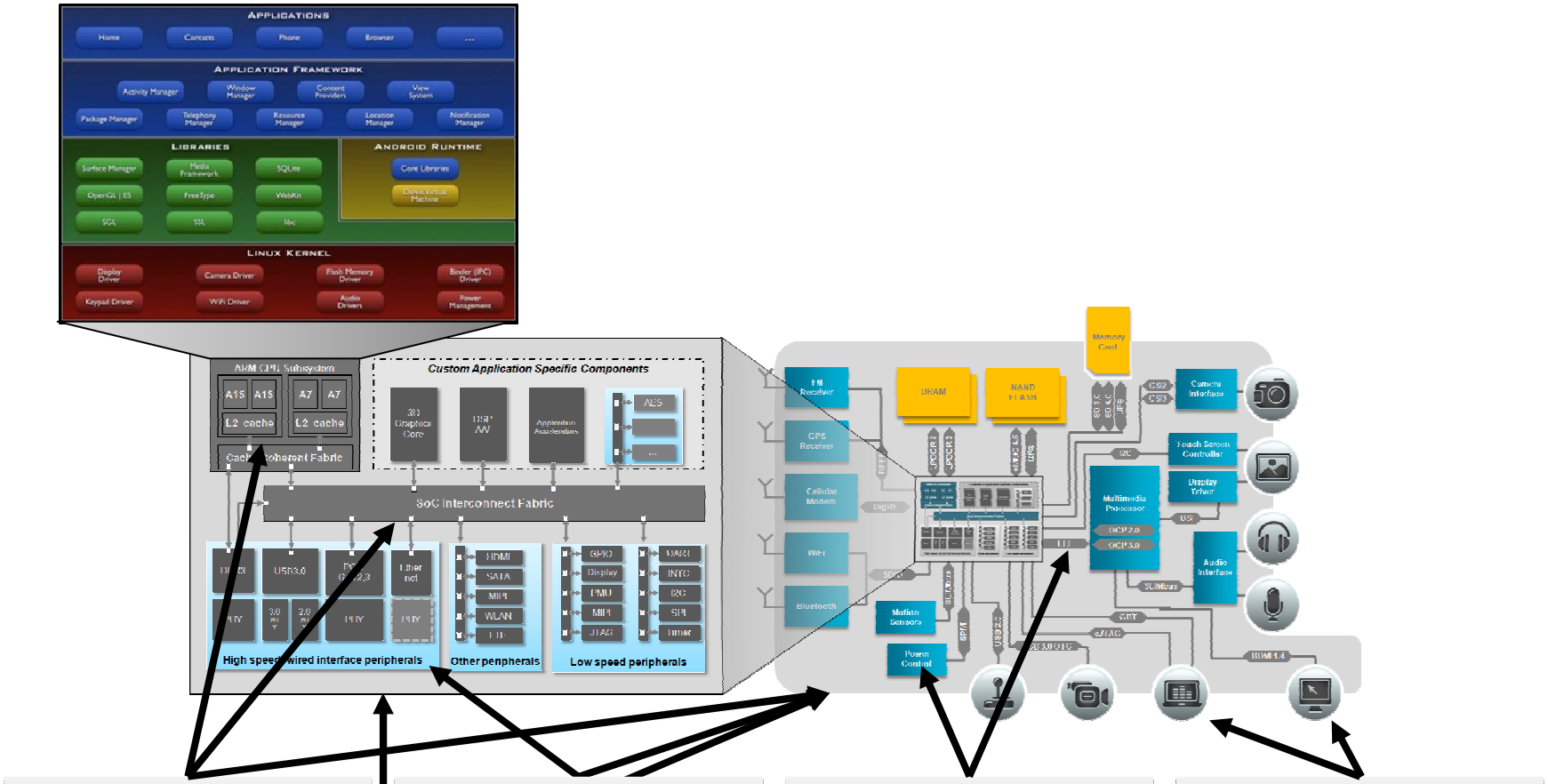


The key trends dictate a mix!



Complex Projects Require Many Model Types

Need for optimized reuse of existing IP assets



High-level models
C or SystemC

RTL models
Verilog, VHDL, SystemVerilog

Silicon / hard-macros
Test chip, silicon sample

System and I/Os
Motherboard, PCIE, USB

Instrumentations
Assertions, monitors, checkers

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TLM – Emulation Hybrids
for Early OS and SW Bring-up

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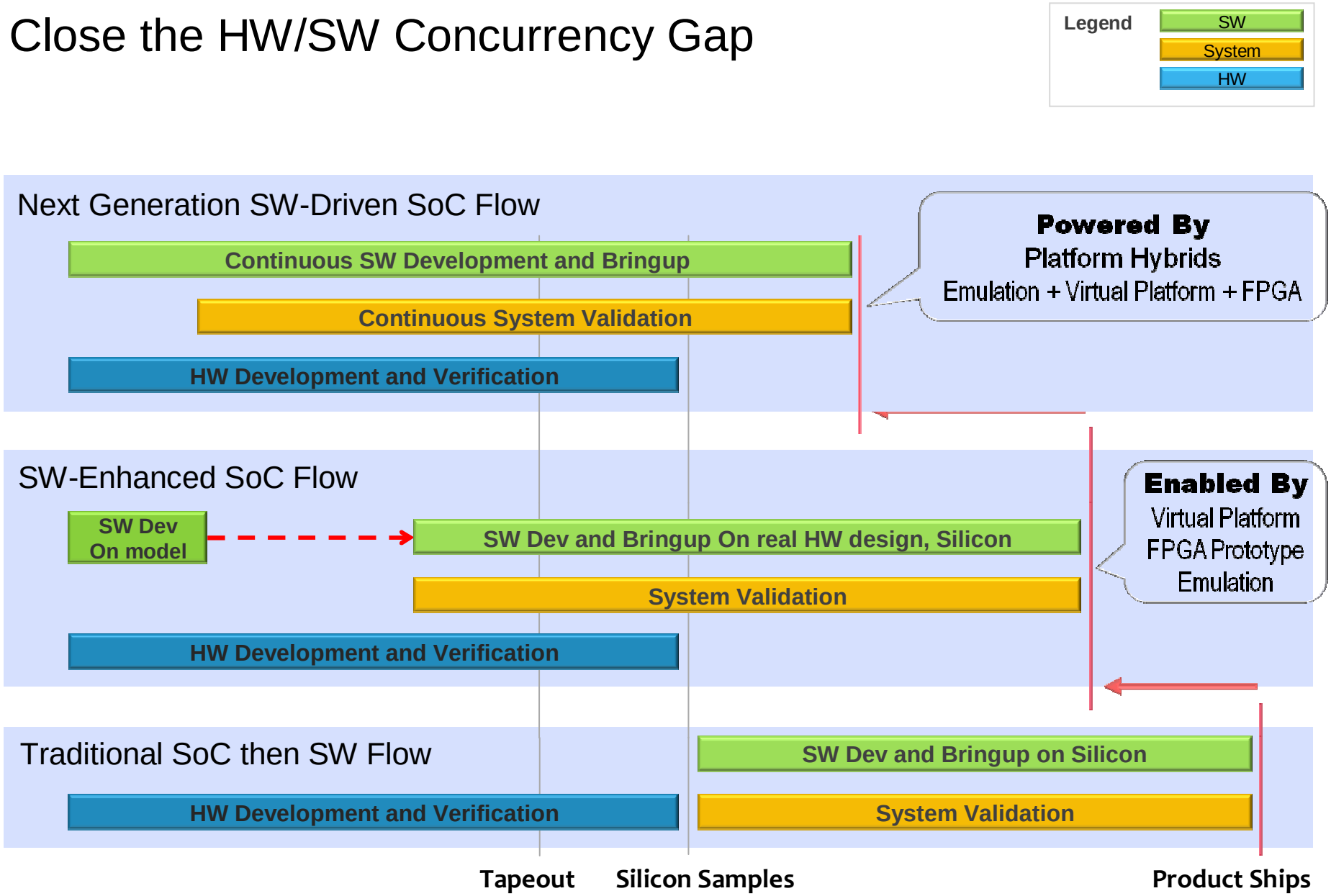
Close the HW/SW Concurrency Gap



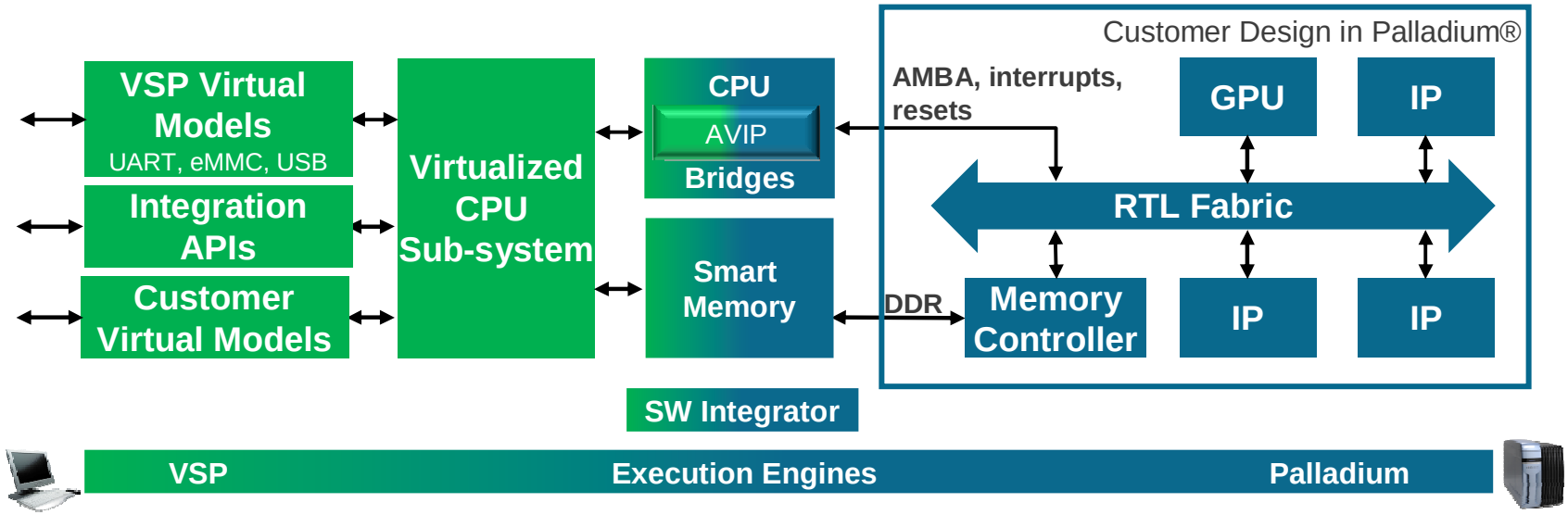
The Palladium/VSP Hybrid Solution

Architected for SW Performance

- High-speed virtual platform
- Asynchronous HW/SW Execution with Interrupt driven sync
- High-Speed Multi-Domain Memory Coherency

Designed to integrate HW and SW flows

- Does not require changes to HW or SW stacks
- Virtual connections into SW Engineer's environments
- Seamless hybrid execution for both HW and SW users



Proven Methodology, Unique Expertise

- Cross-platform and design integration expertise
- Exclusive hybrid methodology delivers performance and repeatability
- Proven during successful application to SW-rich SoCs

Hybrid performance with SW Integrator
Compared to an All-RTL in Emulation Configuration

Metric	All RTL in Palladium*	Hybrid**	Increase
Linux boot (minutes)	30	0.5	**60X**
Android boot (minutes)	900	15	**60X**
Windows RT boot (min.)	1800	30	**60X**
512x512 2D test (min)***	30	2	**15X**
# Emulation gates used	70 Million	40 Million	**0.6X**

* 70 million gate application processor, all blocks in Palladium®

** Virtualized CPU sub-system with register model of L1 and L2 caches. All other SoC blocks in Palladium.

*** Includes Linux boot, data preparation, image processing by HW engine and result checking. 1.3 million memory transactions. All boot numbers are full production images. Linux includes all drivers. Android and Win RT with SW rendering

Target Application
- Large, compute intensive SoCs

Target Users:
- HW-Dependent SW engineers,
- System validation engineers

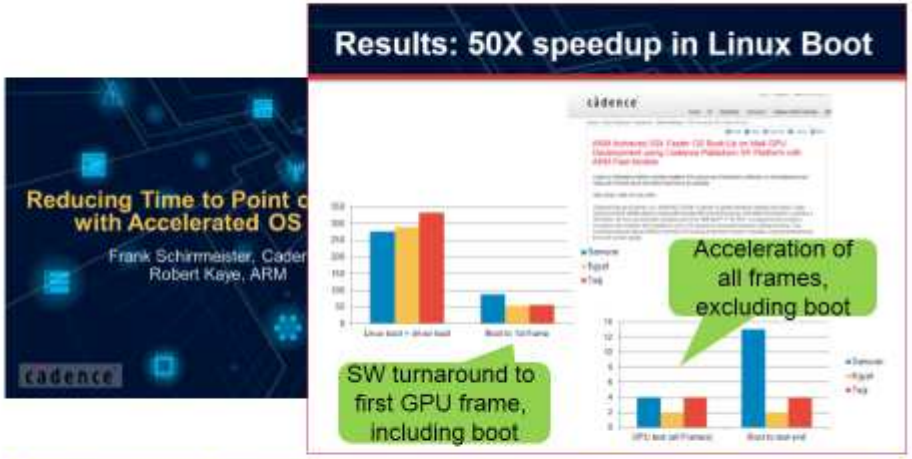
Accuracy (see notes for details)
- SW: Delivers programmers-view accuracy
- HW: Full accuracy except for timing between virtual CPU and SoC fabric
- Memory: in fast mode, memory transactions are performed back-door. Thus, hybrid models not recommended for power or performance estimation

Performance Results

- Boot OSes, run real world applications and benchmarks
- Linux kernel boot
  - Palladium only = 45 mins
  - Hybrid = 2 mins
- Android
  - Palladium only = Hours*
  - Hybrid = 40 - 50 mins
- Windows
  - Palladium only = Days*
  - Hybrid = 75 - 90 mins

ARM Mali - 2014

High-Performance OGL-based GPU Validation



"By using Cadence Palladium Hybrid technology to combine ARM Mali-T760 emulation with ARM Fast Models, we reduced the OS boot-up time, allowing us to run more extensive system-level software workloads and improve product quality."
- Hobson Bullman, general manager, ARM development solutions group

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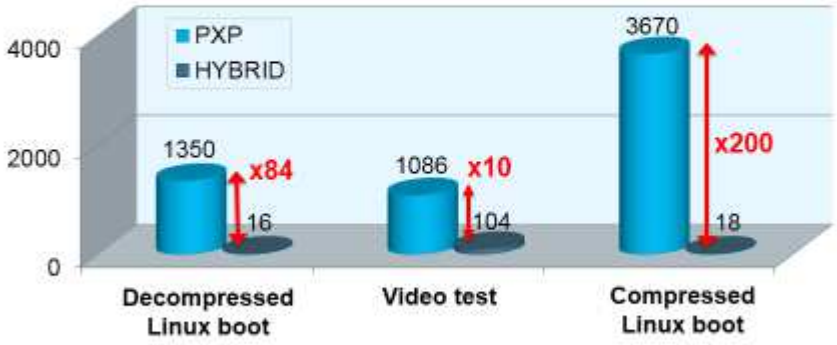
Results

CSR

- Runtime comparisons
  - Palladium compiled at 1.5Mhz, CAKE 1X



HYBRID IS EXCELLENT FOR CPU-CENTRIC DESIGNS

OpenGL Validation

- Successfully met project KOs for OpenGL ES 3.x
  - Executed and passed all 14K test cases by Tapeout
  - SW Stack ready for perf/w tuning on day 1
  - 4x faster than Palladium-only

- Seamless worldwide access by developers
- 24-hr coverage on 6 hybrid seats
- 3 geographically dispersed SW teams over 2 months

There can be more than one!
Many hybrid configurations

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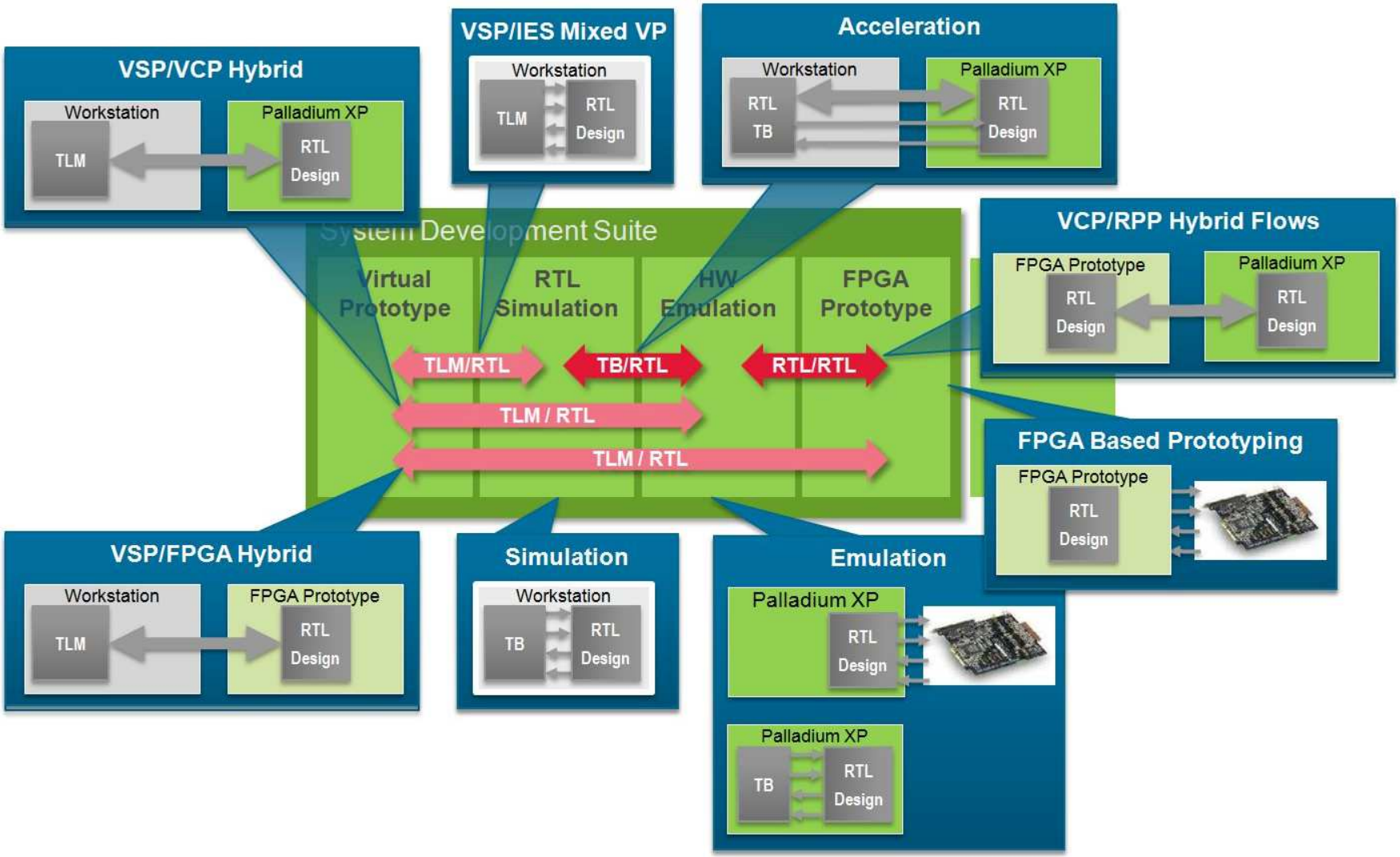
Many hybrid configurations!



Take-aways

- The 90's vision of the "one tool/flow for all" is dead
  - Requires too much modeling
  - There is no "one fits all model/engine"
- Complex projects require many model types
  - Use what you have
- As a result I am willing to bury the dream of a fully articulated golden reference model
  - RTL comes closest today but isn't it either
- Several dynamic engines are needed. Two essential needs:
  - Transfer from engine to engine needs to be as easy as possible
  - Engines need to connect – hybrid configurations!
- TLM – RTL hybrids help OS bring-up and SW development
- There are may different hybrid configurations beyond that!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