Hybrid Virtual Platforms: Are they the highbred Virtual Platforms?

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System view

System
Form Factor
Reference Device

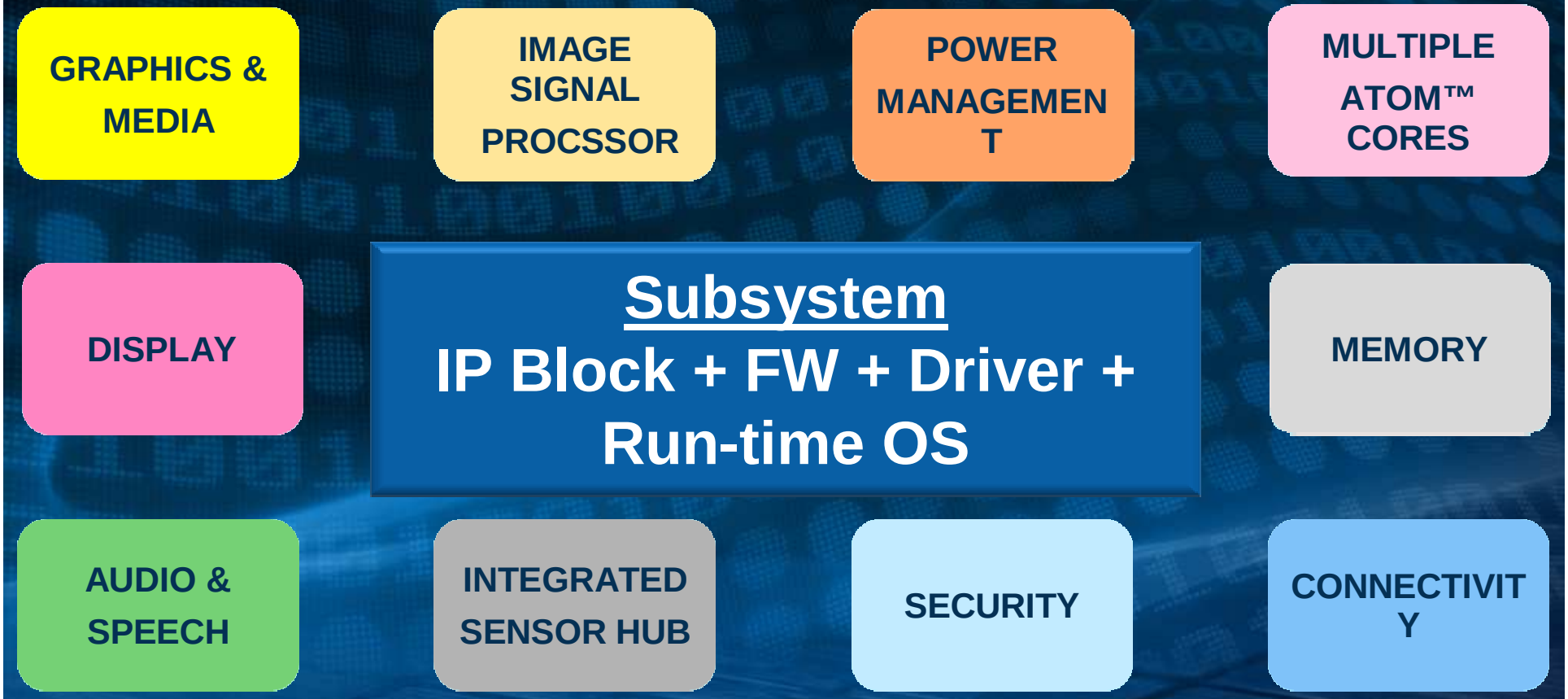
Platform
Board + SoC + SW Stack

SW
- Applications
- OS
- Middleware
- Firmware, Drivers

HW
- Crypto
- Audio
- SoC
- CPU
- Graphics
- Video
- Display
- I/Os
- Sensor Hub
- Connectivity
- Memory

Smart Devices ➔ Complex System

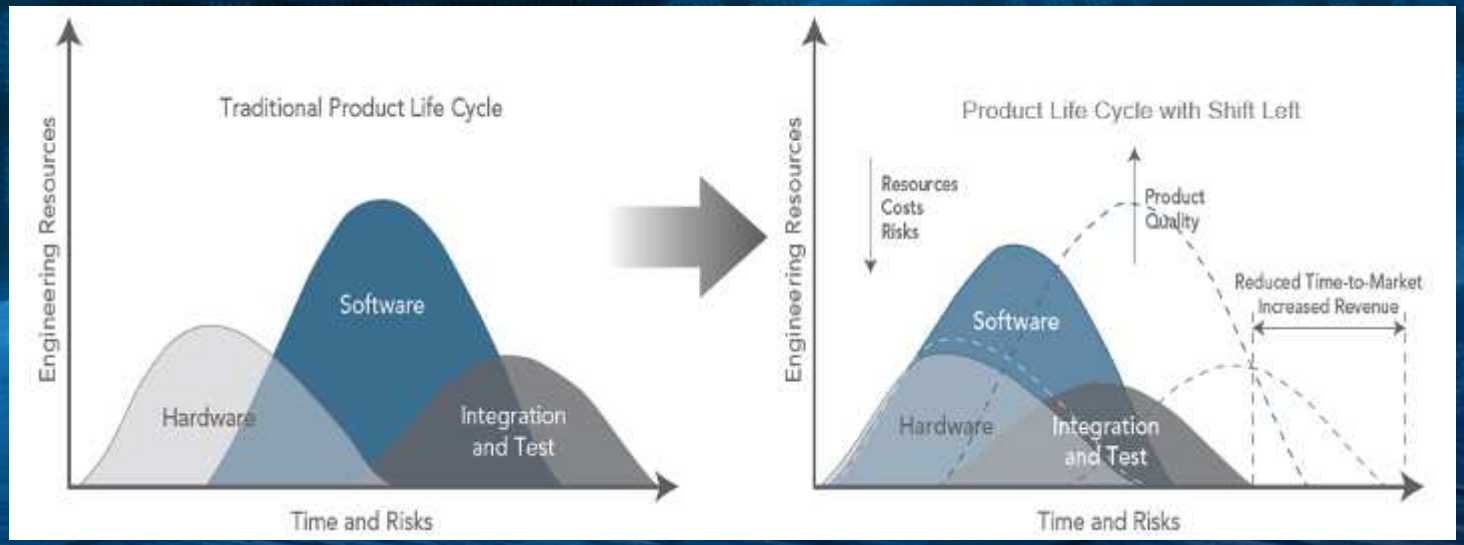
Reality: System of interacting complex Subsystems



Smart Devices ➔ Complex System of Complex Subsystems

Shift Left

Achieving TTM Requires Shift-Left



Tools & Technologies

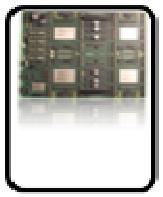
Achieving Shift Left
Requires Better Tools & Methodologies

Tools

Virtual Platform (Soft SoC)

- Benefit: Early development vehicle (no RTL required)

Architectural Exploration | Software Development



FPGA

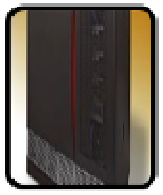
- Benefit: Sub-system level Timing accuracy; RTL health

Software Development | HW-SW Co-Validation

Hybrid VP (VP+FPGA)

- Benefit: SoC & System level VP speed + RTL accuracy

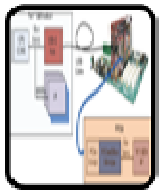
Software Development | HW-SW Co-Validation



SLE / Hybrid SLE

- Benefit: RTL accuracy, RTL debug

Software Development | Post-Si Readiness



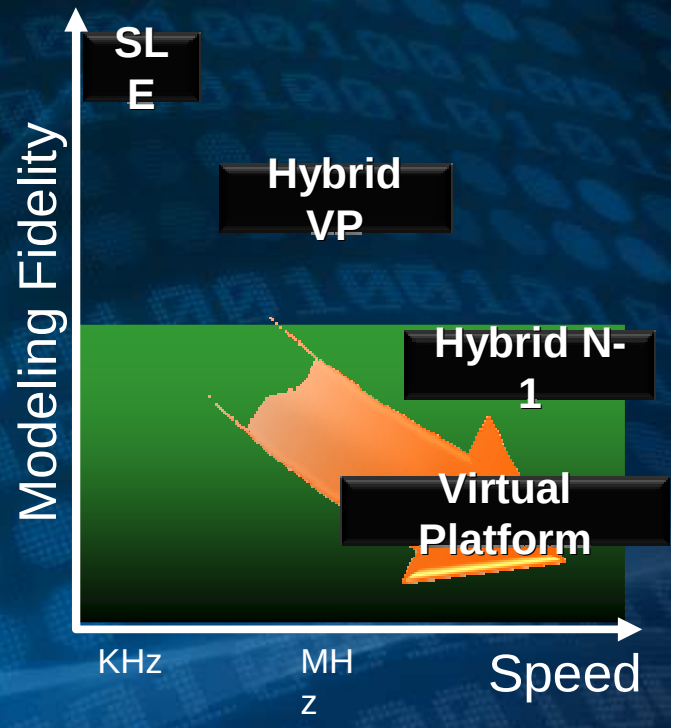
Hybrid Gen N-1 / FPGA

- Benefit: Speed w/real-Si for "good" components & FPGA for new blocks

Software Development | Power & Performance

The need for Hybrid platforms

	VP	Hybrid VP	Hybrid SLE	Hybrid N-1
Ease of Use (SW)				
Ease of Use (HW)				
SW Debug				
HW Debug				
Speed				
Behavioral Modeling Fidelity				
RTL Modeling Fidelity				
Real-world Devices				



No “One-Size Fits All” Solution

Typical Hybrid-FPGA Virtual Platform

North Cluster in VP

GRAPHICS & MEDIA

IMAGE SIGNAL PROCSSOR

DISPLAY

MULTIPLE ATOM™ CORES

IOSF/PCIe

South Cluster in FPGA

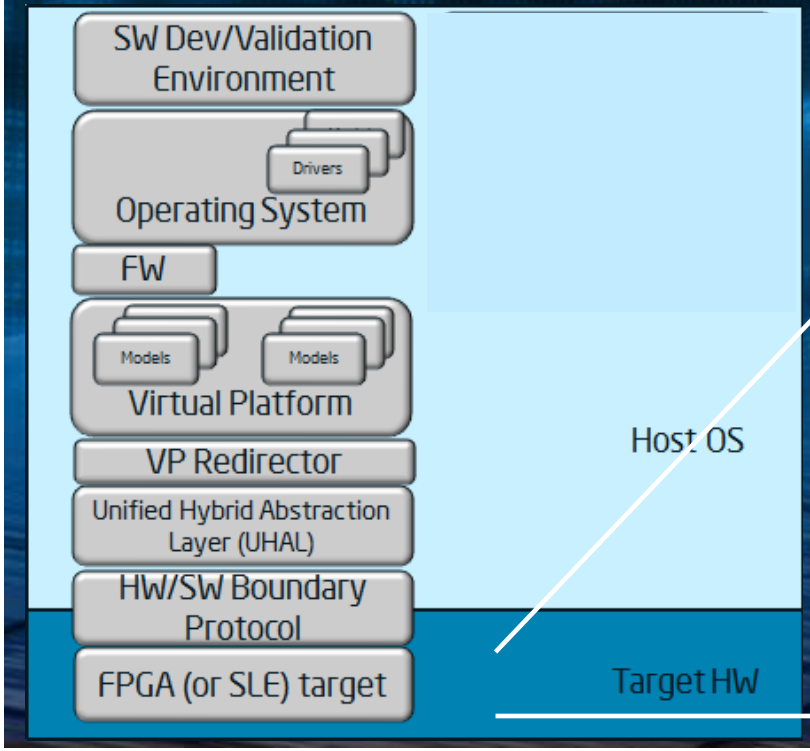
SECURITY

CONNECTIVITY

AUDIO & SPEECH

INTEGRATED SENSOR HUB

I/Os



Key Benefits of Hybrid FPGAs

High speed with select RTL accuracy

Allows re-use RTL vs. build SW models

Mitigates lack of 3rd party VP model (RTL only)

Enables pre-Si systems with @-speed real world devices

Enables true pre-Si HW/SW co-validation

Trustworthy indicator of product health

Hybrids are Highbred indeed!!

Hybrid may fit your needs ….. But

Can You match what Hybrid needs?

Hybrid Challenges

Complex integration of many HW & SW components

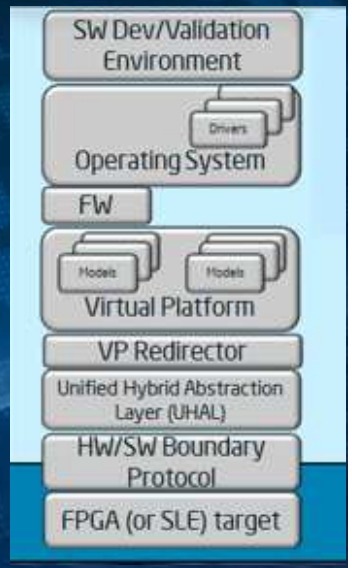
Narrow window of opportunity (after stable RTL)

Multi-team, multi-skill dependency

Cost: FPGA/Emu are expensive

Tooling: FPGA tool chain is still maturing

Velocity: DEBUG!!! Where in the stack is the bug?



Summary

Hybrid Virtual Platforms:
Are they the highbred Virtual Platforms?

Yes they are…

but be prepared for the challenges before you breed them