

## HYBRID PRE-SI PLATFORMS FOR PRODUCTION SOFTWARE READINESS



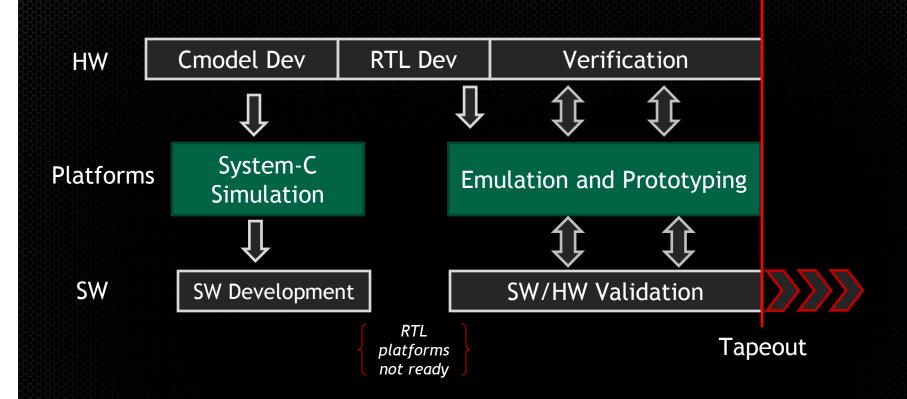
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# Why Hybrid?

### Schedule

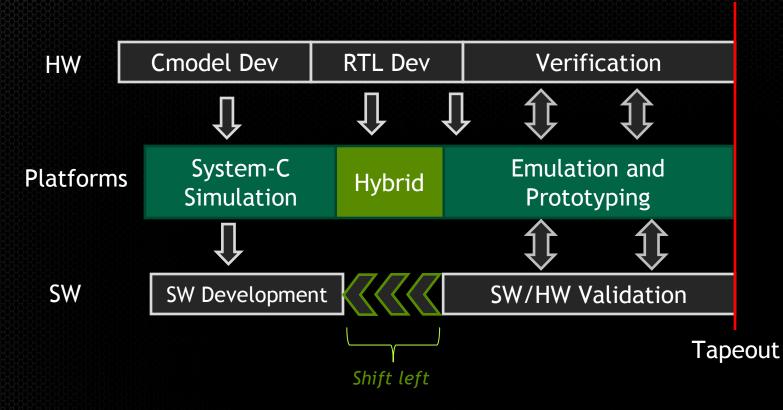
- Get stuff started earlier
- Speed
  - Get stuff done sooner

## **Traditional Pre-Si Flow**



Emulators and FPGAs driven by full-chip RTL schedule
Missed coverage adversely affects SOL production

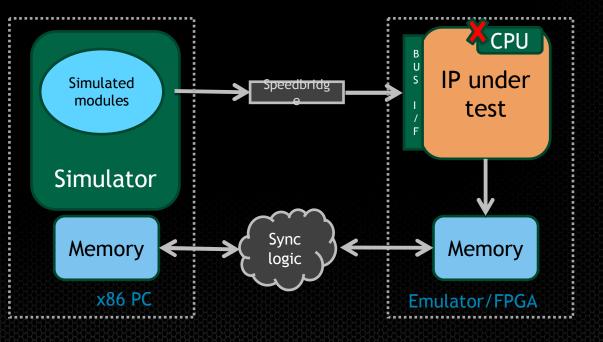
## **Hybrid Pre-Si Flow**



- Hybrid platforms driven by IP RTL schedule
  - Earlier availability
- Substitute IP RTL in system-C simulator
- Finish SW/HW validation in time

## Hybrid Speed Advantage

- Address bottlenecks of traditional full-chip pre-si platforms
  - Emulate mission critical IPs (GPU...)
  - High speed simulation of the rest including CPU
- Boot OS in reasonable wall-clock time



# **NVIDIA Tegra Example**

### Goals

Complete OpenGL based validation by Tapeout

- 14K tests in ~8 weeks
- ~3K hours run-time

#### Boot accelerated UI in reasonable time

• < 1 hr

## Platform solutions explored

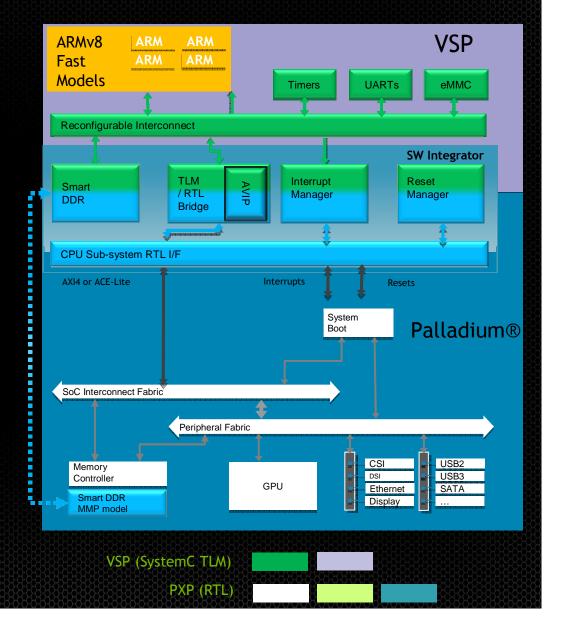
- Palladium emulation
  - UI boot extrapolated to be day(s)
- Custom FPGA platform
  - Complicated RTL partitioning
- Cadence VSP in a hybrid configuration with Palladium



# **Cadence® VSP Hybrid**

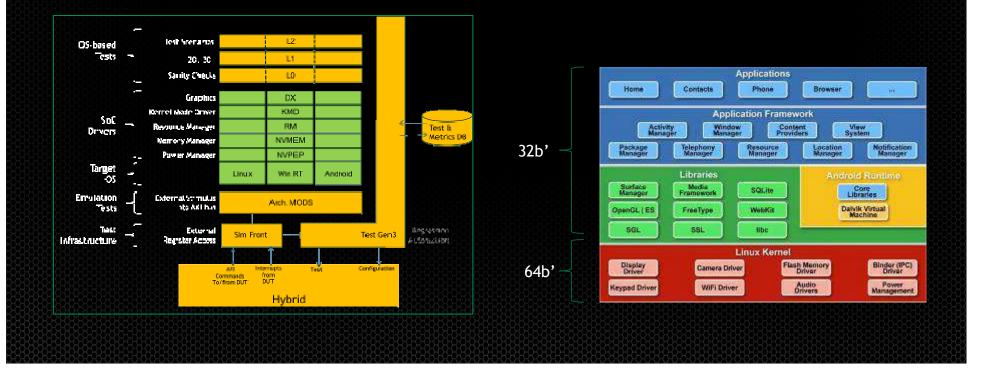
#### Full-chip environment

- OS boot
- Production SW Stack
- Production use cases
- Unified Memory
- Fast access to Palladium emulated memory
  - SmartDDR ®
  - Requires MC tweaks
- Ability to add standard simulation models (TLM2)



## **NVIDIA Tegra Results**

- Used for multiple Tegra SOCs
  - Kernel boot = 2 mins. Android UI = 90 mins
  - 20x faster than traditional emulation
- Met OpenGL Tapeout validation KPI
  - 60% faster than traditional emulation (GPU limited)
- Resolved 32b' user <> 64' kernel interface bugs (Tegra K1/Android K)



# **NVIDIA Tegra Futures**

### SW development and validation on unit IP platforms

- Extend VSP to validate more IPs
- Unit FPGA custom and/or industry standard

### Pre-Si SW perf/w tuning

- Cycle/timing accurate models with system-C Hybrid
- Always-on Pre-Si and Si SW flow
  - Seamless transition between platforms
  - Minimal platform specific SW code

