Multi-Die Packaging – How Ready Are We?

EDPS 2015

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ASE Group
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Agenda

- ASE Brief
- Integration Drivers
- Multi-Chip Packaging
- 2.5D / 3D / SiP / SiM
- Design / Co-Design Challenges: an OSAT Perspective
- Summary

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Brief Backgrounder

- Established 1984, production commenced at flagship factory in Kaohsiung, Taiwan.
- Achieved global market leadership in 2004, surpassing all players in OSAT industry.
- Operations now at 12 facilities worldwide, serving multiple markets, applications, & geographies.
- >50K employees: Global team comprises operations, engineering, R&D, sales, & marketing.
- ASE Group overall revenue of $8.4B in 2014, 14% over 2013. ATM* overall revenue of $5.3B in 2014, 9% over 2013.

ATM*: Assembly, Test, Material

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Integration Drivers

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Value Chain Consolidation

Creating Differentiation

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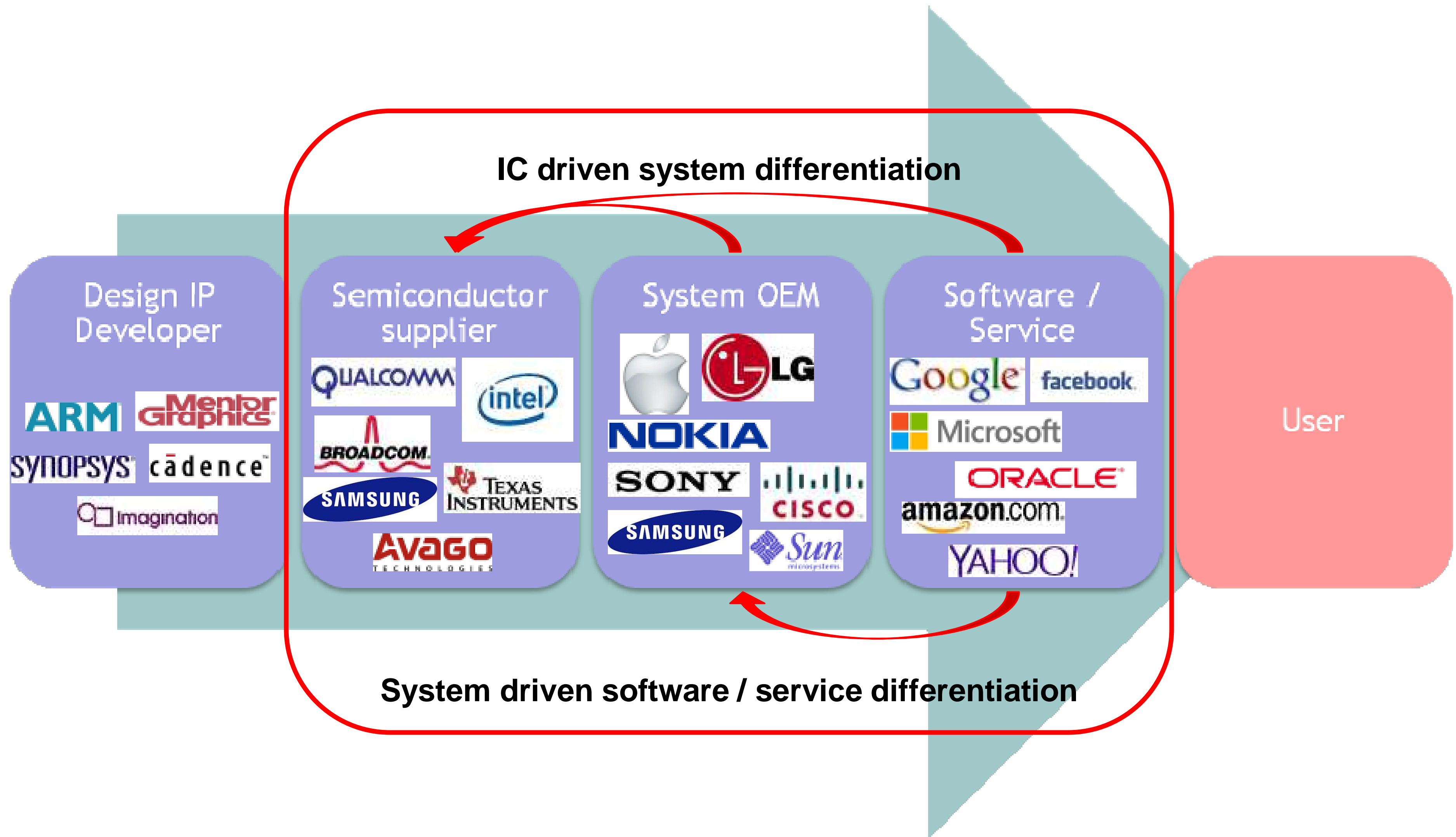

SoC-SiP-SiM Evolution

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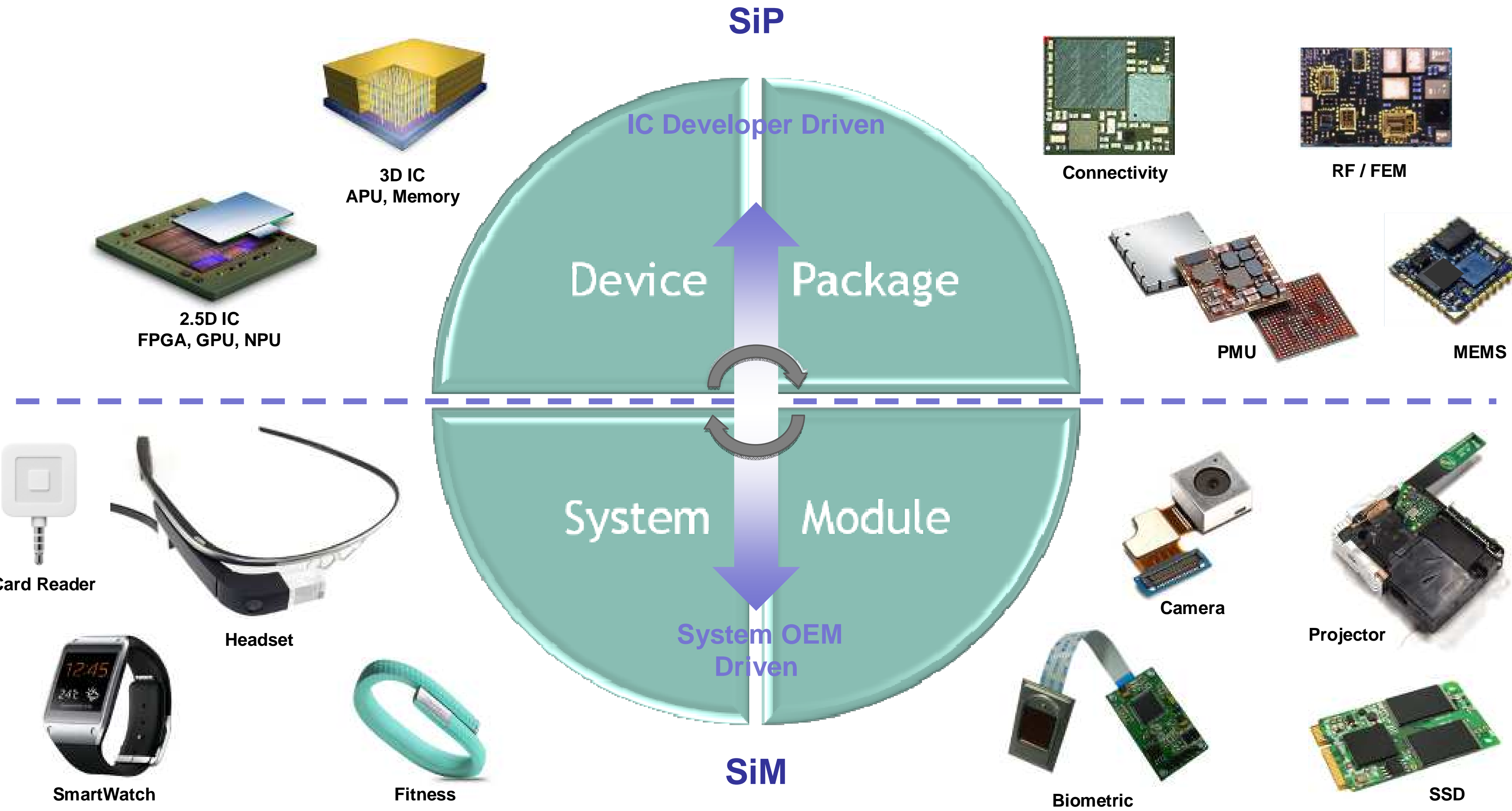

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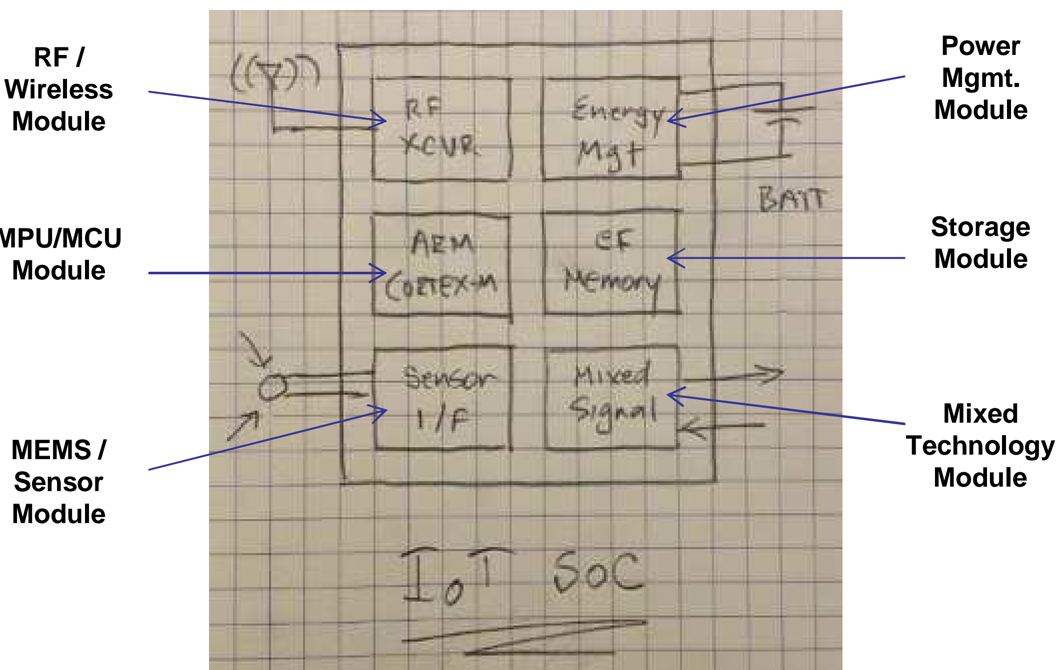
Basic IoT SoC / System



Source: Tyson Tuttle – CEO SiLabs

- Instrumented
  - Able to sense and monitor environment
- Intelligent
  - Capable of analytics
  - Can make decisions based on data
- Interconnected
  - Shares data through cloud
  - Interacts with people and other systems
  - Can remotely monitored and controlled
- Secured
  - Protects data from malware, theft or tampering

- SoC
  - Highly integrated
  - Smallest size / lowest power
  - High cost & long development cycle
  - Limited functional flexibility

VS.

- SiP / SiM
  - Modular – standardized & upgradable
  - Flexibility – application specific
  - Small size / low power
  - Faster time to market & revenue

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Multi Chip Packaging

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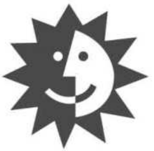
2D & 2.5/3D Packaging Technology



3D

2D

2.5D IC

3D IC

Stacked Die

FC + WB

Laminate Substrate
in BGAs

Build-up Substrate
in FCBGAs

PoP

SOP

QFP

QFN

Leadframe

Side-by-side WB Chips

Side-by-side Flip Chips

1995

2000

2014

Chip

Pkg

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Multi-Dice Loading Trend

- Data covers WB and Flip Chip products

Year	2012				2013				2014			
Quarter	**Q1**	**Q2**	**Q3**	**Q4**	**Q1**	**Q2**	**Q3**	**Q4**	**Q1**	**Q2**	**Q3**	**Q4**
MCM Qty (Mu)	158	156	170	153	127	147	169	154	122	152	173	183
Non MCM Qty (Mu)	820	963	937	784	722	874	882	869	929	1,071	1,142	1,064
MCM %	16%	14%	15%	16%	15%	14%	16%	15%	12%	12%	13%	15%
Non MCM %	84%	86%	85%	84%	85%	86%	84%	85%	88%	88%	87%	85%
TTL Qty (Mu)	**978**	**1,119**	**1,107**	**937**	**849**	**1,021**	**1,051**	**1,024**	**1,051**	**1,223**	**1,316**	**1,248**

Shipping QTY (Mu)

1,400
1,200
1,000
800
600
400
200
-

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

Q1 Q2 Q3 Q4 (2012) · Q1 Q2 Q3 Q4 (2013) · Q1 Q2 Q3 Q4 (2014)

Non MCM Qty (Mu) · MCM Qty (Mu) · MCM % · Non MCM %

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Yield Status

- Incoming Die
  - Standard inspections, same as single die
  - Probed before assembly
- Assembly
  - 2 Dice : >= 99.9%
  - > 2 Dice : >= 99.5%
  - Wirebond, Flip Chip, and combination of both
  - "Mature" subordinate die are commonplace
- Final Test
  - Most customers are doing FT with BIST
  - Typical Yields : > 98.5%
  - Very few customers do full functional testing on memory after assembly

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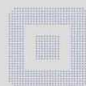

2.5D / 3D / SiP / SiM

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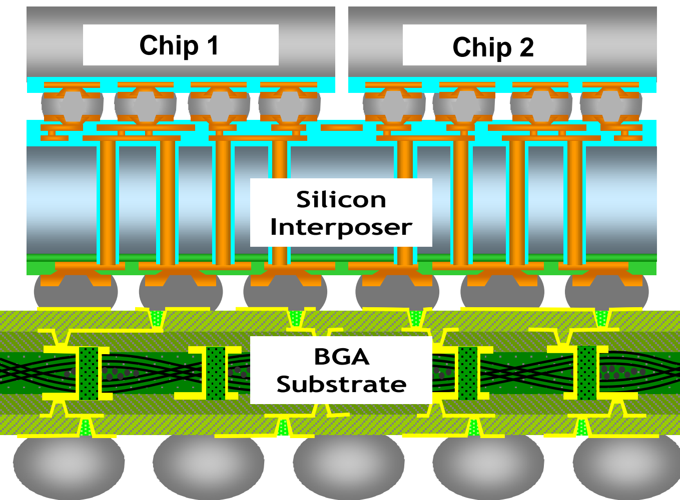
2.5D IC Ecosystem Models



- Foundry IC → Interposer fab → OSAT MEOL+ASSY
- Foundry IC + Interposer → OSAT MEOL+ASSY
- Foundry IC → Interposer fab → OSAT ASSY
- Foundry IC + Interposer w/MEOL → OSAT ASSY
- IDM / Foundry Captive Turnkey
- <u>MOST OR ALL FLOWS WILL LIKELY DEPLOY</u>

Logic IC

Interposer Fab with via formation → MEOL → CoW / CoC Assembly → Final Test

Memory

Analog

Sensors

All components specified by product owner

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Industry 2.5D / 3D IC Manufacturing Readiness

Product Type		Criteria	300 mm Wafer Readiness		
			Y2009	Y2012	Y2014
Wafer Thinning / Grinding		50 µm			
Via Last	Via Etching	20 ~ 50 µm, AR 10			
	Via Isolation	20 ~ 50 µm, AR 10			
	Via Seedlayer	20 ~ 50 µm, AR 10			
Via First	Via Etching	5 ~ 10 µm, AR 10			
	Via Isolation	5 ~ 10 µm, AR 10			
	Via Seedlayer	5 ~ 10 µm, AR 10			
Thin Wafer Handling		50 µm		With Carrier	
Via Surface Finish		No Cu Dishing			
Re-distribution (Double Sides)		-			
Micro-bumping		30 µm Pitch			
TSV Wafer Probing & Testing		30 µm Pitch		50 um Now	
Wafer Singulation		-			
CtW/CtS Bonding		Solder / Micro Bump		TCB	Reflow
Assembly		-			
Final Test		-			

Ready for Mass Production
Ready for Qualification

Ready for Prototyping
No Solution Yet

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2.5/3D IC Test Challenges

- **Wafer Probing**
  - Thinned wafer handling
    - Grinding before/after test
    - Assembly flow vs. Test
  - TSV test
    - TSV defect
    - Double-sided wafer probing?
  - Die/wafer contact interface material
    - Bond pads/ micro bumps/ TSV
    - Cu pillars
  - Contact force of high I/O number vs wafer thickness
    - Probe Force
    - Probe material
  - Fine Pitch
    - Area array pitch < 50um
    - > 1000 contacts

Fundamental Study Capability Is Required for Assembly and Test Subcontractors

- **Package Test**
  - Heterogeneous cores

    Logic + analog + memory
    Embedded passive
    Embedded die
    Assembly and test process flow integration
  - Test Methodologies

    KGD fault coverage
    New fault types
    DFT
    System Level test
  - Cost of test

    One insertion/multi insertions
    ATE or Customized Bench

Joint Development among IC Design/ Foundry/ Assembly & Test companies

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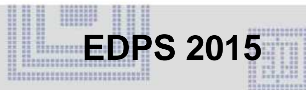

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Design and Co-Design: an OSAT Perspective

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3D IC Concurrent Package & System Modeling & Validation

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Electrical Optimization

TSV Interconnect

R, L, C, S-para, SI/PI

Optimum Design

Memory

Processor

ASIC

Passives

Thermal Optimization

High Power Density

Stress/ DFM/ Reliability Optimization

Chip

Substrate

Maximum Stress

Bump Crack

Inter-delamination

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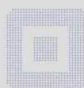

Summary

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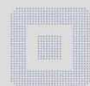
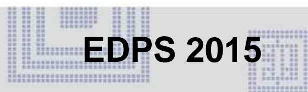
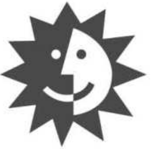



Summary



- Industry drive towards functional integration is at an all time high
- Multi chip packaging has been practiced in large volume, but simpler formats
- SiP, as well as 2.5/3D products, bring a heightened level of complication related to physical interconnect, cost, and business models to produce them.
- Modeling and simulation must be enhanced to enable 2.5/3D products due to sub-system and system level performance requirements

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