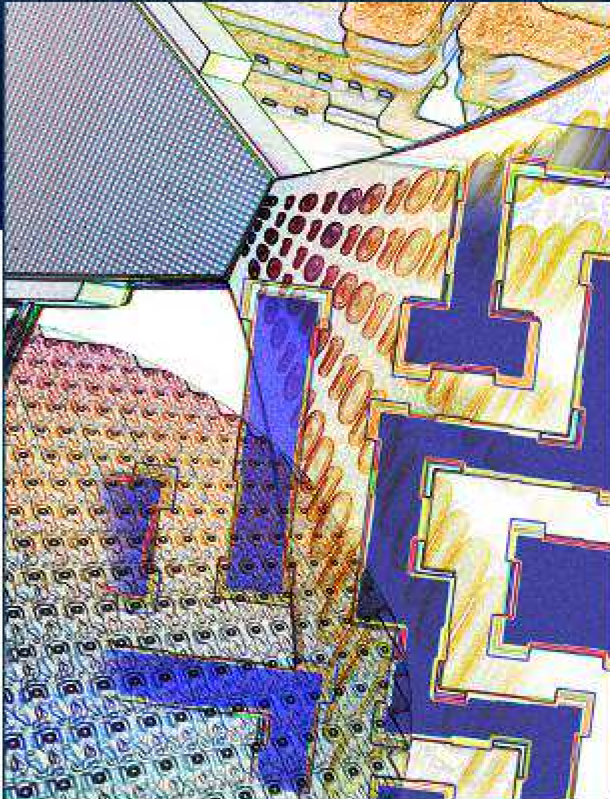
Verification and Extraction of 3D Stack Component Interactions



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Outline

- EDA Challenges in 3D Stack Modeling and Design
  - Different phenomena: electrical, thermal , mechanical
  - Cross- domain integration
- 3D Stack Verification and Extraction
  - Stack verification flow
  - Extraction solutions
- Intra Die Component Interactions and Extraction
  - TSV to TSV
  - TSV to RDL
- Inter Die Interactions
  - Various bonding schemes
  - Analysis of die-to-die capacitive coupling impact
  - In context extraction

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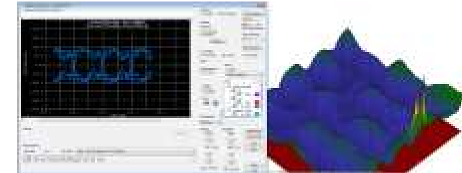
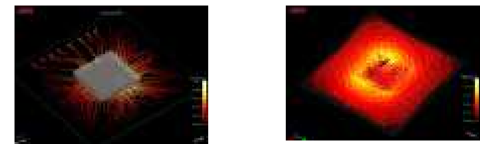
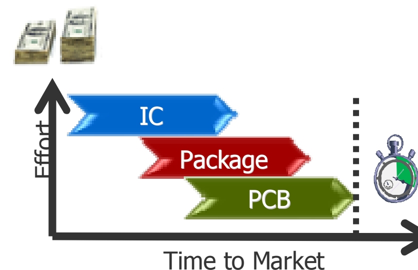
EDA Challenges in Modeling and Design of 3D Stacks

- **Modeling**
  - Different phenomena: electrical, thermal, mechanicals;
  - Interaction modeling
  - Tradeoff between needed accuracy and model complexity and flow integration
  - Consistency between different levels of abstraction

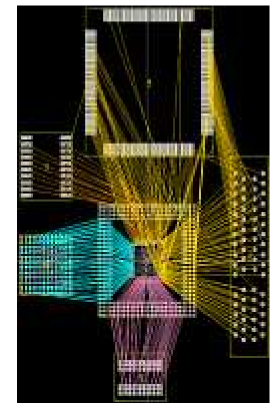




- **Design**
  - Design exploration/optimization tools, managing interactions and controlling parametric yield
  - Cross-domain integration
    - ICs, Interposer, Package , Board



  - Work on resolving issues related to multiple disconnected tools with no standard methodology/flow to synchronize and transfer design data between design disciplines and abstraction levels



  - Standards needed for tool interfaces and data exchange format

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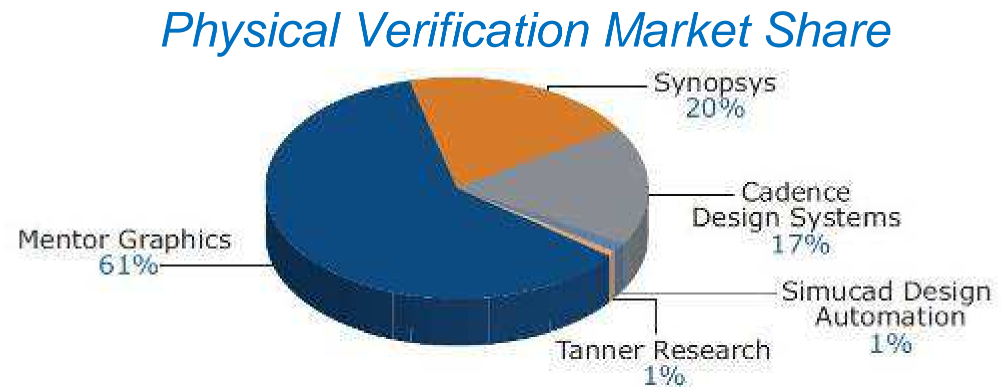
Expanding Calibre to the 3DIC Domain

- Calibre is the dominant sign-off tool for leading IDM, memory, fabless and foundries
  — Lowest Risk
  — Fastest Performance



- Expanding Calibre for 3DIC Verification & Analysis
  — Physical Verification
  — Parasitic Extraction
  — Thermal Analysis
  — Stress Analysis

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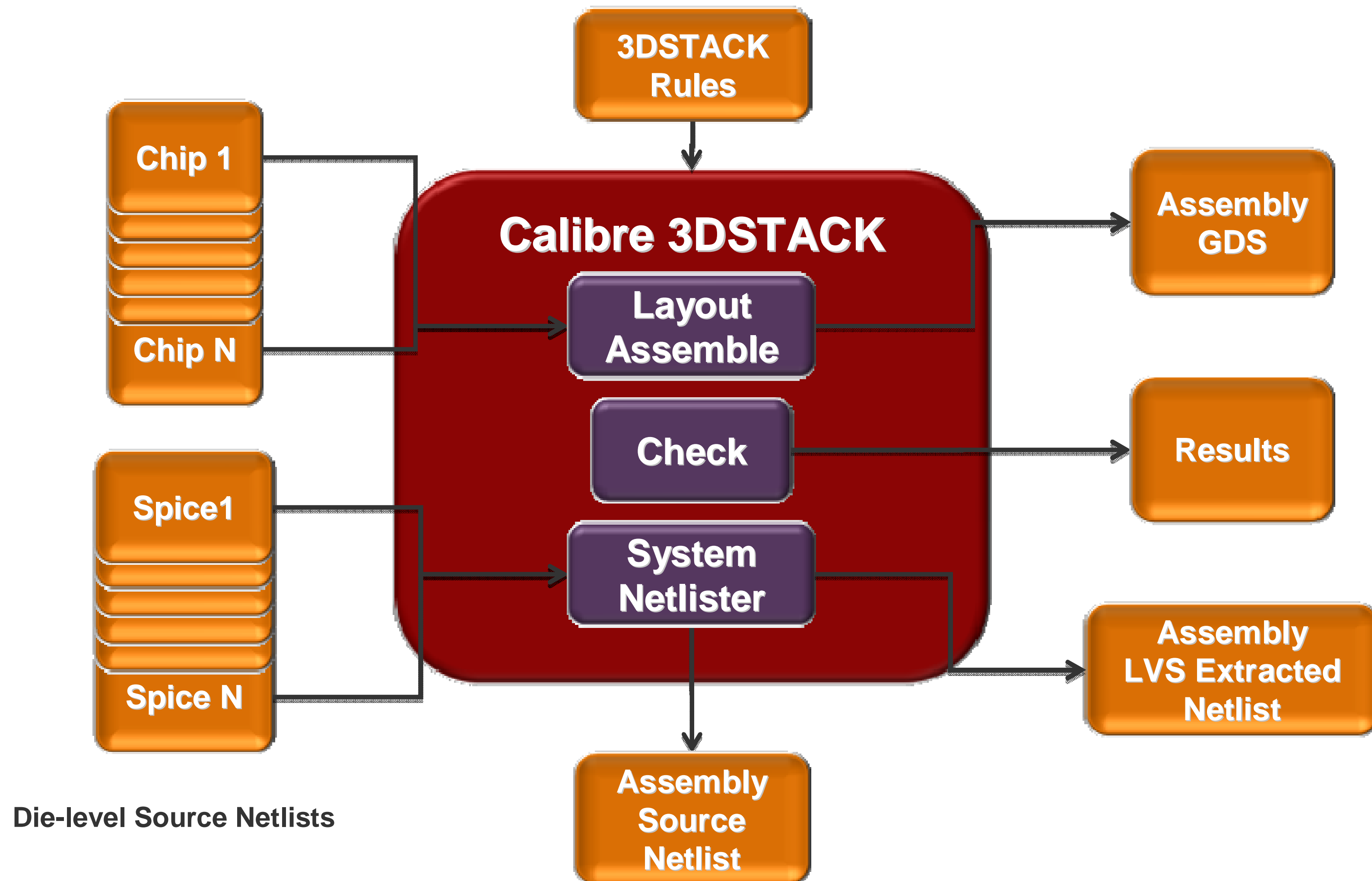
Calibre 3DSTACK: Verification Flow



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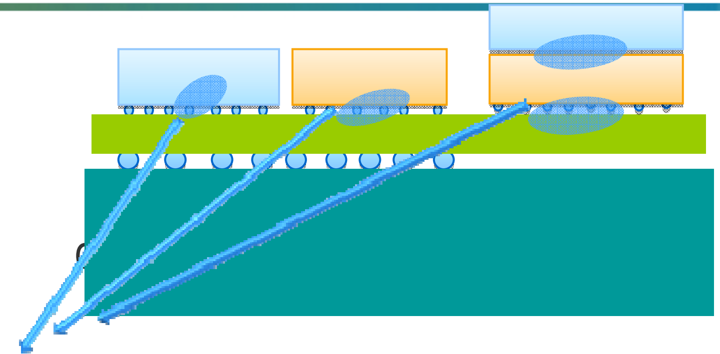
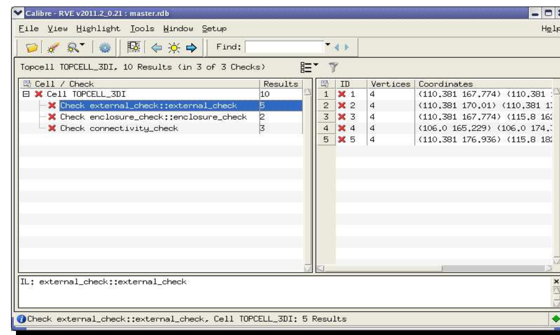
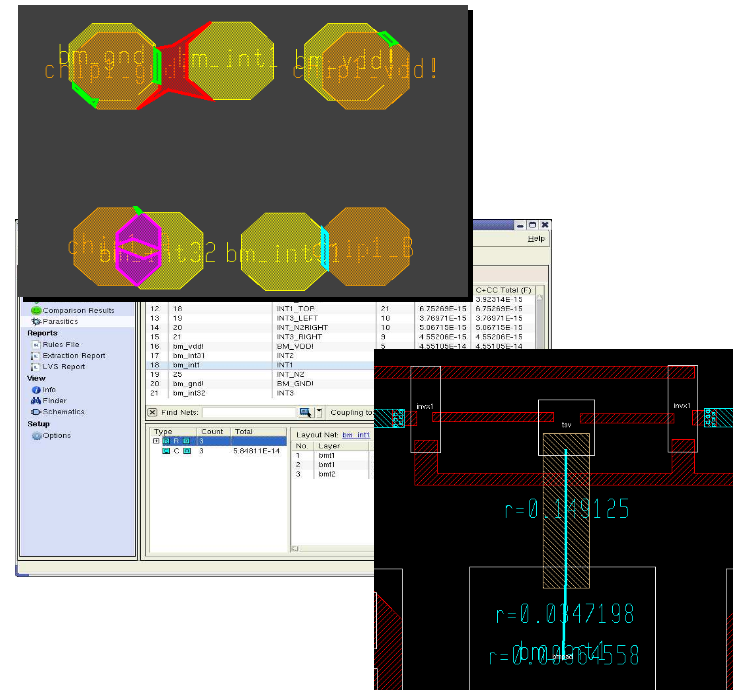
MG Stack Verification Flow



Calibre 3DSTACK

- Verify with micro-bumps are physically aligned
- Verify proper electrical connectivity through interfaces





Calibre xRC/xACT3D

- Extract parasitics of the Dies and Interposer interconnect
- Insert provided TSV circuit into integrated parasitics/TSV netlists, or extract TSV

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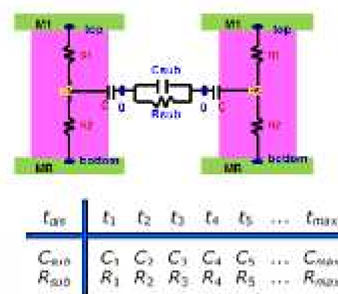
Extraction solutions: TSV Modeling Approaches

- **Stand Alone TSV models**
  - Advantage: Easy to integrate into a flow ; Sufficient in many situations
  - Challenges: Not adequate for high density, high frequency applications

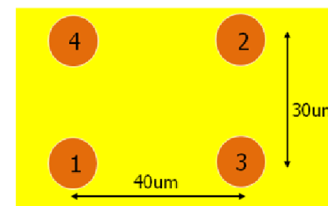
- **Compact parametrized models**
  - Advantage: Can account for some interactions; Faster than FS
  - Challenges :Hard to account for all situations, to parameterize for all important variables

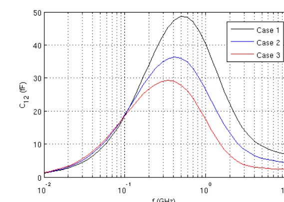


Case 1: TSV 3 and TSV 4 are not present in layout

Case 2: TSV 4 is not present in layout

Case 3: All 4 of the TSV's are present





- **Field solver approach**
  - Advantage: Most accurate
  - Challenges: Performance; Integration

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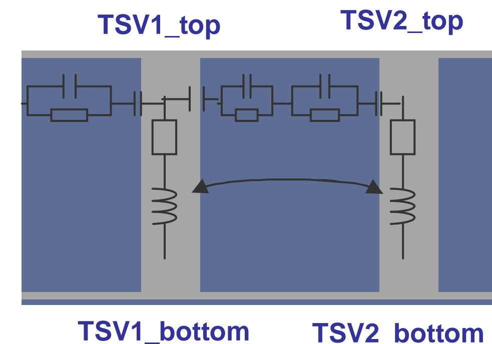
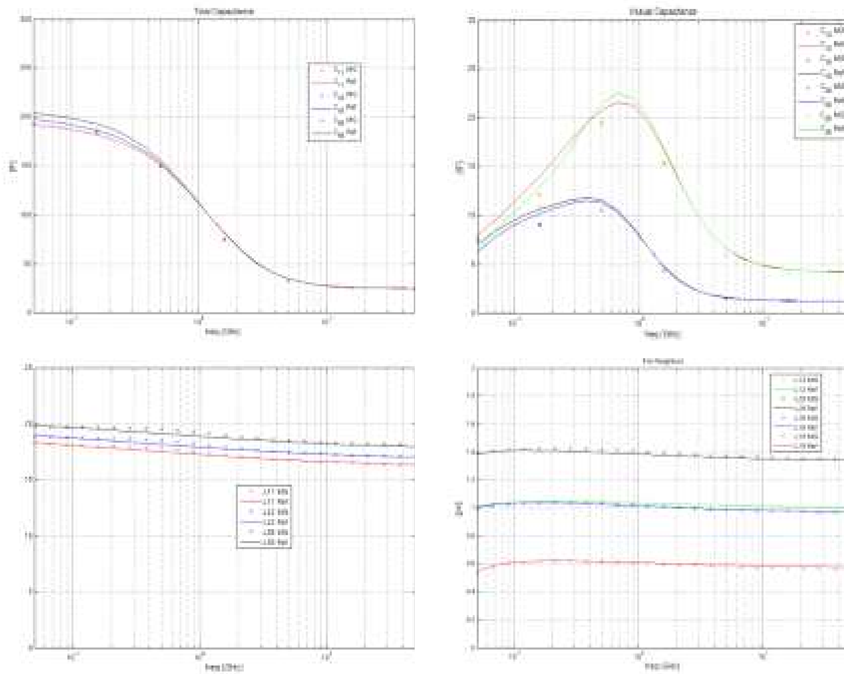
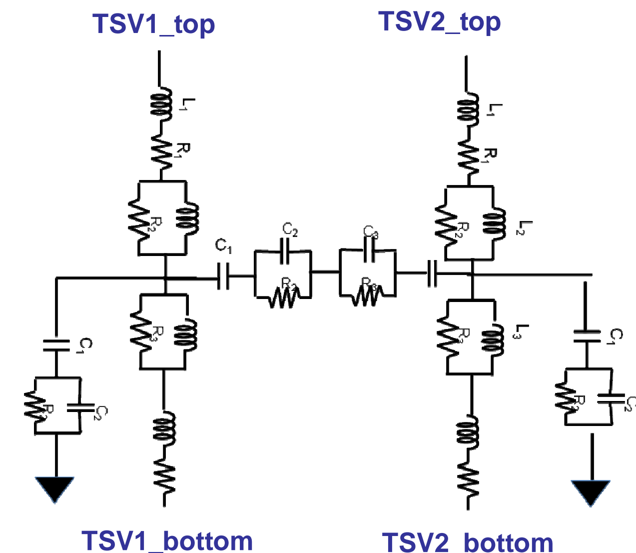
Fast Field Solver Based Solution

- Fast-Field Solver based solution extracts TSV parasitics and TSV to TSV couplings (capacitive and inductive)
  - Produces netlist consisting of frequency-independent linear elements.
  - Accurate vs. reference results
  - Order of magnitude faster than other field solvers







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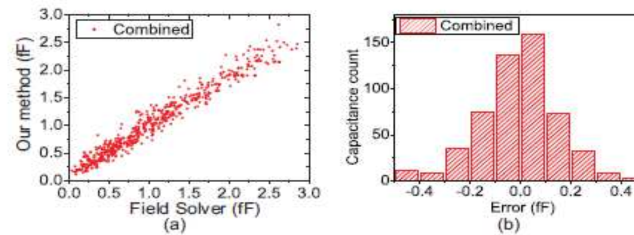
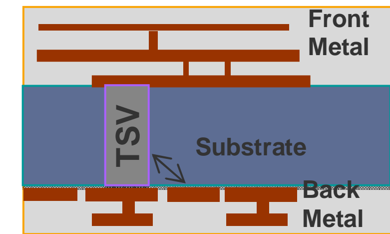
Extraction of TSV to Interconnect coupling

- Model and extract TSV to interconnect extraction
- Full chip solution within 2% accuracy vs FS





- Significant impact:

TABLE I
TSV-TO-WIRE COUPLING FULL-CHIP IMPACT.

Is TSV-to-wire included?	no	yes
Longest path delay (ns)	4.48	5.08 (+13.4%)
Total power on TSV net (mW)	0.303	0.356 (+17.6%)
Total net switching power (mW)	2.42	2.50 (+3.3%)
Total noise on TSV net (V)	32.5	78.2 (+104%)

- To Reduce the impact

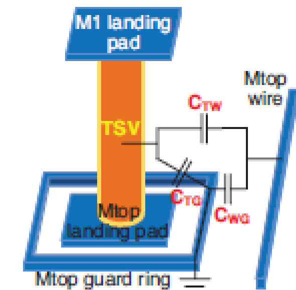


Table 6: Keep-out-zone impact on full-chip design. Power i reported in mW.

KOZ size (μm)	0.5	2.5	5
Longest path delay (ns)	5.08	4.95 (-2.6%)	4.77 (-6.1%)
Total power on TSV net	0.356	0.342 (-3.9%)	0.327 (-8.1%)
Total net switching power	2.50	2.47 (-1.2%)	2.45 (-2.0%)
Total noise on TSV net (V)	78.2	67.0 (-14.3%)	42.9 (-45.1%)

Table 7: Guard ring impact on full-chip design with 2.5μm KOZ. Power is reported in mW.

Guard ring width (μm)	0	0.5	1.5
Longest path delay (ns)	4.95	4.98 (+0.6%)	5.01 (-1.2%)
Total power on TSV net	0.342	0.351 (+2.6%)	0.358 (+4.7%)
Total net switching power	2.47	2.475 (+0.2%)	2.479 (+0.4%)
Total noise on TSV net (V)	67.0	58.0 (-13.4%)	53.6 (-20.0%)

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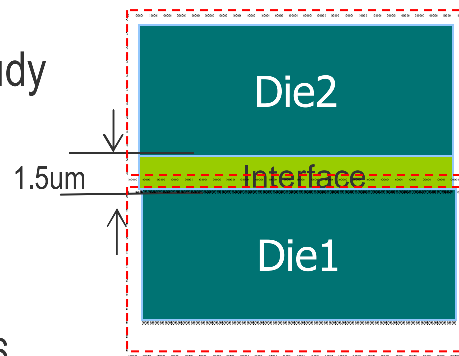
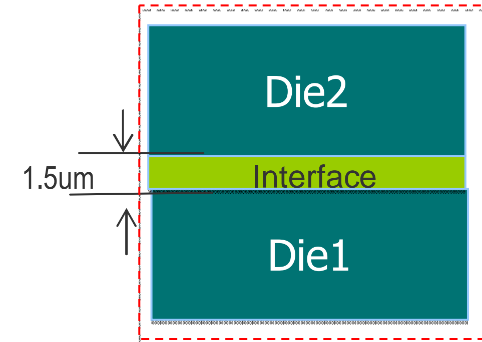
Inter die parasitic extraction in F2F bonding

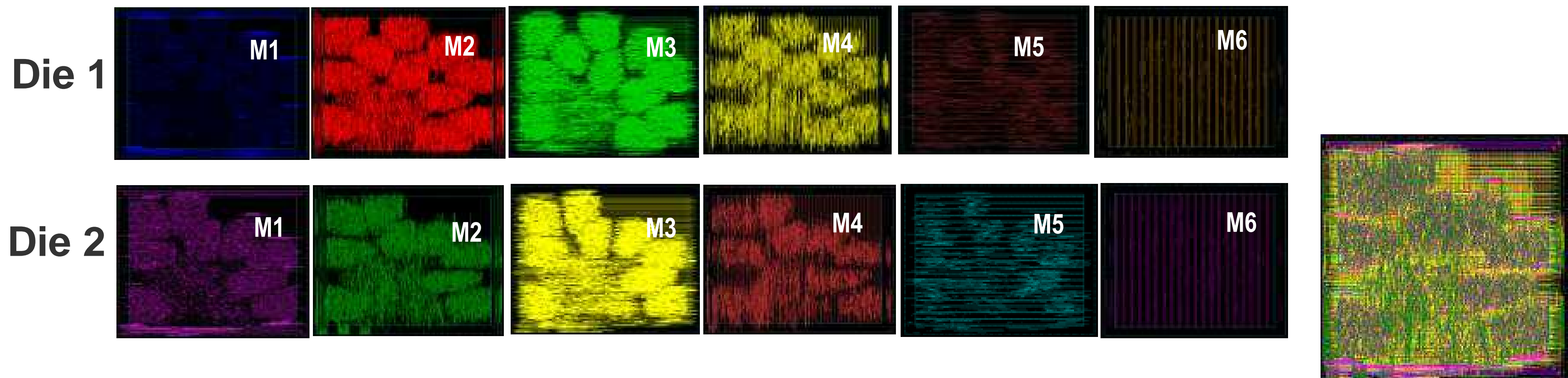
- Two different scenarios for LVS/PEX to study impact of die-to die coupling capacitance
- Dies are connected F2F
- Each die has 6 metal layers
- w/s varies from 0.05/0.05u for M1 to 0.36/036 (M5) and 1.8/1.8u (M6)
- Distance between the dies varied from 10u-1u



Individual die LVS/PEX
Parasitics extracted separately
Ignoring intra-die coupling



3D stack LVS/PEX
Extracting interface and die coupling parasitics



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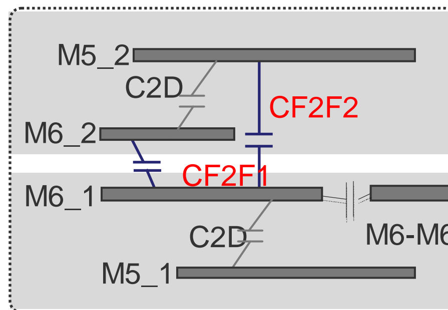
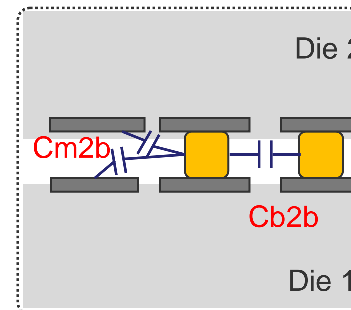
Impact of die capacitive coupling

Impact on various capacitance components





- Impact of charge sharing on top metal coupling capacitance in the same die (M6-M6):

  overestimated by >50% when the dies get close to 1 micron
- No impact (<1%) on lower layer capacitances M5-M5
- Die to die coupling (CF2F1, CF2F2) becomes comparable to intra die coupling (M6-M6)

Impact on full chip noise and critical path delay

- Significant delay impact on individual nets 10%-20% , depending on the design type
- Significant impact on noise voltage , up to 80%
- No impact on power

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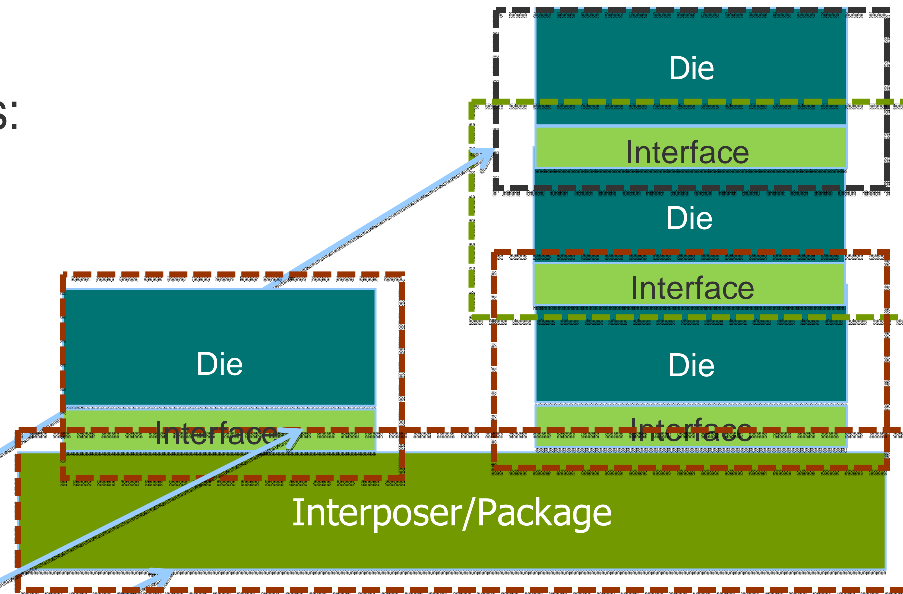
In Context Calibration/Extraction

Inter die and die to interposer interactions:

- Interface extraction
- Capacitive coupling



Describe geometry and materials for inter-die region

Die –to die

Die –to- interposer

Die(or interposer) to package

- Each die would be calibrated/extracted in-context
- Coupling capacitances would be folded in the victim die parasitics
- Interfaces will be owned by the specified dies

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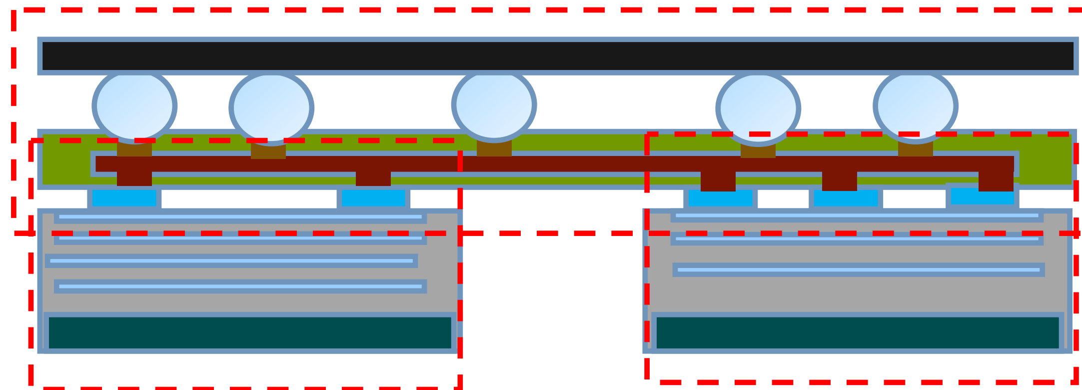
InFO WLP extraction example

- Extract the dies “in context”
- Do not netlist couplings; Fold them into top level capacitances
- Extract the package “in context” with the ground assumed at the board level
- Stitch the netlists



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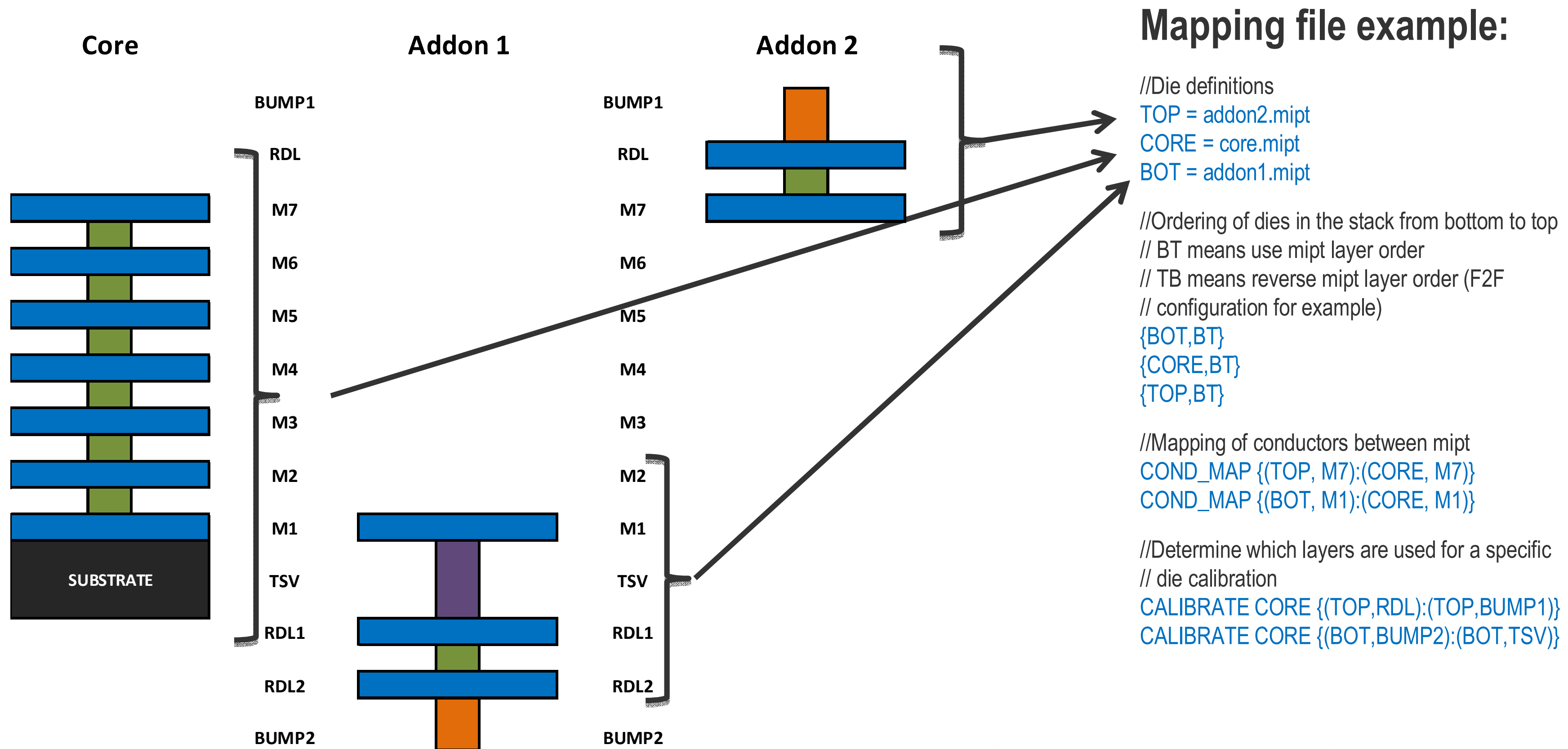
Incremental calibration

- The same die can be put in different environments
- The extraction rules already exist for different metal stacks
- To avoid a need for creating new rule decks incremental calibration can be used



Mapping file example:

//Die definitions
TOP = addon2.mipt
CORE = core.mipt
BOT = addon1.mipt

//Ordering of dies in the stack from bottom to top
// BT means use mipt layer order
// TB means reverse mipt layer order (F2F
// configuration for example)
{BOT,BT}
{CORE,BT}
{TOP,BT}

//Mapping of conductors between mipt
COND_MAP {(TOP, M7):(CORE, M7)}
COND_MAP {(BOT, M1):(CORE, M1)}

//Determine which layers are used for a specific
// die calibration
CALIBRATE CORE {(TOP,RDL):(TOP,BUMP1)}
CALIBRATE CORE {(BOT,BUMP2):(BOT,TSV)}

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