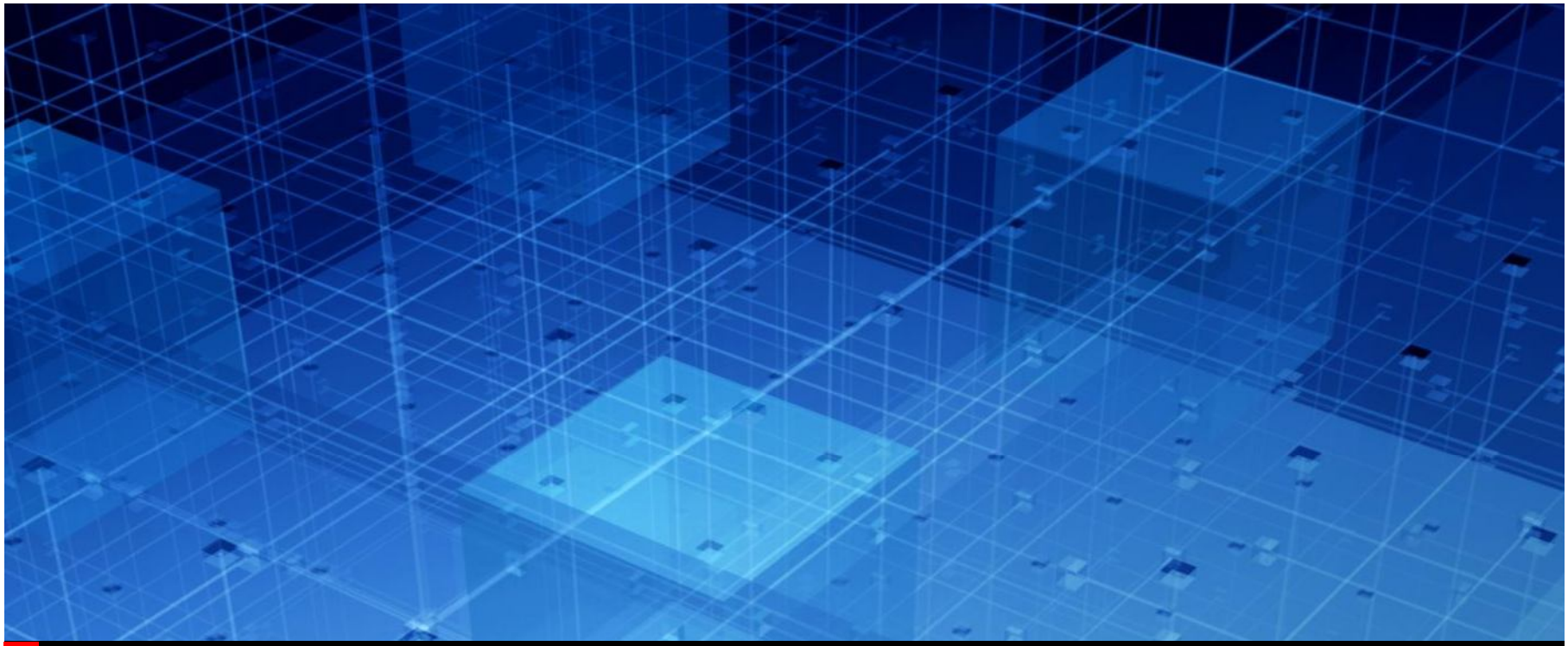

3D-IC Designs for Power, Performance, and Cost

Brandon Wang
Group Director, Strategic Program at Cadence
04-23-2015

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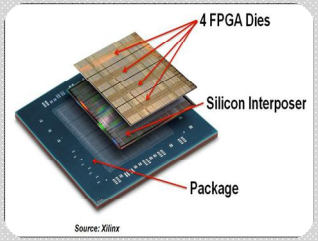
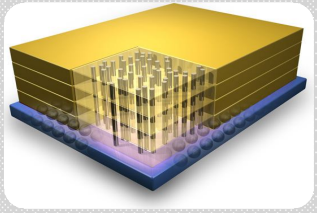
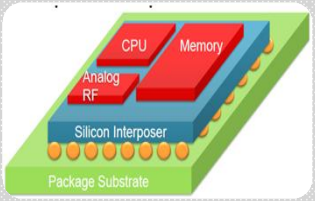
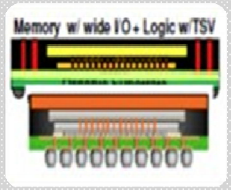
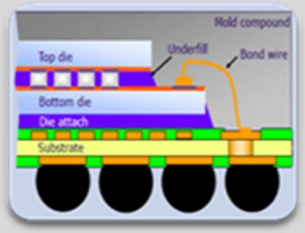
Short-, medium-, and long-term path to 3D-IC











Si Partitioning with TSV Interposer

- Market : FPGA
- **Xilinx in 2010**
- **2011-2013**

Memory Cube with TSVs

- MARKET : Server and computing
- **IBM and Micron**
- **2012-2014**

Logic + memory w/ 2.5D TSV Interposer

- MARKET : Server, Telecom, datacom, gaming
- **Huawei/Hi-Silicon**
- **2013-2014**

Memory + Logic with TSVs

- MARKET : HP mobile/tablet, gaming processors, HPC
- **2015-2016**

Heterogeneous Integration w/o TSV

MARKET : IoT devices, wearable, Automobile

- **~ 2015**

Standards, ecosystem, cost

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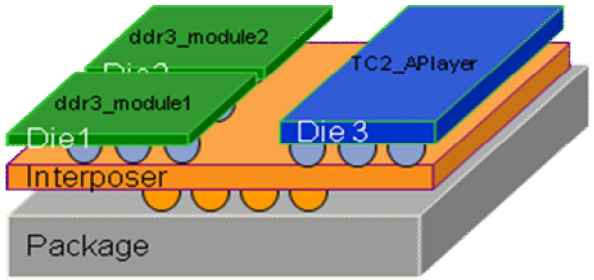
2.5D Silicon Interposer for Performance Driven Applications

- Interposer enables high performance/high bandwidth applications through massive interconnects among dies, particularly logic dies and memory dies;
- TSVs in SI Interposer die provide shorter routes for high speed signals, and deliver adequate power/ground connections to both logic and memory dies;
- Metal mesh and MiM Cap in Silicon interposer further enhance the performance through better SI and PI
- Silicon interposer as better heat conductor for improved thermal dissipation for higher performance



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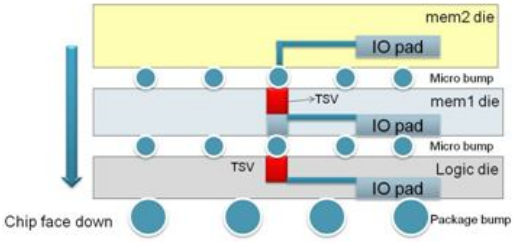
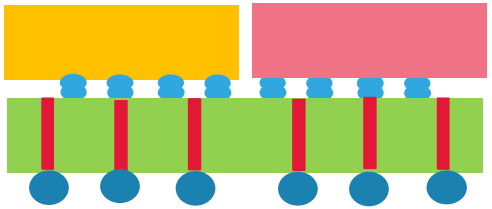
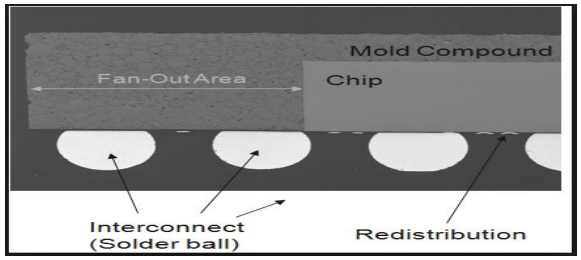
3D Stack and/or Monolithic 3D for lower cost

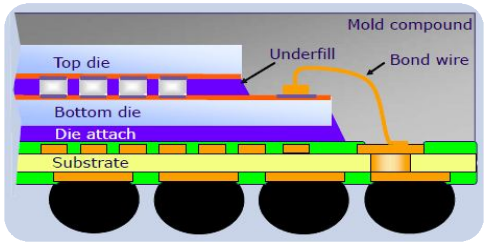
- No additional SI Interposer cost



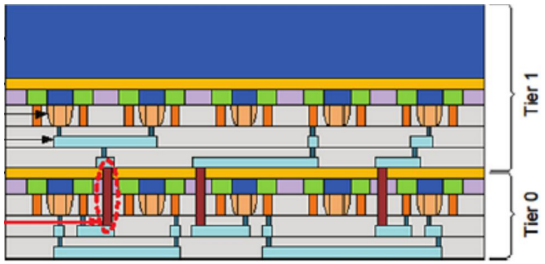
- TSV-Less Integration
  - No wafer thinning, less yield loss
  - Face2face uBump connection for multi-die stack
  - Integrated Fan out WLP







- Monolithic 3D-IC



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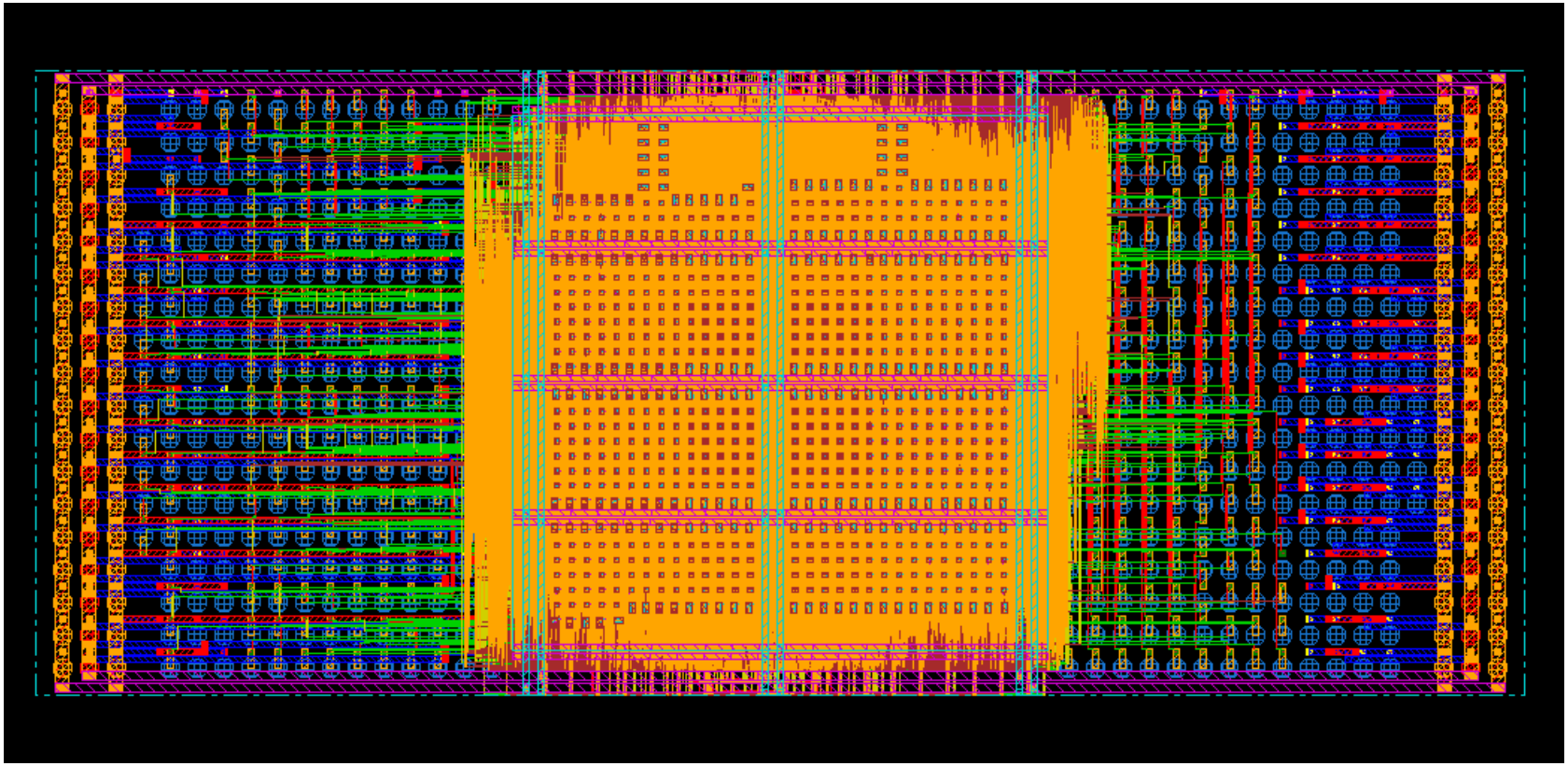
3D-IC using uBumps for inter-die P&R Optimization using EDI/Innovus



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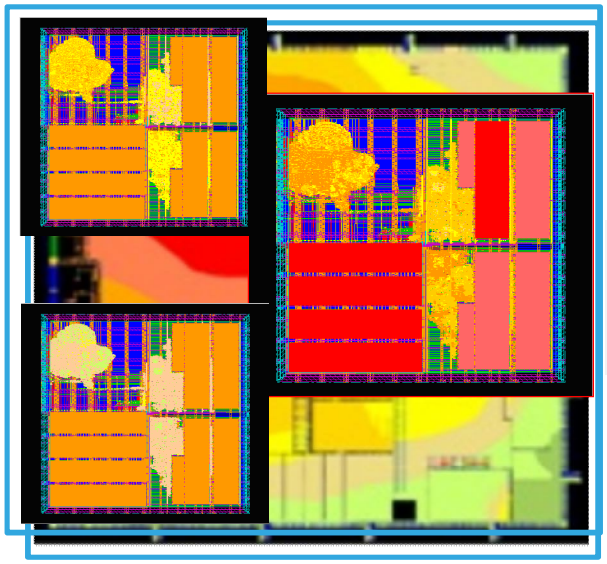
Multi-Dies-package-board thermal co-simulation

Voltus

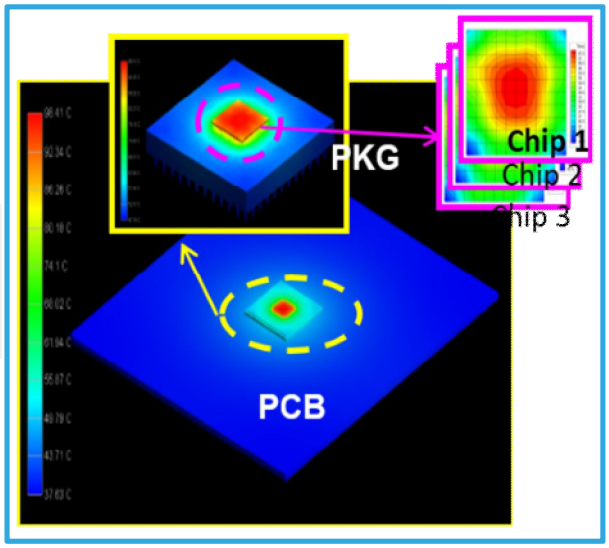
Sigrity PowerDC



Temperature Map
Package Model

Model Connection Protocol (MCP) – Connectivity map from die to package to board

Power Map
Die Model



Power Map

Temperature Map

- **Sigrity PowerDC computes Temperature map including multiple dies, package and board**
- **Voltus computes temperature dependent Power map of each die (leakage, dynamic)**
- **Iterate co-simulation until results converge (equilibrium, transit)**

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Summary

- Different 3D-IC integration technologies are needed for high performance centric, or low cost applications;
- All 3D-IC integration technologies, whether high performance, or lower cost, will reduce system power consumption;
- IoT, Wearable in consumer applications will drive the TSV less 3D integration technologies such as InFO WLP to mass production;
- Monolithic 3D integration will both bring even higher performance and lower power in smaller form factor in near future;
- Implementation method varies for different 3D integration technologies, but electrical and thermal co-analysis are commonly required at die-package at plan/design phases.

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