Session 2: Multi-Die Design Challenges and Applications

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EDPS 2015 in Monterey, CA, April 23

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The 3D IC EcoSystem Today and What's Next

Herb Reiter

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EDPS 2015 in Monterey, CA, April 23

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Agenda

1. Introductions
2. Multi-Die Applications
3. Die-Package CO-Design
   incl. Assembly Design Kit (ADK)
4. Other EDA Challenges
5. What's Next
6. Summary
7. Q & A

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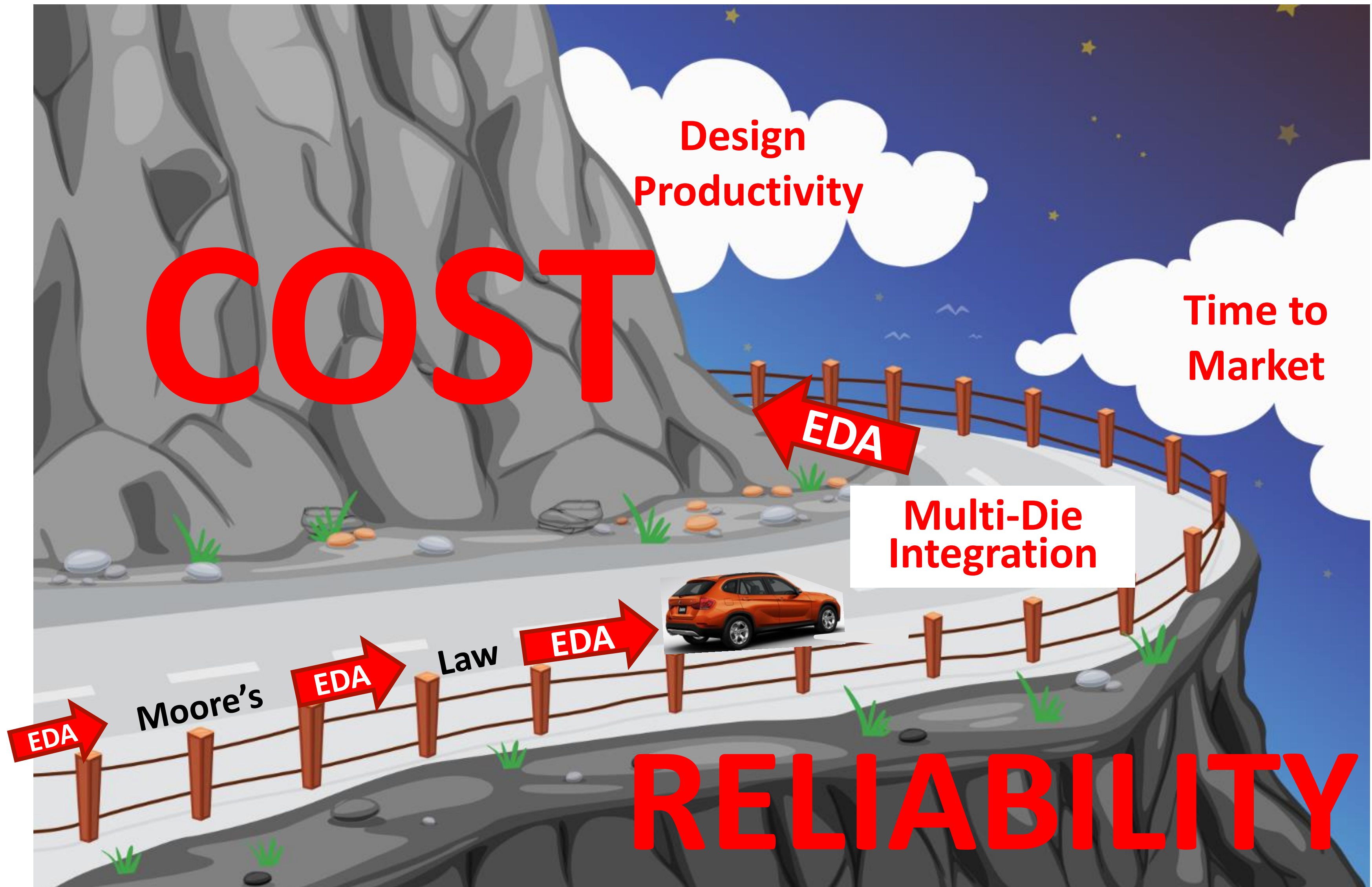
Importance of EDA
Tools and Libraries



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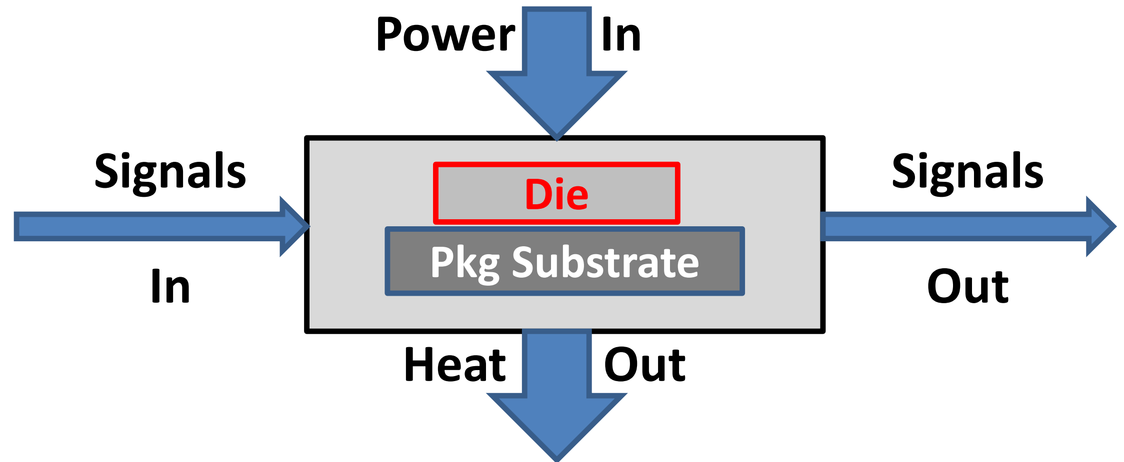
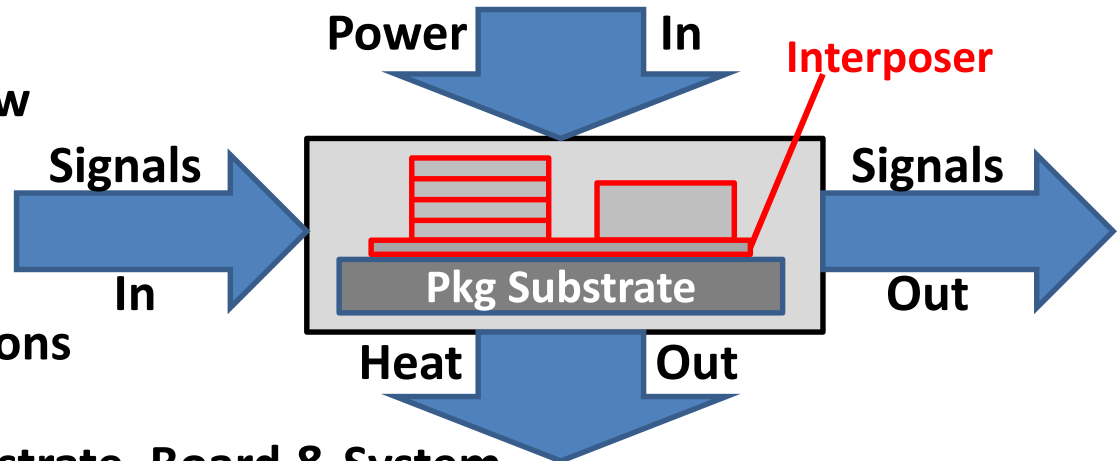
Multi-Die ICs Add To Today's Single Die Packaging Challenges

Power Integrity
Signal Integrity
Bumps Capacitance
Lead Inductance
IC Thermal Limits
…
…



…and
Thinner Die = Less Heat Flow
Heterogeneous Dice
Die to Die Interactions
KGD, Test Coverage
Electrical-Thermal Interactions
Thermo-Mechanical Forces
Thermal Limits of Dice, Substrate, Board & System
Unit COST, Reliability, …



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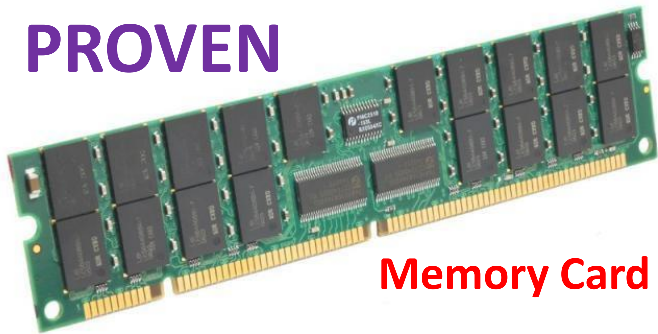
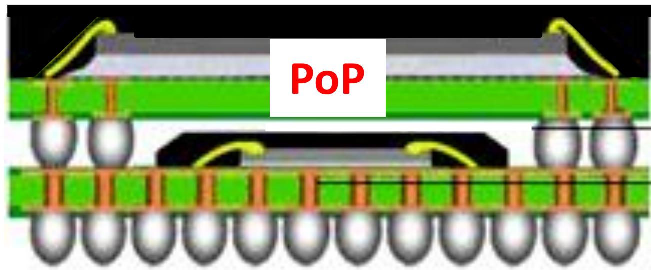
Major Integration Alternatives

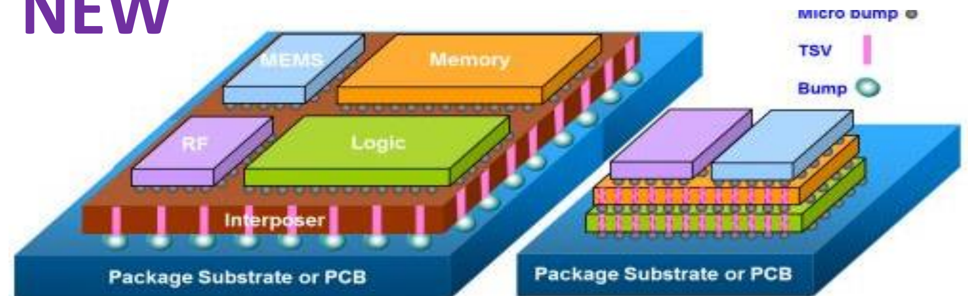
PROVEN



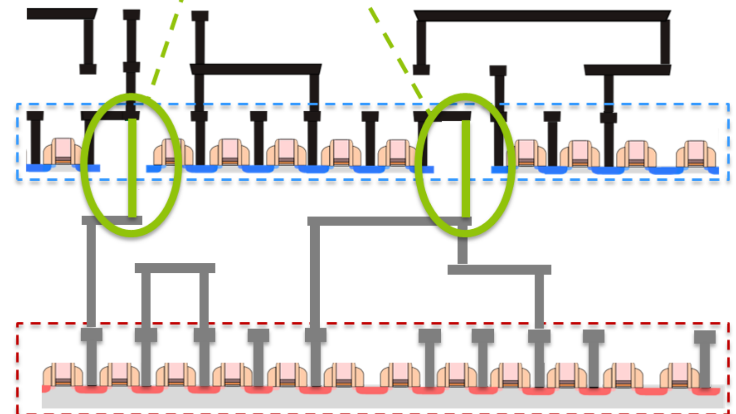


http://www.design-reuse.com/articles/exit/?id=14887&url=http%3A%2F%2Fwww.commsdesign.com%2Farticle%2FprintableArticle.jhtml%3FarticleID%3D196700054

NEW



Monolithic IC "CoolCube"™



Source: Olivier Billoint / CEA Leti, March 2015
"CoolCube" is a Leti Trademark

eda2asic Interposer and 3D EcoSystem Partners

Si2, IPC, GSA, IEEE, JEDEC, MEPTEC, SEMI,...

Engineering Standards & Business Models

Cadence, Mentor, Ansys, Atrenta, eSilicon, Open Silicon, Rambus, Invensas, Promex, ipdia,... Industry Organizations, Design Consultants

System- and IC planning, -design and -verification

Hynix, Micron, Samsung,... and Die-level as well as block-level IP providers

http://www.apple.com/iphone-6/

Wafer Manu-facturing

Global Foundries, Jazz, TSMC, UMC,...

Wafer Thinning and Handling

AMAT, EVG, HHT, Suess, Tokyo Electron,...

Assembly and Test

Amkor, ASE, SPIL, StatsChipPak,...

Advantest, Teradyne,...

New Materials

3M, DNP, Hitachi, Ibiden, IPDiA, Panasonic, Silex, ...

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Opportunity Knocks

http://www.accenture.com/us-en/company/overview/advertising/Pages/index.aspx

2. Multi-Die Applications

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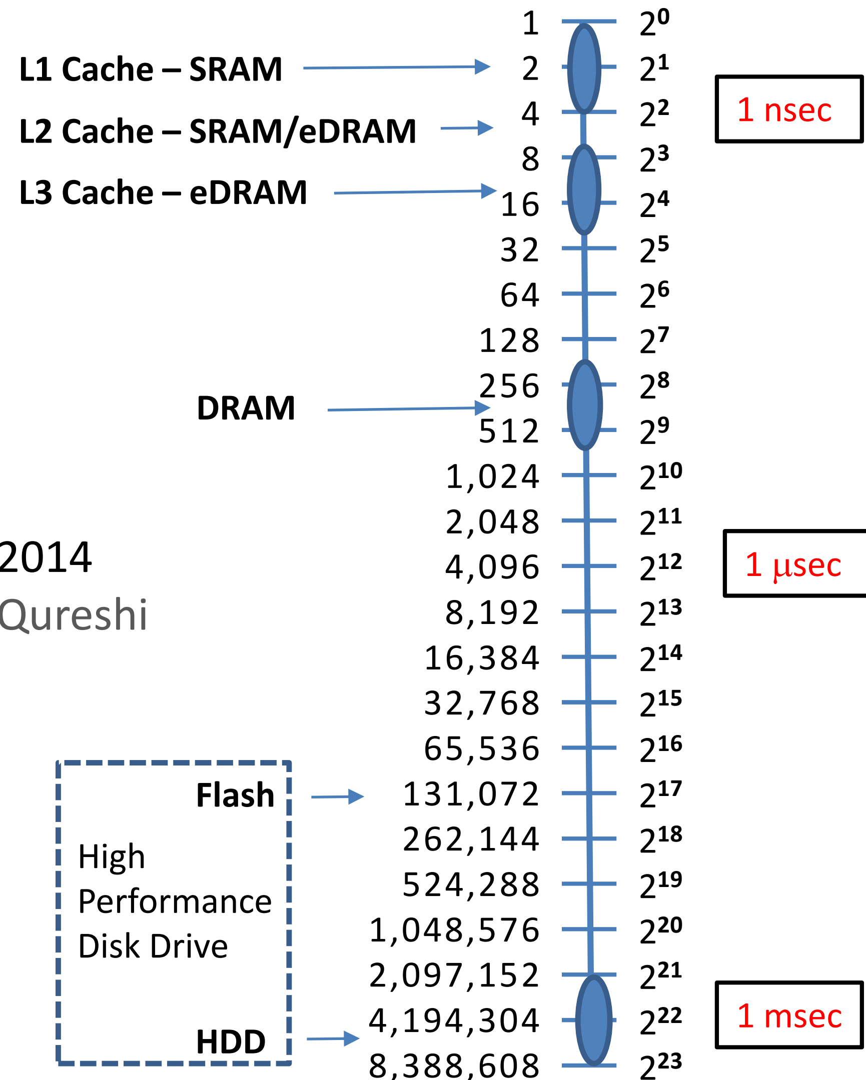
Typical Access Latency in number of Cycles of a 4 GHz Processor
(cycle time = 250 psec)

Based on a presentation by
IBM's Fellow S.S. Iyer at IEDM 2014
Adapted from V. Srinivasa, M. Qureshi



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New Multi-Die Design Methods

❑ 2.5D-IC

- Dice side-by-side and connected to an interposer with TSVs
- No TSVs in dice needed
- TSVs on Interposer are 100 x 10 microns now
- Fast
- Low power
- Easy to cool every die
- Low NRE, little EDA
- Unit cost + interposer
- **Widely deployed now**

❑ 3D-IC

- Dice vertically stacked and interconnected in the assembly process
- All but top die w TSVs
- TSVs currently 50 x 5 μ, 40 x 2 in development
- Faster
- Lower power
- Difficult to cool center
- Higher NRE, more EDA
- Medium unit cost
- **In Memory Cubes now**

❑ Monolithic 3D

- Circuitry vertically stacked. Wafers run 2+ times through fab
- Vias connect circuitry
- Vias between layers of circuitry only tens of nm
- Fastest
- Lowest power
- Cooling needs are less
- Highest NRE, most EDA
- Lowest unit cost

V NAND is in Production

- **In Development now**

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2.5/3D Application Examples

3D Memory Cubes from Hynix, Micron, Samsung in many Applications, e.g.:

Market Segment or Application	Key Benefits	Key Challenge(s)	PUBLICLY ANNOUNCED Projects
Computing	Speed, Bandwidth	Power-Density	Intel & Micron: CPU
Networking	Bandwidth, Latency	Power-Density	**IBM & SEMTECH: ADC & DSP** TSMC & Huawei: NPU
Graphics	Bandwidth, Power Savings	Power-Density, Component Cost	Nvidia & Hynix & TSMC: GPU AMD & Hynix & …. : GPU
Wireless/Mobile	Bandwidth, Power, Size	Component Cost	**Samsung Tablet: Exynos 5 and DRAM stacked using Wide I/O 1**
Industrial/Auto	Heterogeneous - Integration	Too new… Reliability	…. & …: Vision Systems
IoT Peripherals	Power, Size, Heterog. Integr.	Component Cost	……………………: IoT Platform(s)
FPGAs	Gate Count, Power Savings	DesignComplexity, Component Cost	**Xilinx & TSMC & SPIL: High-end FPGA Family**

… and Samsung's V-NAND in production in SSDs for Google, …

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Pointers to Above Examples

❑ Monolithic Flash Memories' Unit Cost and Speed becoming compelling

Samsung strikes SSD drive deal with Google http://www.koreatimes.co.kr/www/news/tech/2015/03/133_176227.html

New 3D NAND flash will triple capacity of SSDs, Intel and Micron

http://www.pcworld.com/article/2902246/new-3d-nand-flash-will-triple-capacity-of-ssds-intel-and-micron-say.html

❑ JEDEC and HMCC standardize TSV-connected Memory Cubes' Interfaces

Detailed (100+ pages) datasheets of memory cubes - for free downloading - available at:

HMC http://hybridmemorycube.org/files/SiteDownloads/HMC-30G VSR_HMCC_Specification_Rev2.0_Public.pdf

HBM http://www.jedec.org/standards-documents/docs/jesd235

Wide I/O 2 http://www.jedec.org/standards-documents/docs/jesd229-2

❑ Interposer-based Designs

XILINX FPGA family: https://ca.finance.yahoo.com/news/xilinx-delivers-industrys-first-4m-120000221.html

Intel/Micron: http://newsroom.intel.com/community/intel_newsroom/blog/2015/03/26/micron-and-intel-unveil-new-3d-nand-flash-memory

IBM/SEMTECH: http://www.semtech.com/Press-Releases/2010/semtech-and-ibm-join-forces-to-develop-high-performance-integrated-adcdsp-platform-using-3d-tsv-technology.html

TSMC/Huawei: http://www.extremetech.com/computing/190941-tsmc-announces-its-first-16nm-finfet-networking-chip-32-core-arm-cortex-a57#disqus_thread

Nvidia/TSMC/Hynix: http://www.digitaltrends.com/computing/what-is-nvidias-volta-gpu-what-will-it-do-for-pcs/#!WIqZO

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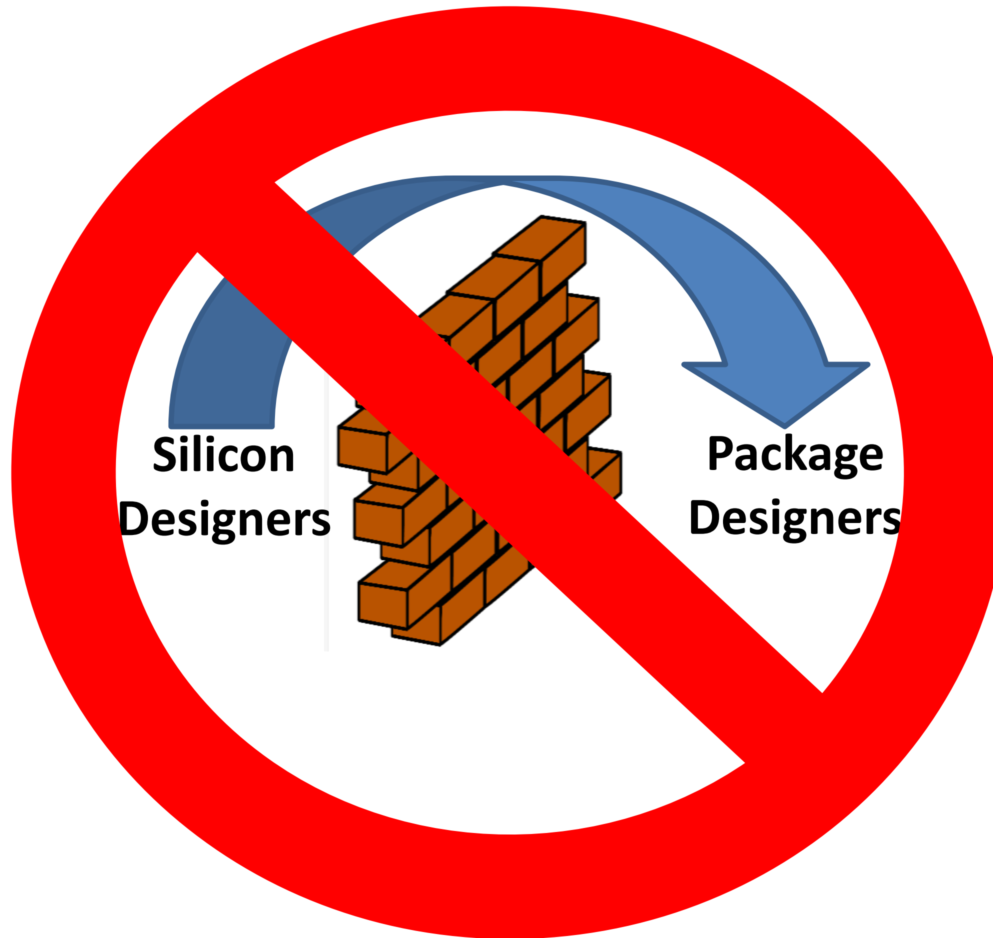
3. Die – Package CO-Design Flow
incl. Assembly Design Kit (ADK)



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Die-Package CO-Design Flow

Data-flow, formats and responsibilities highly structured,
True "Sign-off" technically feasible

Pathfinding, Design & Verify ICs
Si2: TOOLS INTEROPERABILITY

Captive Packaging Expert(s) and OSAT Engineering Team cooperate to make die-pkg combo cost-effective

FRONT-END (Wafer-fab)
Capabilities & Constraints

Proven PDK

Process Design Kit

- **Libraries**
- **Design Rules**
- **Spice Models**
- **Reference Flows**
- **Utilities**
- **....**

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Die-Package CO-Design Flow

Data-flow, formats and responsibilities highly structured, True "Sign-off" technically feasible

Data-flow, formats and responsibilities not clearly structured, "Sign-off" NOT feasible today

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Si2: TOOLS INTEROPERABILITY

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BACK-END (Assembly)
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Heatsink Data
PCB Stack-up
Ball/Pin Data
Underfill Data
Package D
Substrate Stack-up

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Pathfinding, Design & Verify ICs
Si2: TOOLS INTEROPERABILITY

Plan, Design & Verify Pkg
Si2: MODELING & DATA FORMATs

XML Models

XML Models

FRONT-END (Wafer-fab)
Capabilities & Constraints

BACK-END (Assembly)
Capabilities & Constraints

Proven PDK

Process Design Kit

- Libraries
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- ....

New ADK

Assembly Design Kit

Heatsink Data
PCB Stack-up
Ball/Pin Data
Underfill Data
Package D
Substrate Stack-up

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XML Models

XML Models

FRONT-END (Wafer-fab)
Capabilities & Constraints

BACK-END (Assembly)
Capabilities & Constraints

New Working Group in Si2

Proven PDK

Process Design Kit

- Libraries
- Design Rules
- Spice Models
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- ....

Universal Design Kit

U D K

New ADK

Assembly Design Kit

Heatsink Data
Ball/Pin Data
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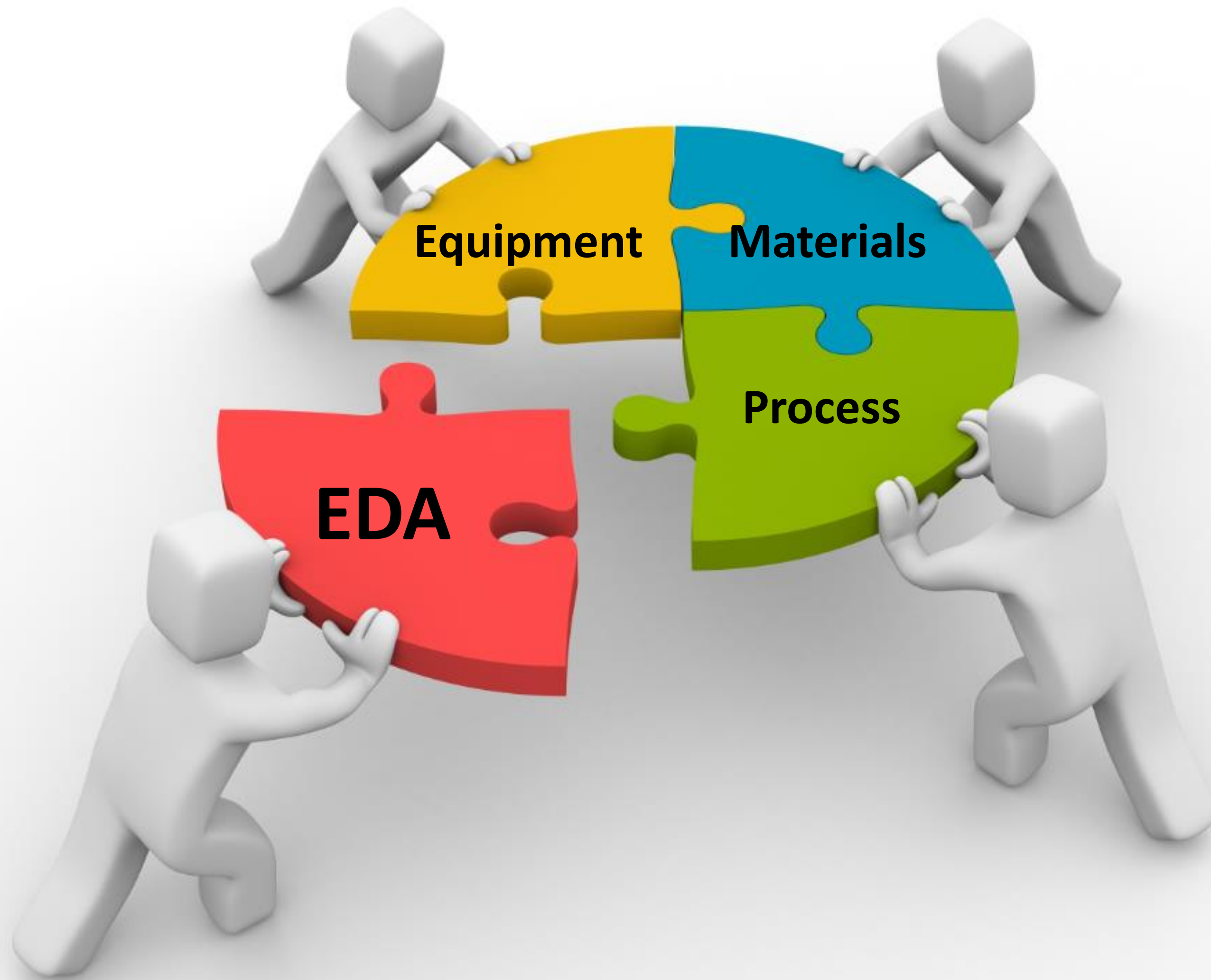
4. Other Multi-Die EDA Challenges



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EDA Challenges to Address

- Modeling and Data Formats as EDA tools' inputs
  - Capabilities, material characteristics, fab flows,…
- Tools interoperability; user-friendly design flows

- PathFinding/partitioning IC- and system designs
- Much higher complexity (sub-) system designs
- Higher abstraction levels → die-level IP models
- Integrating multiple heterogeneous dice
- Electrical – Thermal – Mechanical interactions

- **Closer developer ←→ user cooperation**

5. What's Next ?

2020s

2019

2018

2017

2016

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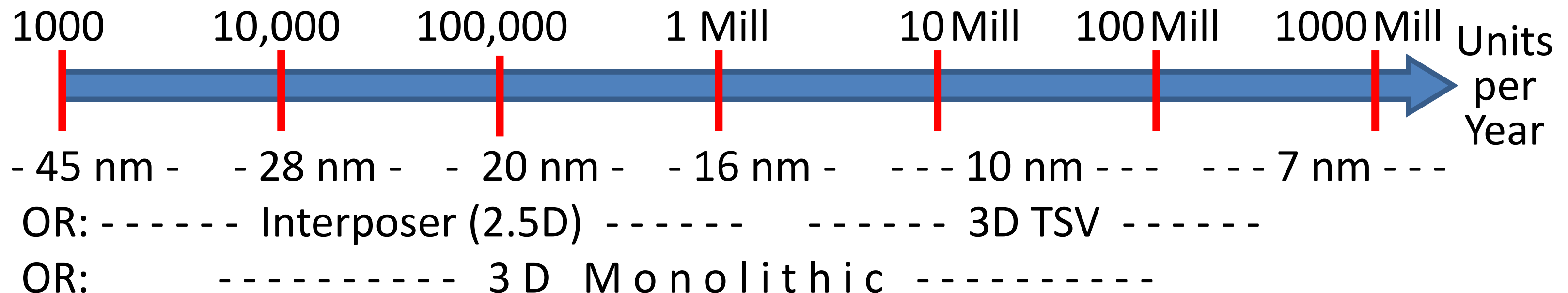
A Peek into the Near / Far Future

2010s

- Production volumes will drive 2.5/3D **cost reductions**
- **Cost reductions** will further increase market demand
- Unit volume determines choice of technology, e.g.:



2020s

- Bigger library of die-level mega-functions for 2.5/3D-ICs
- IC designers develop these die-level IP building blocks
- System designers create systems with these blocks
- Rules & Standards as backbone for WW cooperation

6. SUMMARY

1: EDA and Manufacturing to reduce unit cost

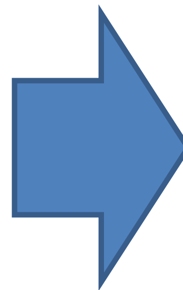
2: Business models to enable closer cooperation

3: Interposer- & 3D-ICs aren't simple components, they are system building blocks

Semiconductors may follow the Automotive Industry

➔ Use Modularity: Die-level IP blocks from subcontractors

➔ Build a strong EcoSystem with clear responsibilities



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THANK YOU !

Q & A

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