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Panel Session:

Tradeoffs in bulk planar FET, FD-SOI, and FinFET Design

IEEE Electronic Design Process Symposium, 4/23/2015
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Outline

1) Introduction
  - terminology
  - device cross-sections, device parasitics
  - process options: triple-wells, Vt's, Lg bias, analog components

2) Device modeling
  - compact models
  - sources of variation
  - parasitic extraction and reduction

3) Design of library cells

4) Methods for power/performance optimization
  - path-level and block-level optimizations
  - body-biasing, Lg bias
  - dynamic methods – e.g., DVFS

Focus will be on design tradeoffs

tradeoff *noun*

Definition:

a balancing of factors all of which are not attainable at the same time

Each process option has advantages and disadvantages that must be evaluated against design objectives – i.e., power, performance, area (PPA), and ultimately, cost.

(NOTE: Circuit reliability – both aging effects and the susceptibility to external upset events – is also a key factor. These won't be discussed in detail in these slides.)

Introduction

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Terminology

Process lithography "nodes":

- 45/40nm, 32/28nm, 22/20nm, 16/14nm, 10nm, 7nm

Device options to be reviewed:

1) bulk planar FET

2) Fully-Depleted Silicon-on-Insulator (FD-SOI) FET
   - aka, "Ultra-Thin Body SOI" (UTBSOI)

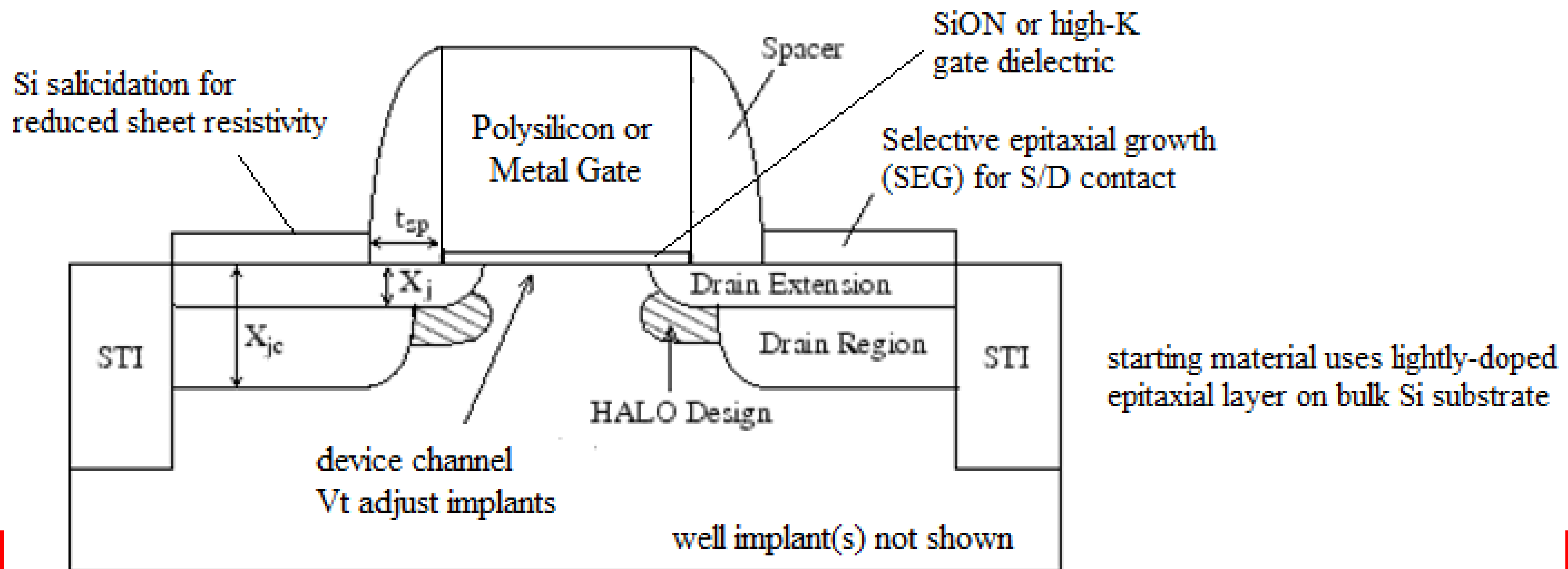
3) FinFET
   - bulk or SOI substrate
   - aka, "Tri-gate FET" (nomenclature used by Intel)

(NOTE: All commercial FinFET processes are currently using a single gate covering the fin sides and top, rather than an independent dual-gate input.)

Device cross sections

Bulk planar FET

- well implants
  - “twin” wells for nFET/pFET devices, “triple” well for nFET isolation
- implant to provide “halo” for short-channel punch-through control
- implants to offer device Vt options (e.g., HVT, SVT, LVT, ULVT)
- implant to provide the lightly-doped channel extension (LDD)
- NOTE: There are add’l. implants for I/O (high-voltage) devices.



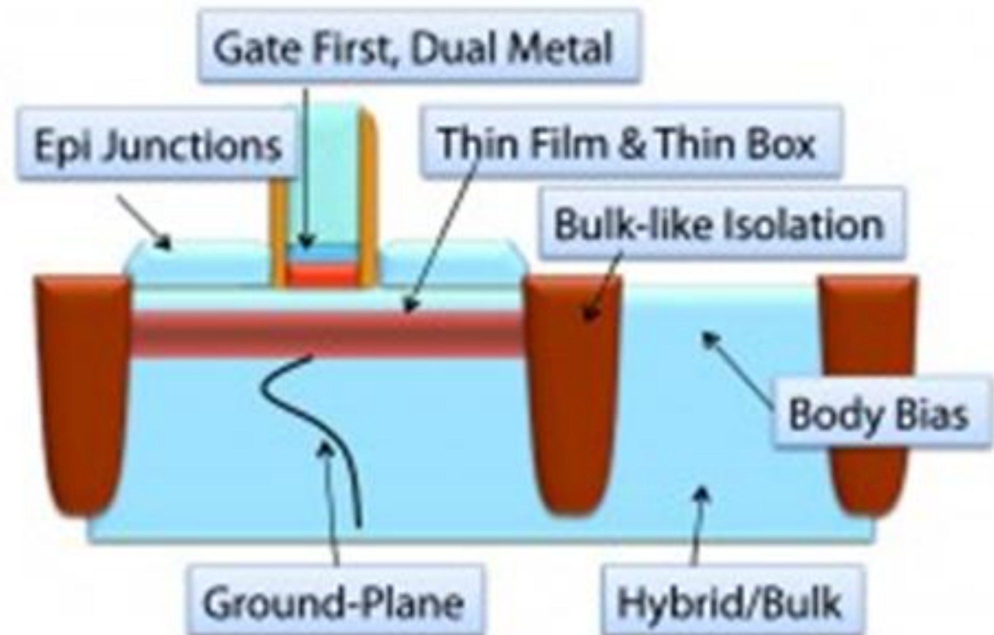
http://www.iue.tuwien.ac.at/phd/wittmann/node6.html

Device cross sections

Fully-depleted Silicon-on-Insulator (FD-SOI)

- thin Silicon epitaxial layer over a dielectric ("ultra-thin body")
  - device body is "depleted" of free carriers at |Vgs| = 0
- Selective Epitaxial Growth for S/D contact areas
- Vt options:
  - gate workfunction potential, "ground plane" or well implant below body
- "hybrid" process used to implement bulk components, body contact

- Channel extension implant required, but no "halo" implant

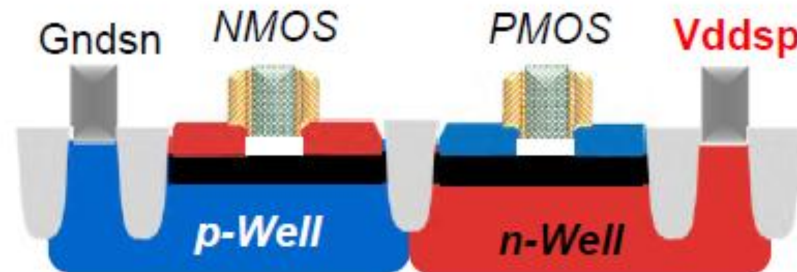


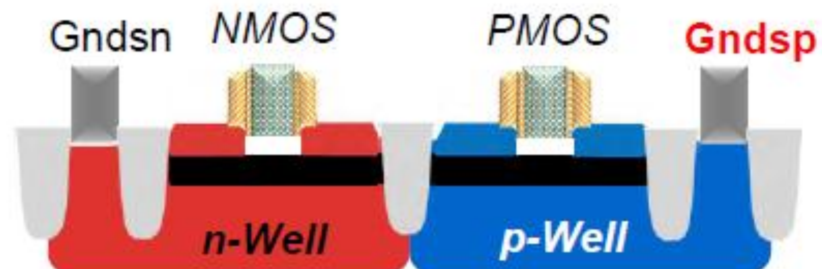
http://www.advancedsubstratenews.com/2011/11/st-fd-soi-for-competitive-socs-at-28nm-and-beyond/

Device cross sections

Fully-depleted Silicon-on-Insulator (FD-SOI) – body voltage bias

- Vt options:
  - Depending upon the target utilization of reverse and forward back-bias, alternative Vt's are also provided by a “flip well” implant (and contact):





UTBB-FDSOI Design and Migration Methodology.pdf, P. Flatresse, ST Microelectronics

Device cross sections

Fully-depleted Silicon-on-Insulator (FD-SOI) – substrates

- The prevalent method for FD-SOI substrate manufacture uses the “SmartCut” process, licensed by SOITEC to wafer suppliers.

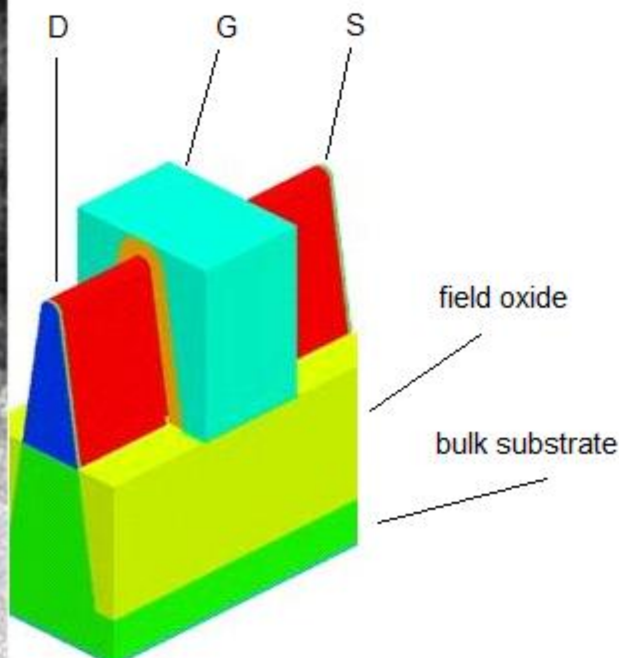
For the 28nm node, the uniformity of the thin Silicon layer is +/- 5A over the 300mm wafer, equivalent to 0.2” between Chicago and San Francisco.

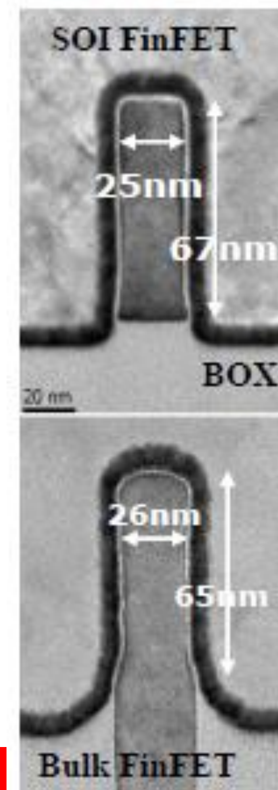
http://www.soitec.com/en/products-and-services/microelectronics/fd-2d/

Device cross sections

FinFET

- a vertical silicon “fin” is fabricated for the device channel, with a surrounding thin (HK) dielectric and (metal) gate input
- fins can be fabricated on either bulk silicon wafers or SOI
- similar to FD-SOI, the FinFET channel region is fully depleted





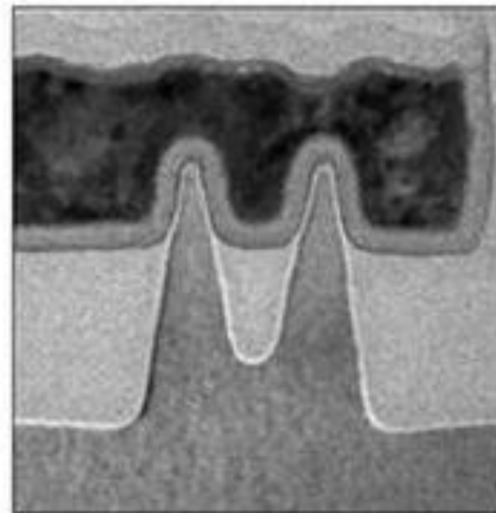
“Benchmarking SOI and bulk FinFET alternatives for PLANAR CMOS scaling succession”, **Solid-State Electronics, Volume 54, Issue 9, Sept. 2010, p. 855-860.**

Device cross sections

FinFET – continued

- the profile of initial 22nm FinFET’s in production is relatively “tapered”, with rounding at the fin top
- to better enable device scaling, increasing R&D efforts are being applied to fabricate a more rectangular fin profile

Transistor Fin Improvement



22 nm 1st Generation Tri-gate Transistor

14 nm 2nd Generation Tri-gate Transistor

Intel, IEDM-2014, as reported by: http://www.eetimes.com/document.asp?doc_id=1324343

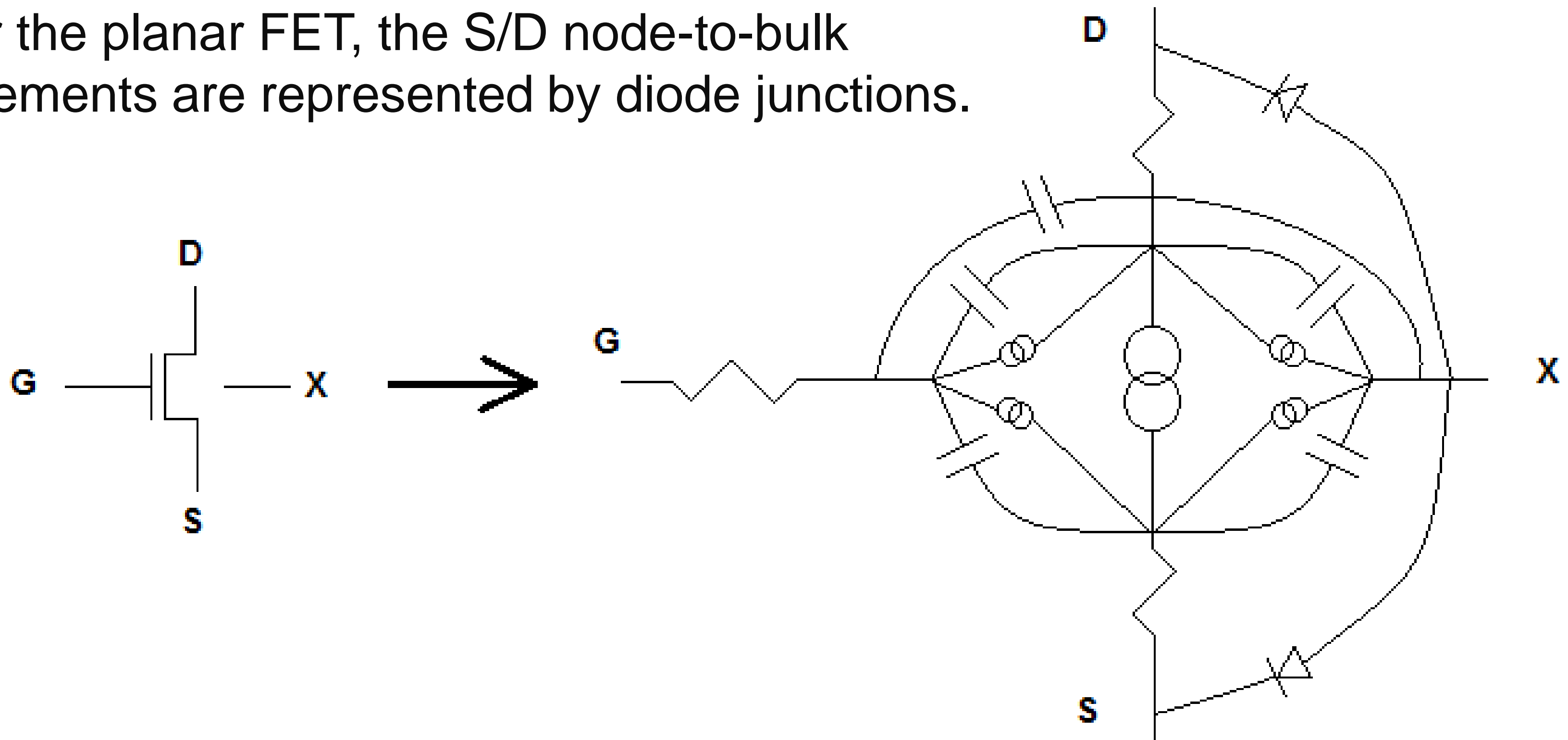
Device parasitics

The general FET circuit simulation model consists of:

- a voltage-dependent current source
- parasitic resistance,
- and (voltage-dependent) capacitance elements

- Each element is a function of the (electrical) W/L of the device,.

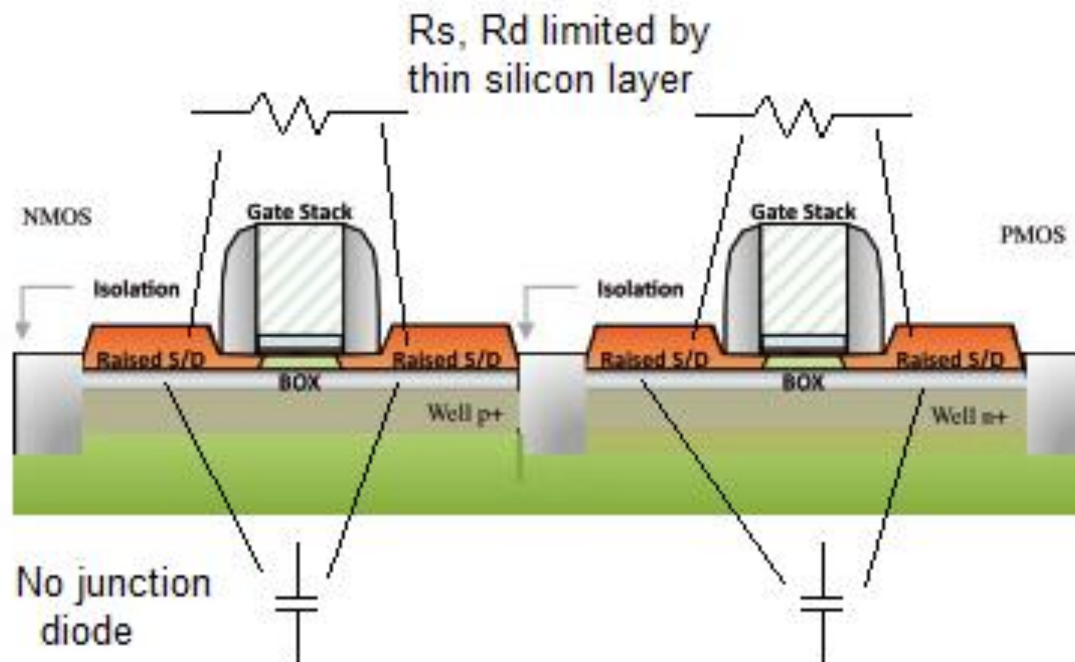
- For the planar FET, the S/D node-to-bulk elements are represented by diode junctions.



Device parasitics – FD-SOI

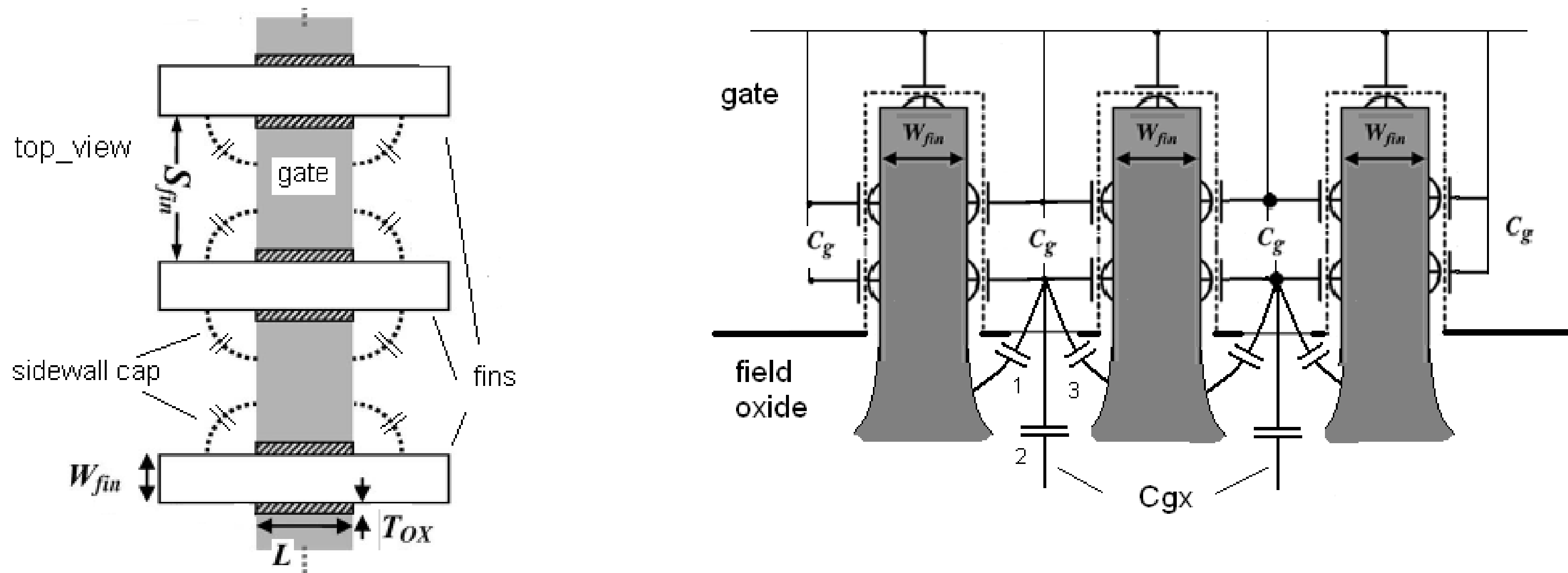
The parasitics of the FD-SOI device differ from the planar FET:

- The channel and S/D junction diode-to-substrate elements are reduced to a capacitance (with the buried oxide dielectric thickness) → no junction leakage is present.
- Rd and Rs are increased, due to the thin Si layer.
  - Selective epitaxy growth reduces the Rd and Rs "spreading" resistance to the device contact.



Device parasitics – FinFET

Each individual FinFET has numerous parasitic capacitances, due to the topography of the gate traversing over the fin:



3 fins in parallel with common gate input – top and cross-section views, showing parasitic gate input sidewall capacitance and gate-to-substrate capacitance

The very high effective drive current per sq. um of the FinFET is mitigated somewhat by the higher C_in parasitics.

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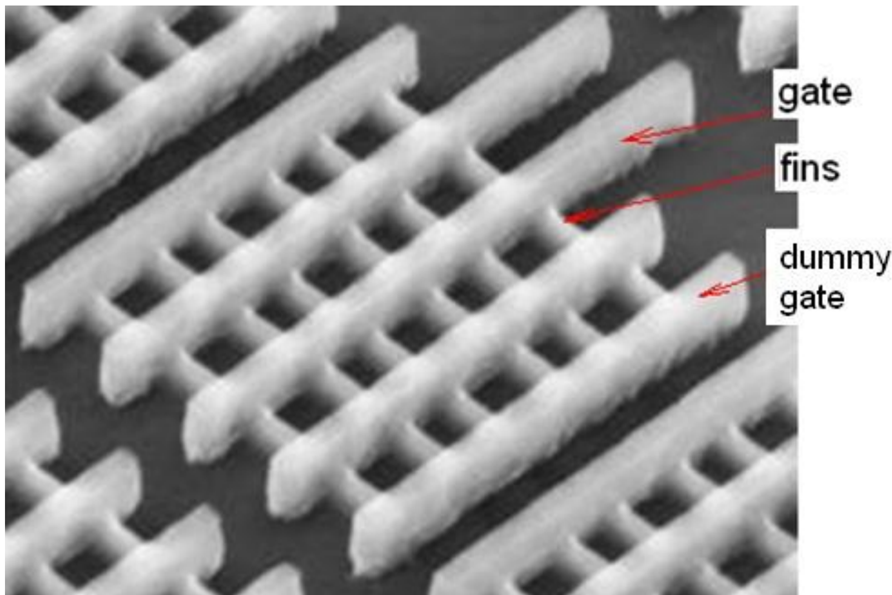
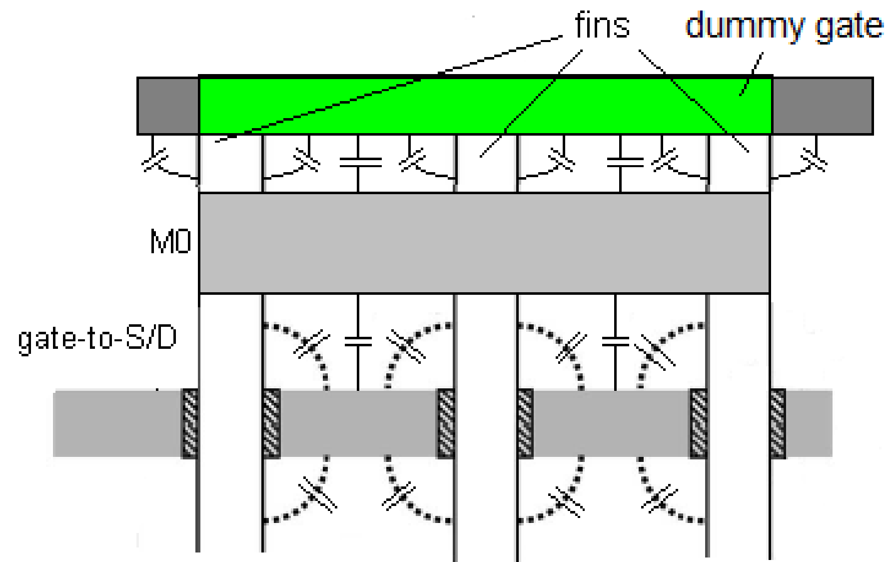
Device parasitics – FinFET (continued)

For uniformity of SEG for the FinFET source/drain, dummy devices are added at the end of the fins → additional parasitics.





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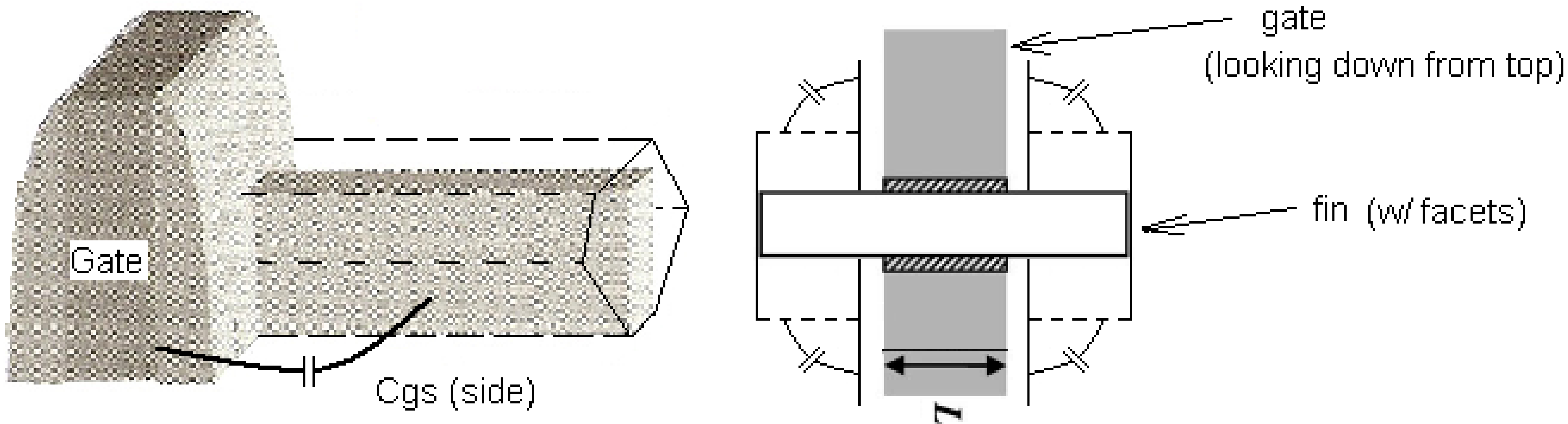
Device parasitics – FinFET (continued)

The SEG for the the FinFET source/drain results in complex gate-to-fin sidewall geometry, for Cgs/Cgd parasitic extraction.



Cgs/Cgd – another sidewall view

Process Options

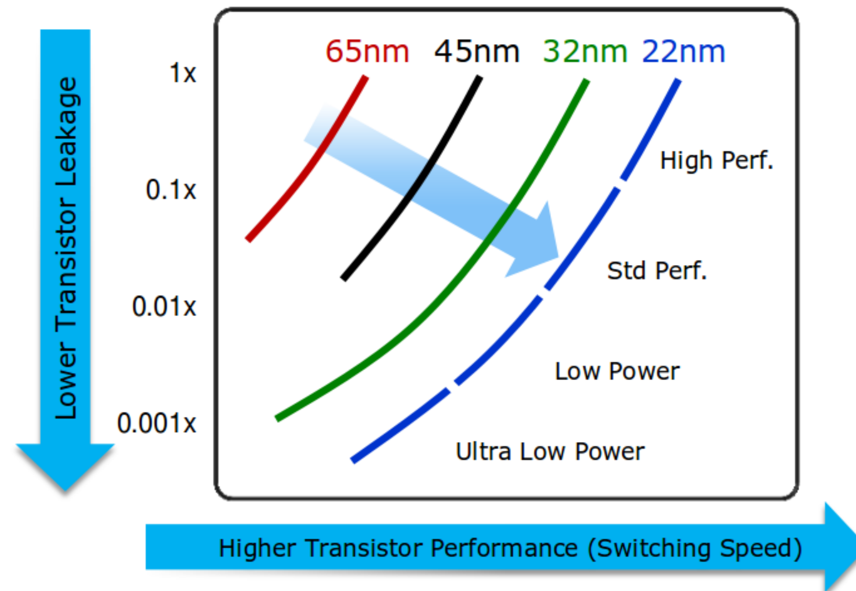
Vt's

- Multiple Vt's are typically available, characterized by the "Ioff vs. Ion" (log-linear) curve for a typical device

Stdcell libraries offer Vt variants for logic functions, for power/perf optimization.

For layout efficiency, all N or P devices in a logic gate usually have the same Vt.

Typically, these cells use the same footprint, for post-physical design swaps.

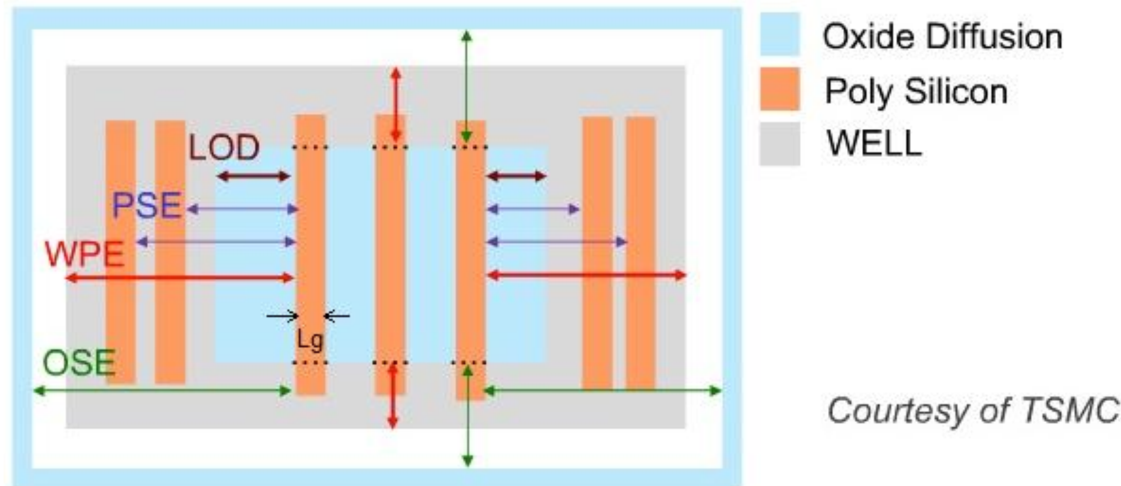


From Intel Developer Forum 2012

Process Options

Gate length

- Circuit designers typically have some latitude in selecting the device gate length, as another option for power/perf optimization.
  - NOTE: that range is MUCH reduced in DSM processes

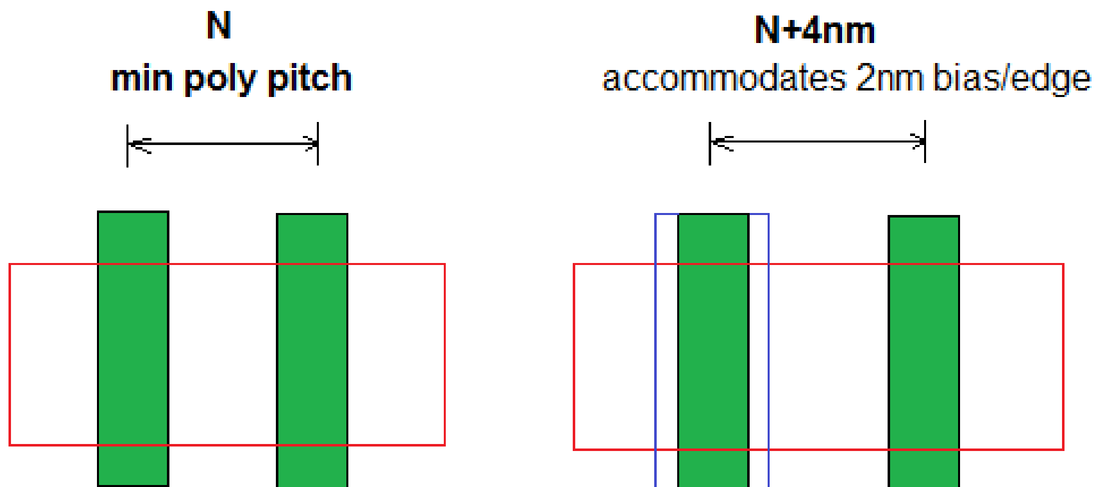


- Digital cells may offer some Lg variants in the released library
  - Requires add'l. characterization (w/ layout-dependent effects)
  - Vt variants are a more common library design approach

Process Options

Lg bias approach

- Another common post-PD optimization is to override the as-drawn gate length with a small Lg “bias” – e.g., ~2-4nm Lg addition
  - The gate pitch in the cells is selected to accommodate bias
  - Small change in circuit performance, big change in leakage
    - No need to re-characterize cells (e.g., minor Cg increase)
  - Applied only to select, non-critical devices to reduce leakage
    - Positive timing slack on the gate input
    - Mask overlay shape added to GDS-II, can be easily removed
    - Multiple, adjacent gate lengths need to be “litho-friendly”



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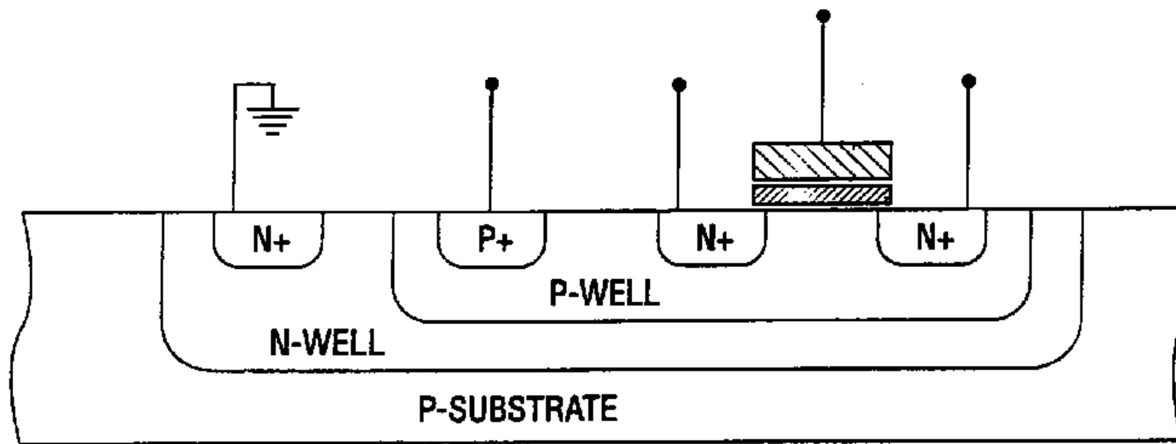
Process Options

"Triple-well" (independent p-well) devices

- An add'l. p-well implant (planar or FinFET device) is introduced, that allows for electrical isolation of the nMOS substrate potential.
- Used for highly-sensitive analog circuits, to isolate the "noisy" digital substrate from the analog device body.



- Other options include adding "guard rings" around sensitive layouts for improved isolation.

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Diagram from US Patent Application EP0810667A2

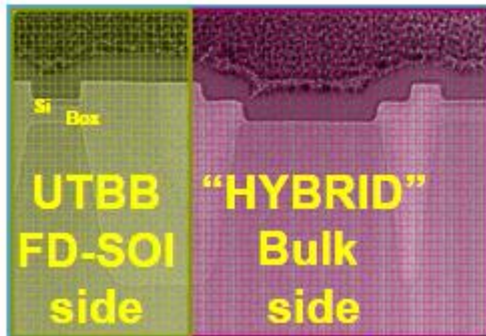
Process Options

Analog components

- Processes differ greatly on how various analog structures are implemented – diodes, BJT's, varactors, precision + well resistors.
- Need to review your analog component specs. with the foundry

<u>Example</u>

- FD-SOI utilizes a "hybrid bulk" region for some analog structures. (similar to the the BOX opening to the bulk for back-side contact)



Device Type	UTBB FD-SOI	BULK
Logic	2Vt / PB0-16nm	
SRAM	✓	
Capacitor		✓ (EG)
Varactor	✓ (SG,EG)	
Drift MOS (OTP)		✓
Digital I/O	✓	
Power Switch P	✓	
Resistors	✓ (Poly)	✓ (Active)
Diodes (antenna)		✓
ESD Devices	✓ (FET)	✓ (FET, diode, SCR)
Vertical Bipolar		✓

From:
"Seamless design migration to FD-SOI",
L. LePailleur, STMicro

Device modeling

Device modeling

- All device types require the development of a "compact model", that can be efficiently used in a circuit network simulation tool.

- The qualification of compact models for the EDA industry is led by the Compact Model Coalition, a group within Si2.

https://www.si2.org/cmc_index.php

- Models have been qualified for planar, SOI, and FinFET devices.

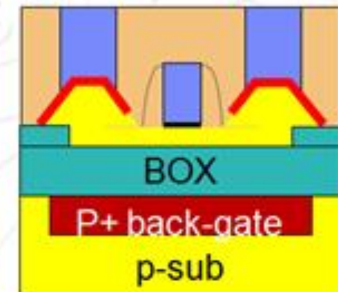
Device modeling

- Although multiple MOSFET models have been adopted, the prevalent formats are:
  - BSIM
  - BSIM-SOI (Partially Depleted)
  - BSIM-CMG (FinFET),and
  - BSIM-IMG (FD-SOI)

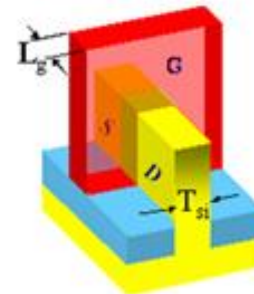
BSIM-IMG

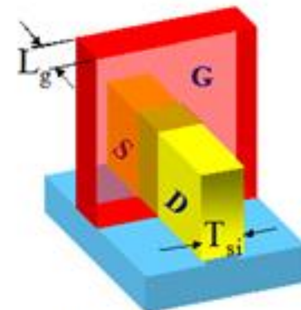
UTBSOI

BG-ETSOI



BSIM-CMG





FinFETs on Bulk and SOI Substrates

http://www-device.eecs.berkeley.edu/bsim/?page=BSIMCMG_FAQ

Device modeling

Foundries may add to the Compact Model, providing a software interface layer that provides additional features, and expands to the underlying model parameters.

- Device layout dependent effects
  (NOTE: There are no LDE parameters currently incorporated into the CMC BSIM-CMG or BSIM-IMG models, only BSIM and BSIM-SOI.)
- Statistical model variation
- Device aging model drift (e.g., NBTI, PBTI)

•The CMC is working on "standardizing" the software interface layer above the models, as well:

Next, CMC also supports standardization of various application programming interfaces (API) supporting designers who need access to model parameters during simulation. For example, TMI2 is a CMC-standard API that currently supports the BSIM3 model. Additionally, efforts are underway to develop a standard reliability interface for designers who need to vary parameters in support of reliability analysis. *Si2-CMC Member Report 2014*

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Device modeling

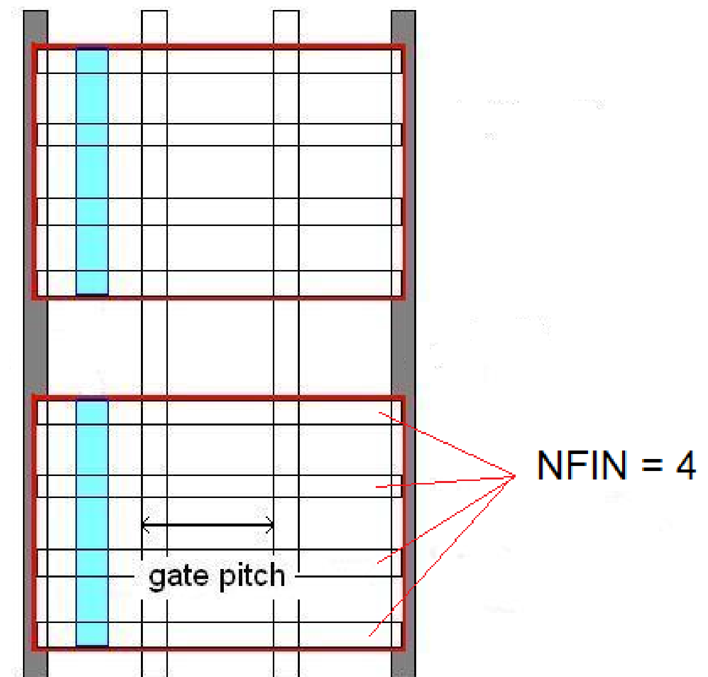
One specific note about FinFET BSIM-CMG models…

NFIN_total = NFIN * NFINGERS (NFIN = # of fins/finger)

$$I_{ds} = IDS0MULT \cdot \mu_0(T) \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot i_{ds0} \cdot \frac{M_{oc}}{D_{vsat} \cdot D_r \cdot D_{mob}} \times NFIN_{total} \qquad (3.280)$$

- The unique layout-dependent effects for edge fins must be handled in the model interface software layer.

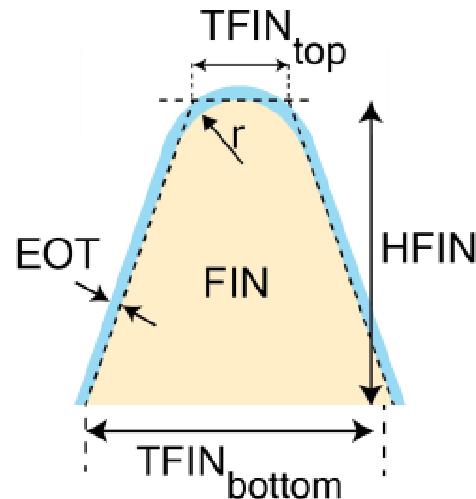
- The "distributed" gate input RC parasitic model is approximated, using the NFIN multiplier. Inaccuracy is controlled by a low "max number of fins/finger".



Device modeling

One other quick note about FinFET BSIM-CMG models…

- Work is ongoing at UC-B to develop a BSIM-CMG model that better fits the behavior of non-rectangular fin profiles:



And, the BSIM team is anticipating needing to model a wider variety of (high mobility) fin semiconductor materials – e.g., SiGe, Ge, InGaAs.

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Device modeling

Sources of variation

- RDF: random dopant fluctuation
  (reduced with FD-SOI and FinFET's)
- LER: gate line edge roughness
- t_ox
- Metal gate grain boundary variation (Vt workfunction, Rgate)

Sources of variation specific to the FinFET geometry include:

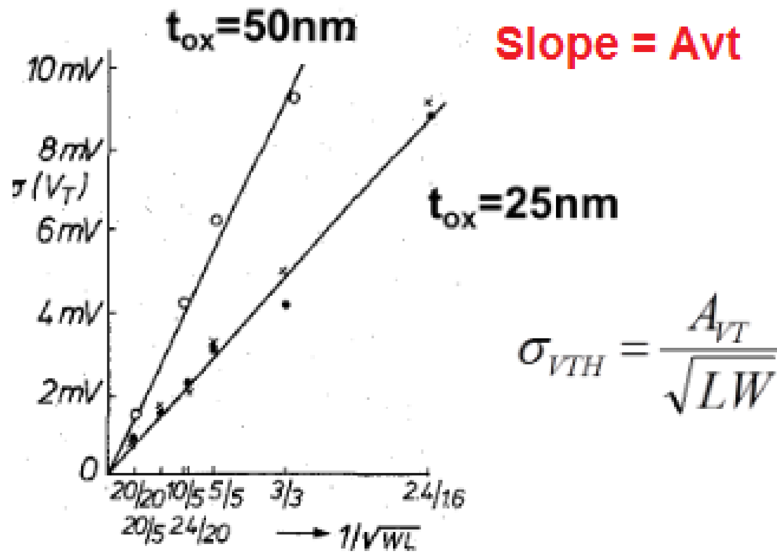
- Fin height
- Fin thickness
- Fin corner rounding profile
- Fin sidewall roughness
- Gate CD length variation over multiple, parallel fins

Baravelli, et al, "Impact of Line Edge Roughness and Random Dopant Fluctuation on FinFET Matching Performance", IEEE Transactions on Nanotechnology, v.7(3), May 2008.

Device modeling

Sources of variation

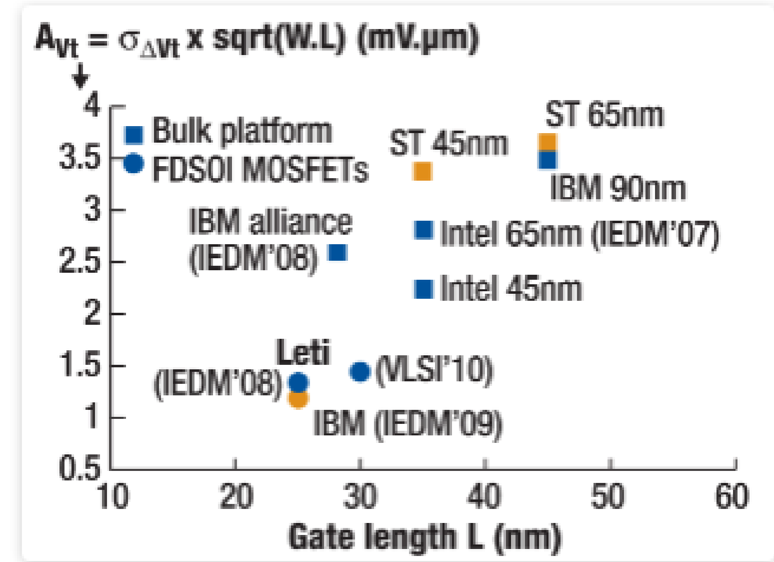
- Most of the sources of variation impact the device Vt
- The Pelgrom parameter ("Avt") remains the standard for comparing the threshold voltage variation between processes:



$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

Basic Pelgrom plot (w/ 2 different tox values)

M.J.M. Pelgrom, et al., JSSC, Vol. 24, No. 5, October, 1989.



Reported Avt values for various bulk and FDSOI processes

http://electroiq.com/blog/2010/11/planar-fully-depleted-soi-the-technological/

Device modeling

Parasitic extraction

The key questions:

“What parasitic Cgs, Cgd, Cgx, Rs, Rd, and Rg elements are incorporated into the device model (and model API)?”

“What elements are to be annotated to the device netlist by layout parasitic extraction (SPEF parasitic file)?”

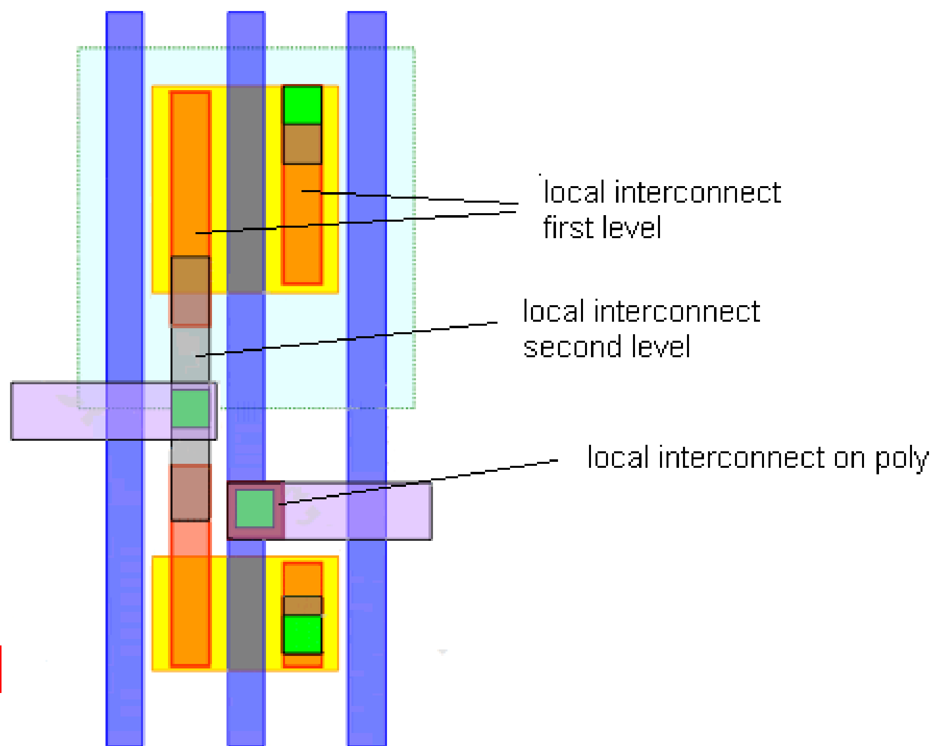
“What parasitic reduction is done for multiple device fingers for the same logical gate input?”

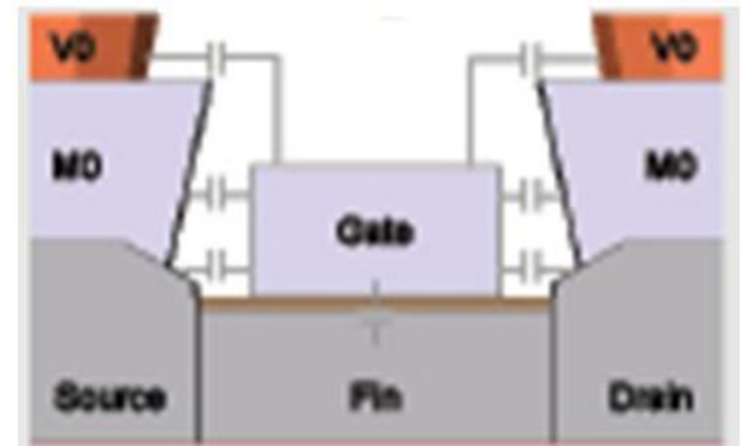
“What parasitic reduction is done for multiple fins in a finger?”

Device modeling

Parasitic extraction

- Recent process nodes have added Local Interconnect to active and gate nodes prior to Metal_1 contacts (aka "MEOL").
- These materials require additional focus on extraction qualification for elements Cgs and Cgd (especially for FinFET's).

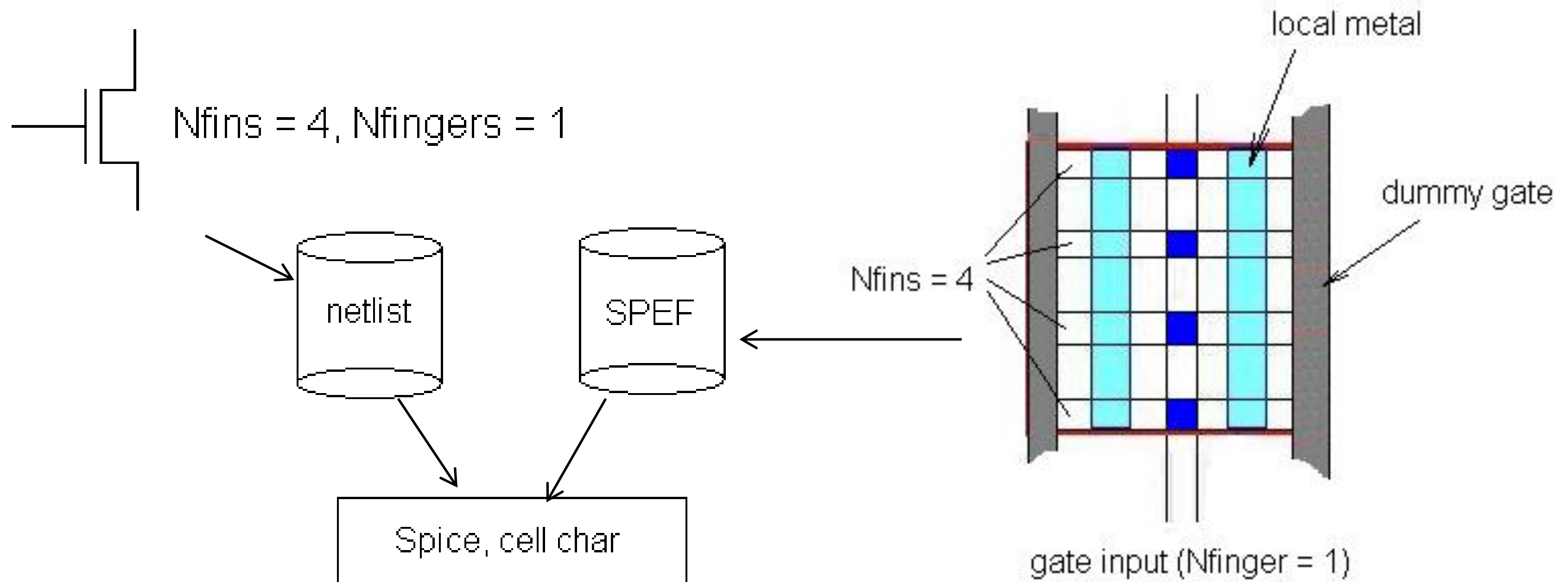




cross-section showing M0 MEOL local interconnect

Parasitic reduction

- To annotate the extracted model, it is necessary to “reduce” the parasitic elements to the corresponding device netlist.



- Individual FinFET extracted capacitances (Cgs, Cgd, Cgx, Csx, Cdx), resistances (Rs and Rd), and “Rgate” need to be suitably reduced to annotate to the netlist model derived from schematics.

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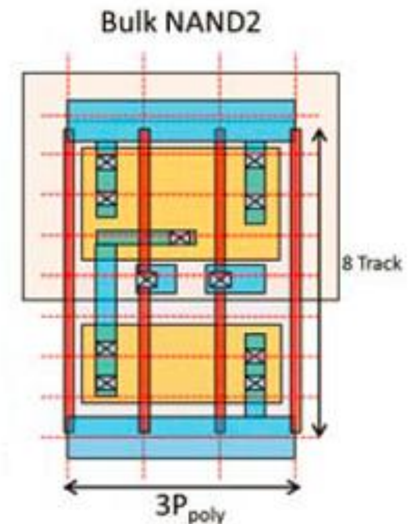
Design of library cells

Library cells – general

Lots of design tradeoffs when developing standard cell libraries…

- logic offerings (esp., max # of logical inputs on complex gates)
- flop and latch offerings (also, multi-port register file options)
- clk drivers (requiring balanced RDLY/FDLY)
- drive strength range for each offering (e.g., NAND2_1X to _8X)
- standard cell template height (in the # of M1 wiring tracks)
    - power rail + grid design to the cell rows
    - cell abutment options
      (e.g., shared wells and rail contacts)
- Vt offerings, for power/performance opt.
  (HVT, SVT, LVT, ULVT)
- DFT architecture
- compatibility with decap cell design + insertion



Library cells – general

Similar considerations are required for the I/O cell library…

- drive strength + output impedance matching
  - support for differential signaling
- cell template (with consideration for the bump pitch)
  - power rail design
  - cell abutment options
    - both horizontal and vertical perimeter I/O's, internal I/O's?
- external supply voltage compatibility (e.g., 2.5V, 1.8V, 1.5V)
- DFT architecture (e.g., JTAG)
- ESD robustness

Library cells for planar, FD-SOI, and FinFET processes

- Cell abutment requirements
  - shared power supply rails/contacts
  - shared well regions
    - especially important consideration for FD-SOI, if different wells are used for Vt selection and/or unique body bias
- Poly gate litho uniformity (for advanced nodes)
  - ensuring “dummy” poly gates at cell edges
  - requires library design and insertion algorithm for “fill cells” (inactive) between placed stdcells

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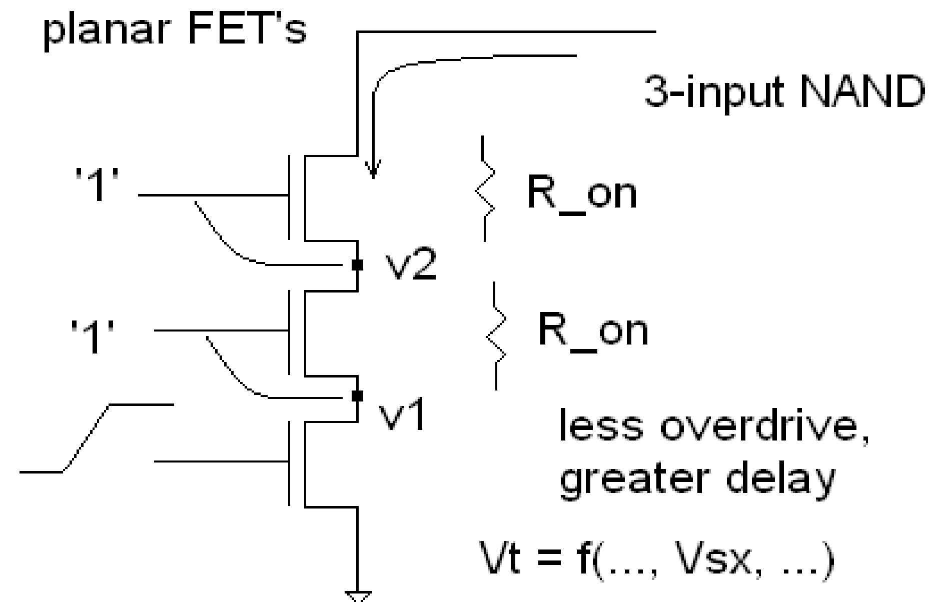
Library cells for planar, FD-SOI, and FinFET processes

- Body effect on circuit performance
  - FinFET technologies have a weak “body effect”: Vt = f(Vsx)
  - body effect has a negative performance impact for high fan-in logic gates (stacked FET’s):



  - FinFET libraries leverage higher I_on/um**2, weak body effect
    - higher fan-in logic may be offered, higher gates/mm**2

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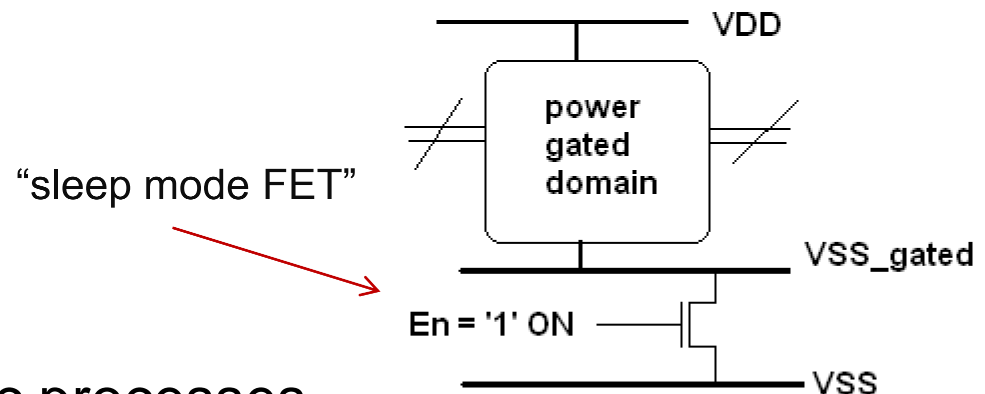
Methods for power/performance optimization

Path-level and block-level power optimizations

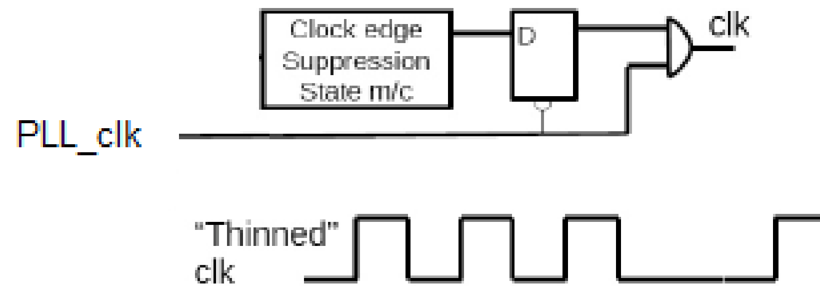
- Applicable to planar, FD-SOI, and FinFET’s
  - “downsizing” cell Vt’s to reduce leakage (during or post-PD)
  - gate length bias (during or post-PD path optimization)
    - limited range in 1xnm processes, for litho uniformity
  - clock gating (with sequential logic depth)
  - “sleep FET” power rail interruption (a block-level optimization)



- Applicability limited to specific processes
  - body “negative back bias” (a block-level optimization)
    - limited range for planar devices, wider range for FD-SOI
    - not effective for FinFET’s

Dynamic methods for performance/power optimization

- Applicable to planar, FD-SOI, and FinFET's
  - Dynamic Voltage and Frequency Scaling (DVFS)
    - assuming the clock need not be periodic, clock pulses can be suppressed to reduce the "effective" frequency



  - Adaptive Voltage Scaling (AVS)
    - additional on-chip performance and/or thermal sensing circuitry provides feedback to voltage regulator(s)
- Adaptive Body Bias for threshold scaling – best suited for FD-SOI

From: Amrutur, et al., J. Low Power Electron. Appl., 2011, 261-276.

Summary

Summary

- Bulk planar, FD-SOI, and FinFET process options offer a diverse set of device tradeoffs, in terms of:

  - I_on vs. I_off characteristics
  - Vt and gate length bias alternatives
  - device modeling and parasitic extraction requirements
    - sources of device variation
  - circuit design (cell library) logic offerings
  - implementation of analog structures
  - power/performance optimization options
    - esp., back bias ("body effect") device threshold control

- It is crucial to assess these tradeoffs as they apply to your design requirements, to select the optimal process.

BACKUP SLIDES

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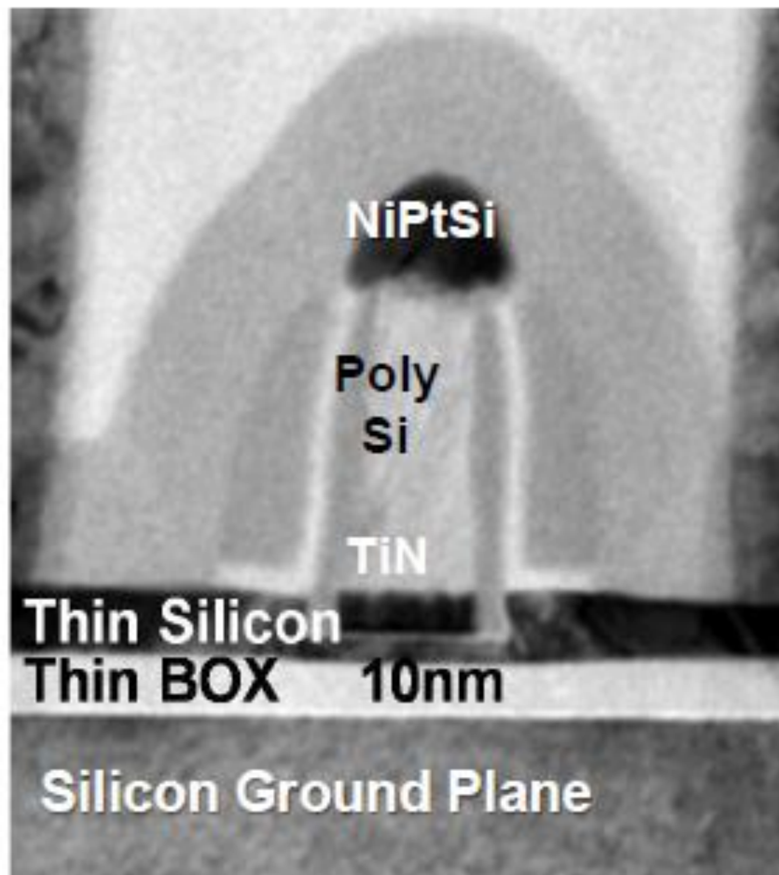
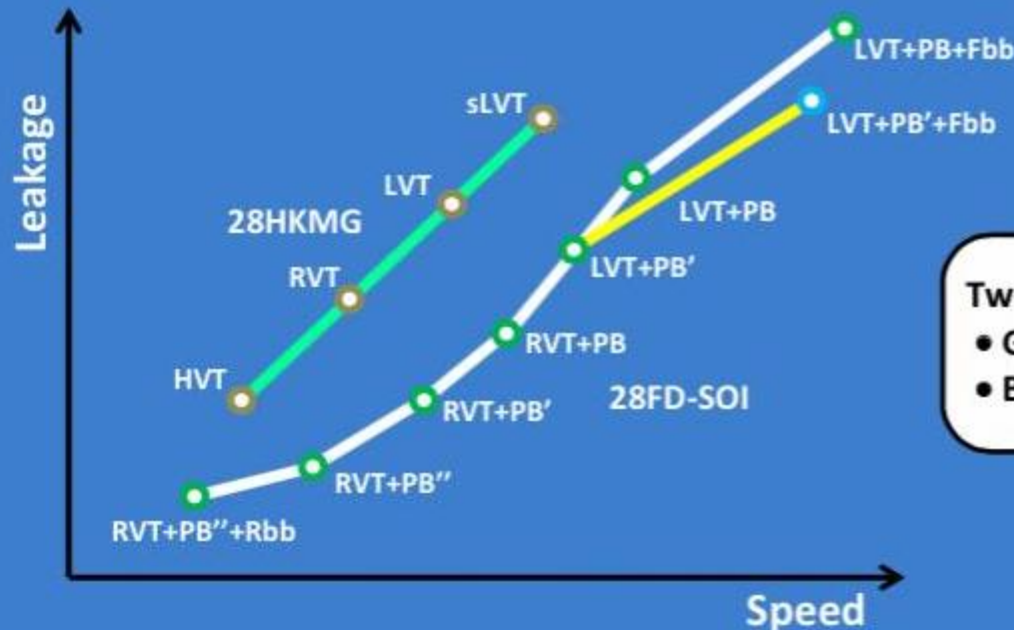


- Shallow Trench Isolation
- Ground-Plane Implant
- $HfZrO_2$/TiN/poly-Si gate stack formation
- Offset Spacer Formation
- Selective Si Epitaxy
- LDD Implantation
- D-shaped Spacer Formation
- S/D Implantation + RTA
- Silicidation (NiPtSi)

TEM cross-sectional view of UTBB FD-SOI MOSFET and its key fabrication flow



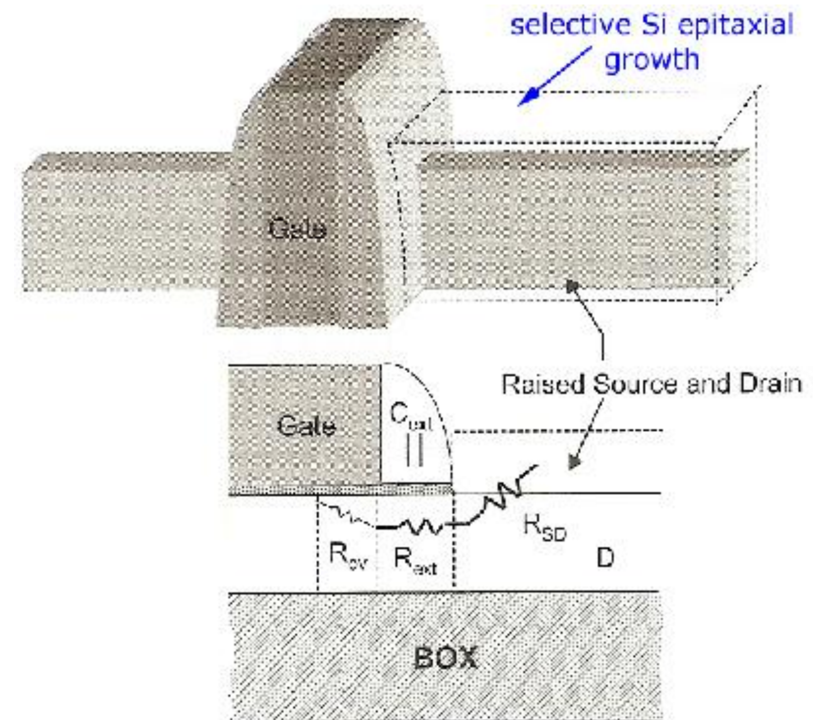
Ioff versus Ion curve for FD-SOI, including: Vt selection, gate length bias (PB), and body voltage bias (Fbb, Rbb)

FinFET’s – reducing Rs and Rd through SEG

- Additional processing steps are taken to reduce the resistance of the source/drain regions (Rs, Rd).

- Selective Epitaxial Growth adds silicon volume, after the FinFET gate is formed – a “raised” source/drain.

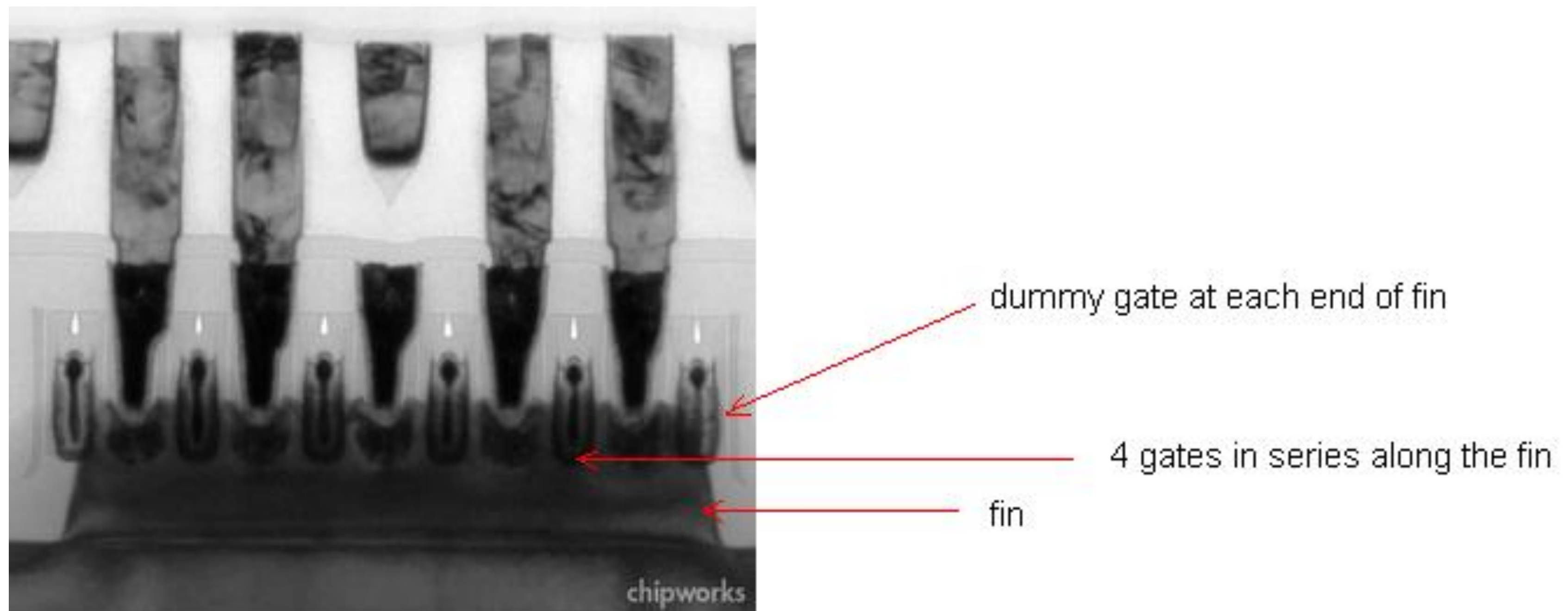
  - gate spacer defines SEG volume
  - reduces Rs_total and Rd_total:
    (Roverlap + Rext + Rspreading)
  - different SEG for nFET's & pFET's
    (SiGe for pFET's for mobility enh.)
  - **higher Cgs and Cgd**



Wade Xiong, “FinFET’s and Other Multi-Gate Transistors”, J.P. Colinge (Ed.), Springer, 2008.

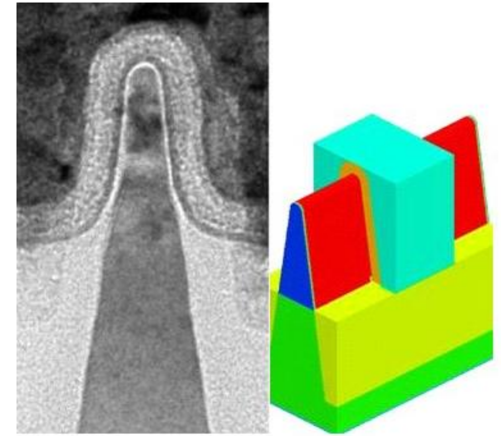
Dummy devices for process uniformity

- The ends of the fins include a “dummy” gate, which is also part of the parasitic FinFET model (cross-sectional view):



http://www.chip-architect.com/news/2012_04_19_Ivy_Bridges_GPU_2-25_times_Sandys.html

Parasitic FinFET extraction – ITF



ITF format to support FinFET's

MULTIGATE fin1 {

FIN_SPACING = <space of fin>

FIN_WIDTH = <width of fin>

FIN_LENGTH = <length of fin>

FIN_THICKNESS = <thickness of fin>

GATE_OXIDE_TOP_T=<gate oxide top thickness>

GATE_OXIDE_SIDE_T=<gate oxide side thickness> (optional)

GATE_OXIDE_ER=<gate oxide permittivity>

GATE_POLY_TOP_T=<poly top thickness>

GATE_POLY_SIDE_T=<poly side thickness> (optional)

CHANNEL_ER = <CHANNEL ER>

GATE_DIFFUSION_LAYER_PAIR {(PGATE PDIFF)(NGATE NDIFF)} }

Note that this enhanced ITF format assumes an ideal rectangular fin profile.

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