Beyond Soft IP Quality to Predictable Soft IP Reuse

TSMC 2013 Open Innovation Platform®
Presented at Ecosystem Forum, 2013

Open Innovation Platform®

Agenda

SPYGLASS® FROM ATRENTA

- **Soft IP Quality – Establishing a Baseline With TSMC**
- **Soft IP Quality – What We Checked and What We Found**
- **Soft IP Reuse – Methodology and RTL Signoff**
- **Summary and Next Steps**

TSMC & Atrenta IP Kit - History

Atrenta Announces SpyGlass Tool Used in TSMC Soft IP Qualification Flow

Quality reports generated by SpyGlass® to be available on TSMC web site

San Jose, Calif. and HSINCHU, Taiwan, R.O.C. — May 26, 2011 — Atrenta Inc. today announced the deployment of a comprehensive soft IP qualification program using Atrenta's SpyGlass® platform and a targeted subset of its G
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TSM

Atrenta and TSMC IP Quality Initiative Gains Broad Industry Acceptance

SAN JOSE, Calif. - March 5, 2012 - Atrenta Inc., a leading provider of SoC Realization solutions for the semiconductor and electronic systems industries, today announced that 10 intellectual property (IP) providers have qualified their soft IP for inclusion in the TSMC 9000 IP library using the Atrenta IP Handoff Kit.

Digit
Inc.;
infor
sem

Atrenta and TSMC Announce SpyGlass® IP Kit 2.0 Availability

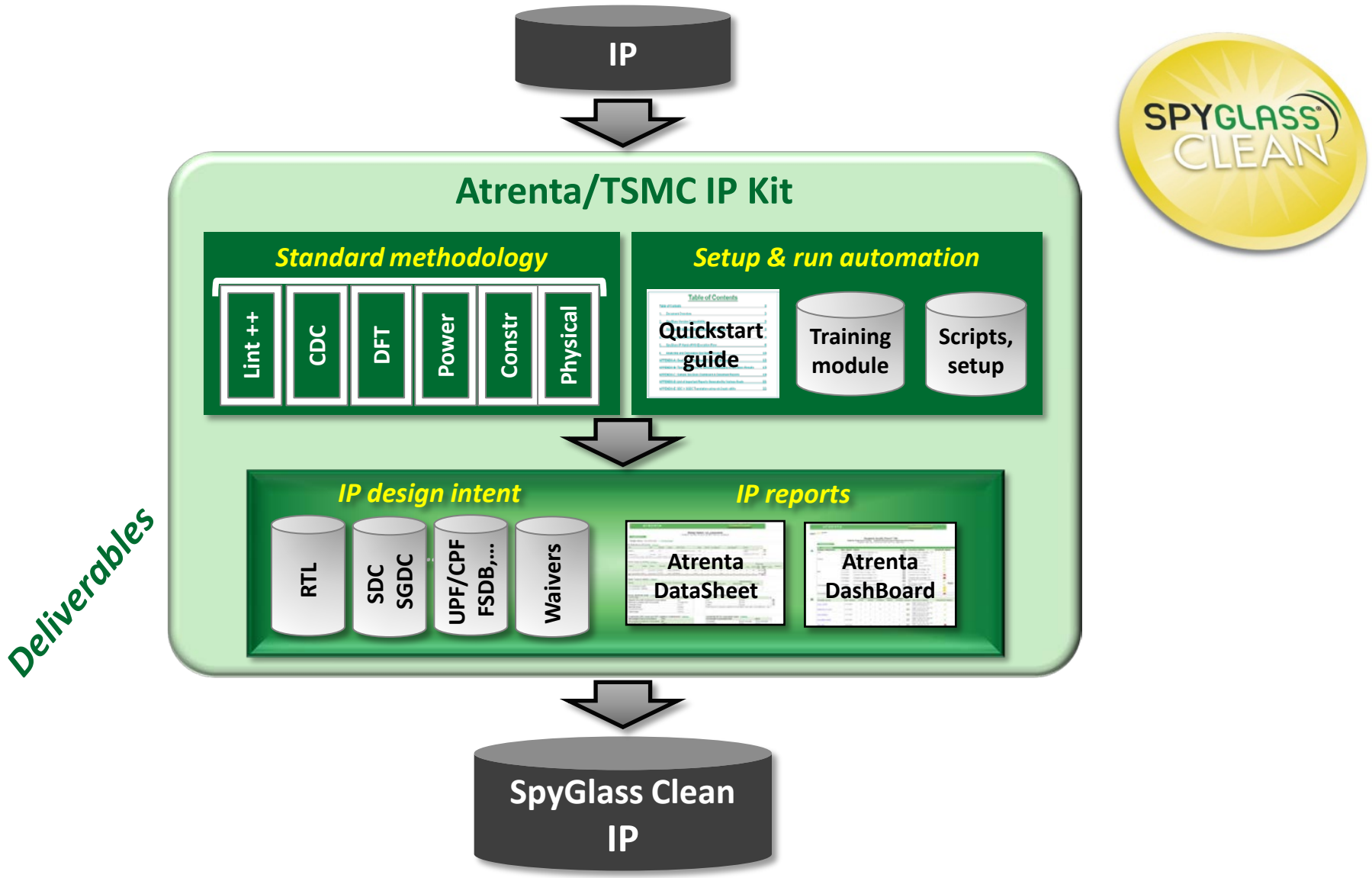
New soft IP qualification platform more comprehensive and easier to use

SAN JOSE, Calif and HSINCHU, Taiwan, R.O.C. — Oct 31, 2012 — Atrenta Inc., the leading provider of SoC Realization solutions for the semiconductor and consumer electronics industries, with TSMC announced today the planned availability of IP Kit 2.0.

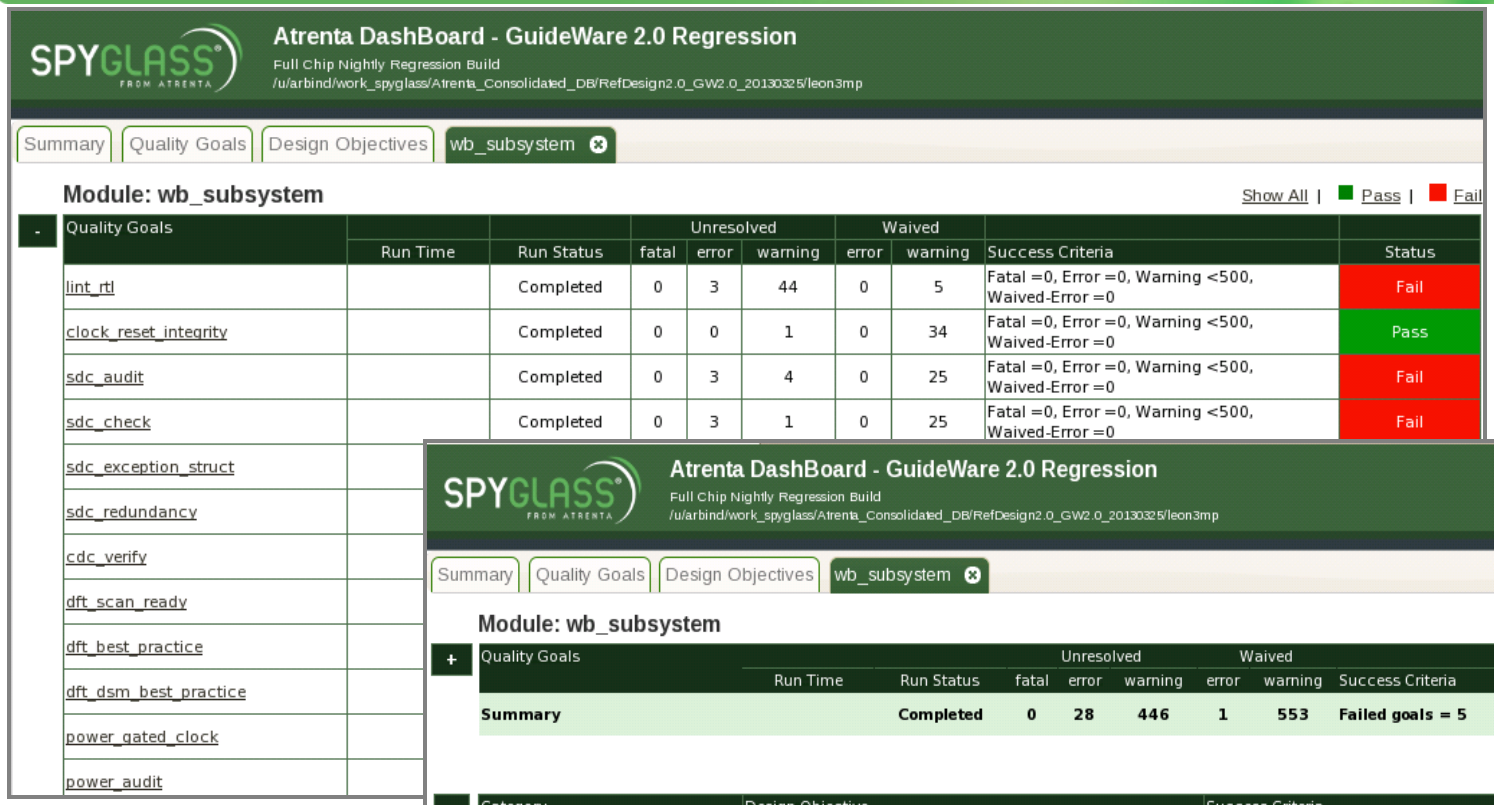
TSMC/Atrenta Collaboration

- **Golden Rules for soft IP handoff analysis**
- **Definition of quality metrics to assess soft IP**
  - Modified severity of errors to conform to quality requirements
- **Enable various IP packaging types**
- **Optimize work flow to ensure ease-of-use and reliable, fast operation**
  - Tuned mandatory vs. optional goals
- **Joint roll out plan development and beta testing with IP partners**
  - Ease of use a critical requirement

IP Kit – Establishing IP Quality Baseline



IP DashBoard Report



Atrenta DashBoard - GuideWare 2.0 Regression

Full Chip Nightly Regression Build

/u/arbind/work_spyglass/Atrenta_Consolidated_DB/RefDesign2.0_GW2.0_20130325/leon3mp

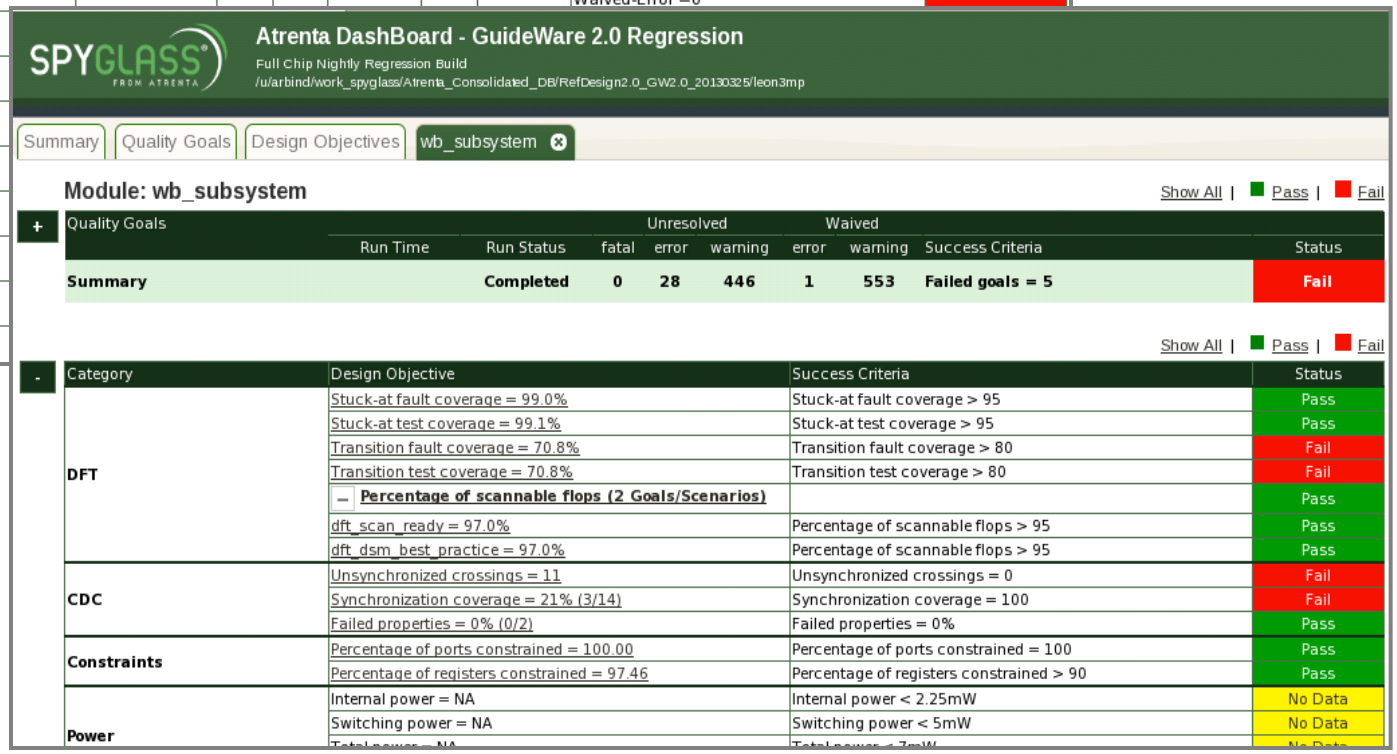
Summary | Quality Goals | Design Objectives | wb_subsystem

Module: wb_subsystem

Show All | Pass | Fail

Quality Goals			Unresolved			Waived			
	Run Time	Run Status	fatal	error	warning	error	warning	Success Criteria	Status
lint_rtl		Completed	0	3	44	0	5	Fatal =0, Error =0, Warning <500, Waived-Error =0	Fail
clock_reset_integrity		Completed	0	0	1	0	34	Fatal =0, Error =0, Warning <500, Waived-Error =0	Pass
sdc_audit		Completed	0	3	4	0	25	Fatal =0, Error =0, Warning <500, Waived-Error =0	Fail
sdc_check		Completed	0	3	1	0	25	Fatal =0, Error =0, Warning <500, Waived-Error =0	Fail
sdc_exception_struct									
sdc_redundancy									
cdc_verify									
dft_scan_ready									
dft_best_practice									
dft_dsm_best_practice									
power_gated_clock									
power_audit									

IP Quality



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Quality Goals			Unresolved			Waived			
	Run Time	Run Status	fatal	error	warning	error	warning	Success Criteria	Status
Summary		**Completed**	**0**	**28**	**446**	**1**	**553**	**Failed goals = 5**	**Fail**

Show All | Pass | Fail

Category	Design Objective	Success Criteria	Status
DFT	Stuck-at fault coverage = 99.0%	Stuck-at fault coverage > 95	Pass
	Stuck-at test coverage = 99.1%	Stuck-at test coverage > 95	Pass
	Transition fault coverage = 70.8%	Transition fault coverage > 80	Fail
	Transition test coverage = 70.8%	Transition test coverage > 80	Fail
	Percentage of scannable flops (2 Goals/Scenarios)		Pass
	dft_scan_ready = 97.0%	Percentage of scannable flops > 95	Pass
	dft_dsm_best_practice = 97.0%	Percentage of scannable flops > 95	Pass
CDC	Unsynchronized crossings = 11	Unsynchronized crossings = 0	Fail
	Synchronization coverage = 21% (3/14)	Synchronization coverage = 100	Fail
	Failed properties = 0% (0/2)	Failed properties = 0%	Pass
Constraints	Percentage of ports constrained = 100.00	Percentage of ports constrained = 100	Pass
	Percentage of registers constrained = 97.46	Percentage of registers constrained > 90	Pass
Power	Internal power = NA	Internal power < 2.25mW	No Data
	Switching power = NA	Switching power < 5mW	No Data

IP Specs

TSMC Soft IP Qualification Program

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IP ecosystem partners

ARM, Arteris, CEVA, Chips Media, intrinsic ID, OMP, AuthenTec, tensilica, SONICS, Discretix, Imagination, MIPS Technologies, PLDA, VIVANTE, COSMIC circuits, GUC, evatronix, DOLPHIN INTEGRATION

tsmc

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Atrenta DashBoard

Atrenta IP Kit 2.0

Handoff

Atrenta DataSheet

TSMC Online

IP1

IP 2

IP 3

IP n

Atrenta summary reports

Atrenta IP Kit 2.0

Inspection/ acceptance

End customers

Chip project 1

Chip project 2

Chip project 3

Chip project n

Strong Uptake on the Program

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DAC 2012

DAC 2013

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IP Kit – Sample Tests

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Power

- What will the average power dissipation be?
- Are my power domains correctly defined?

Clocks & Timing

- Are clock and reset constraints set properly?
- Are clock definitions consistent, correct and complete?
- Are clock domain crossing synchronizers bug-free?
- Are timing constraints consistent across block boundaries?
- Are false path and multi-cycle paths correctly identified?

Lint

- Is the design ready for simulation and synthesis?

Test

- What will the stuck-at and at-speed test coverage be?
- Can all sequential elements be scanned?

What Did We Find?

Many items that would impact integration/debug time and chip function were found & fixed

Some examples:

- **Missing synchronizers on CDC paths causing possible chip function issues**
- **Data loss on fast-slow CDC paths**
- **Uncontrolled data path impacting transition fault coverage**
- **Index out of range which causes synthesizability issues**
- **Unconstrained I/O ports leading to poor SDC coverage**

Faster time to silicon

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Journey – Soft IP Quality to Soft IP Reuse

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- Soft IP quality is a necessary *but not sufficient* condition for soft IP reuse
- Enforcing a known standard of quality for IP blocks is important
- How those blocks are assembled is just as important
- The concept of RTL Signoff* is a critical enabler for successful soft IP reuse

** RTL Signoff: A series of must-pass requirements before the flow proceeds*

Traditional Signoff

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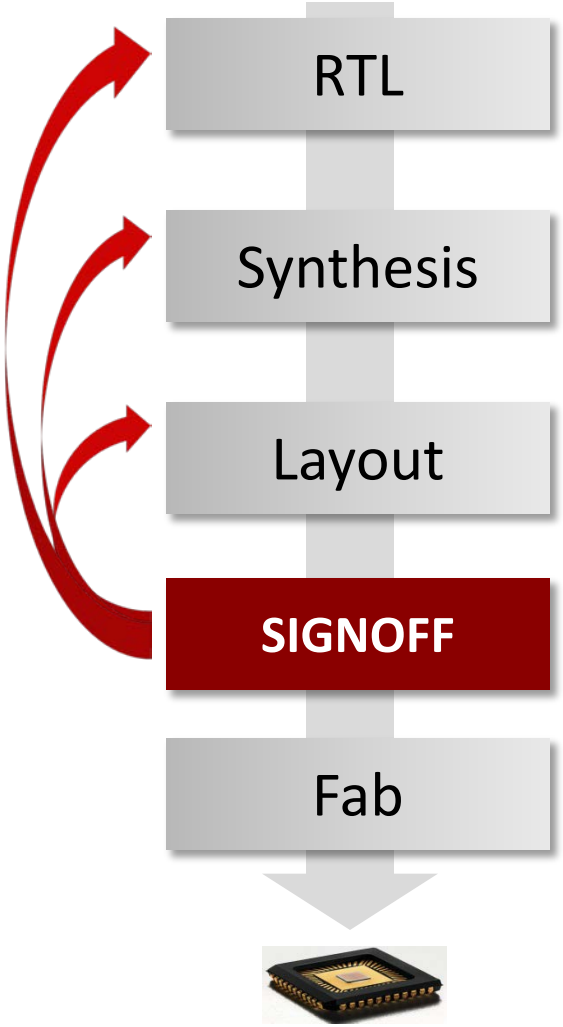
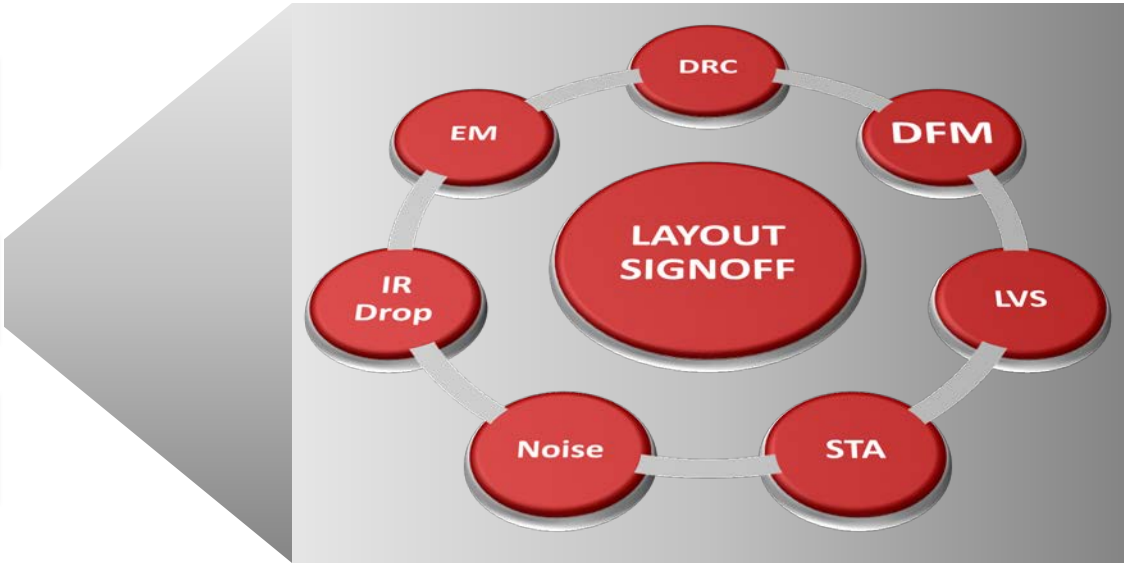


A series of <u>must pass</u> requirements before tapeout

- Typically done post-layout
- Requires iterations with layout, synthesis and even RTL
- Design convergence becomes worse at 28→14 nm
- 3rd party IP's further increase the design risk
- **<u>Too late in the flow, too much design risk</u>**



Traditional signoff no longer sufficient

RTL Signoff Emerges

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RTL

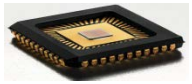
RTL SIGNOFF

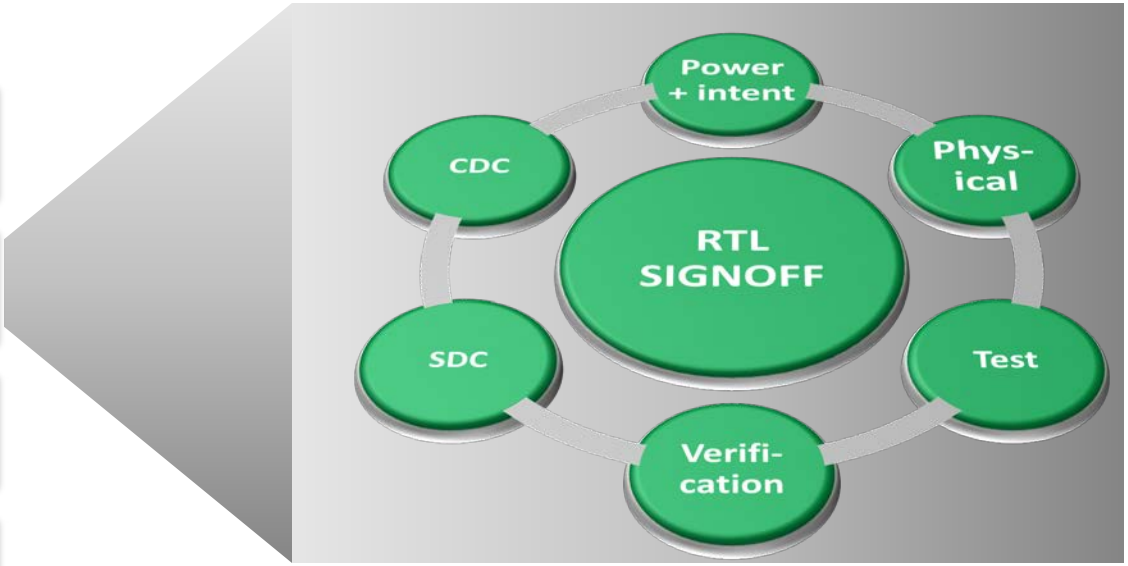
Synthesis

Layout

LAYOUT SIGNOFF

Fab





A series of <u>must pass</u> requirements before synthesis

- Does not replace, but augments post-layout signoff
- Minimize late stage surprises & iterations
- Must be applied to the entire design including 3rd party IP's
- **<u>Run times are an order of magnitude faster than post-layout</u>**

Only viable approach to address soft IP reuse

RTL Signoff Requirements

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Signoff Domain	MUST PASS Requirements
Verification	✓ **Functional coverage** signoff ✓ High quality **assertions** checked into simulation regressions
CDC	✓ **Clock, reset, data** synchronization signoff ✓ **Static** (structural + formal), **Dynamic** (simulation) signoff
SDC	✓ Complete and consistent **SDC** to synthesis ✓ **False & multi-cycle paths** fully verified
Power intent (*PF)	✓ **Power intent (UPF/CPF)** signed off ✓ Must be done **before & after insertion** of level shifters, isolation logic, …
Power	✓ Efficient **clock gating** for registers and memories ✓ RTL meets **power spec** - taking into account physical effects
Test	✓ RTL meets **stuck-at test coverage** requirements ✓ RTL meets **at-speed test coverage** requirements
Physical	✓ RTL is **congestion-free**, ✓ RTL meets **area** & **timing** targets

RTL Signoff applies to IP/blocks and full SoC

Complete Platform for RTL Signoff

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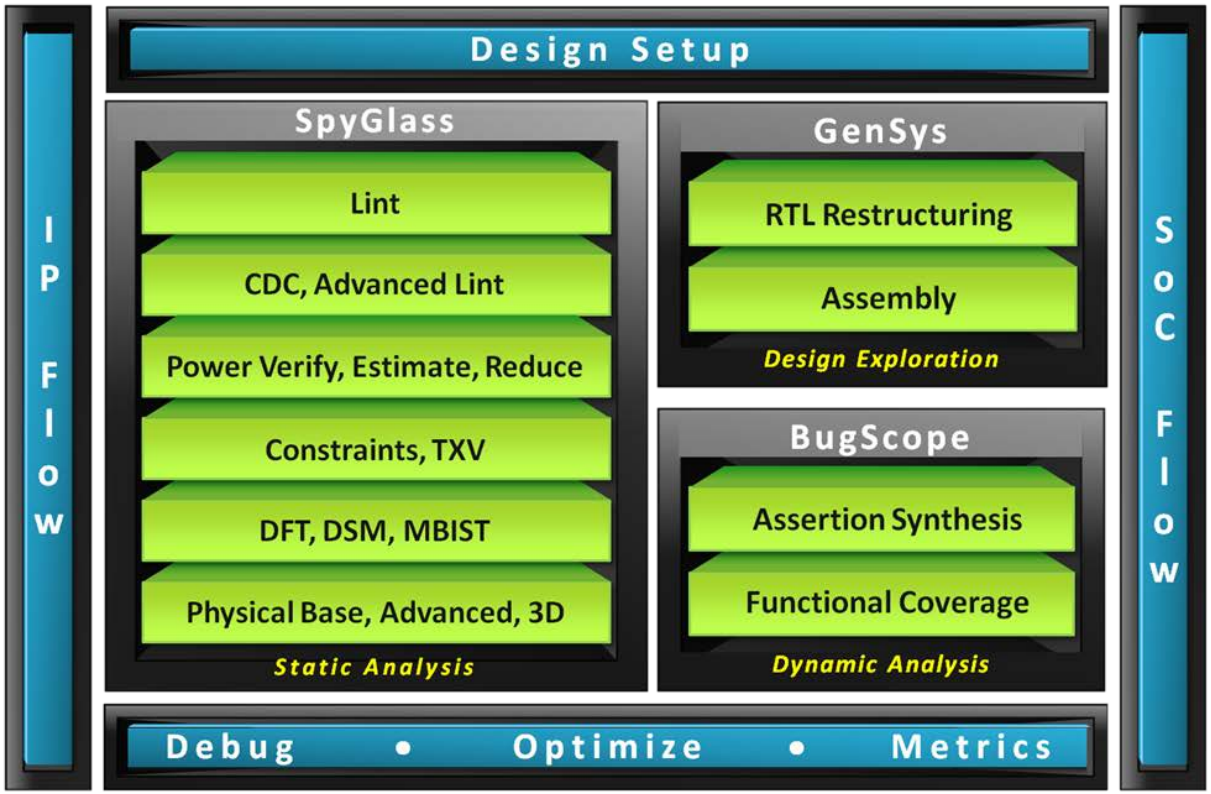
System Realization

SoC Realization

Silicon Realization

RTL Signoff™



RTL Signoff™

RTL Signoff with Atrenta

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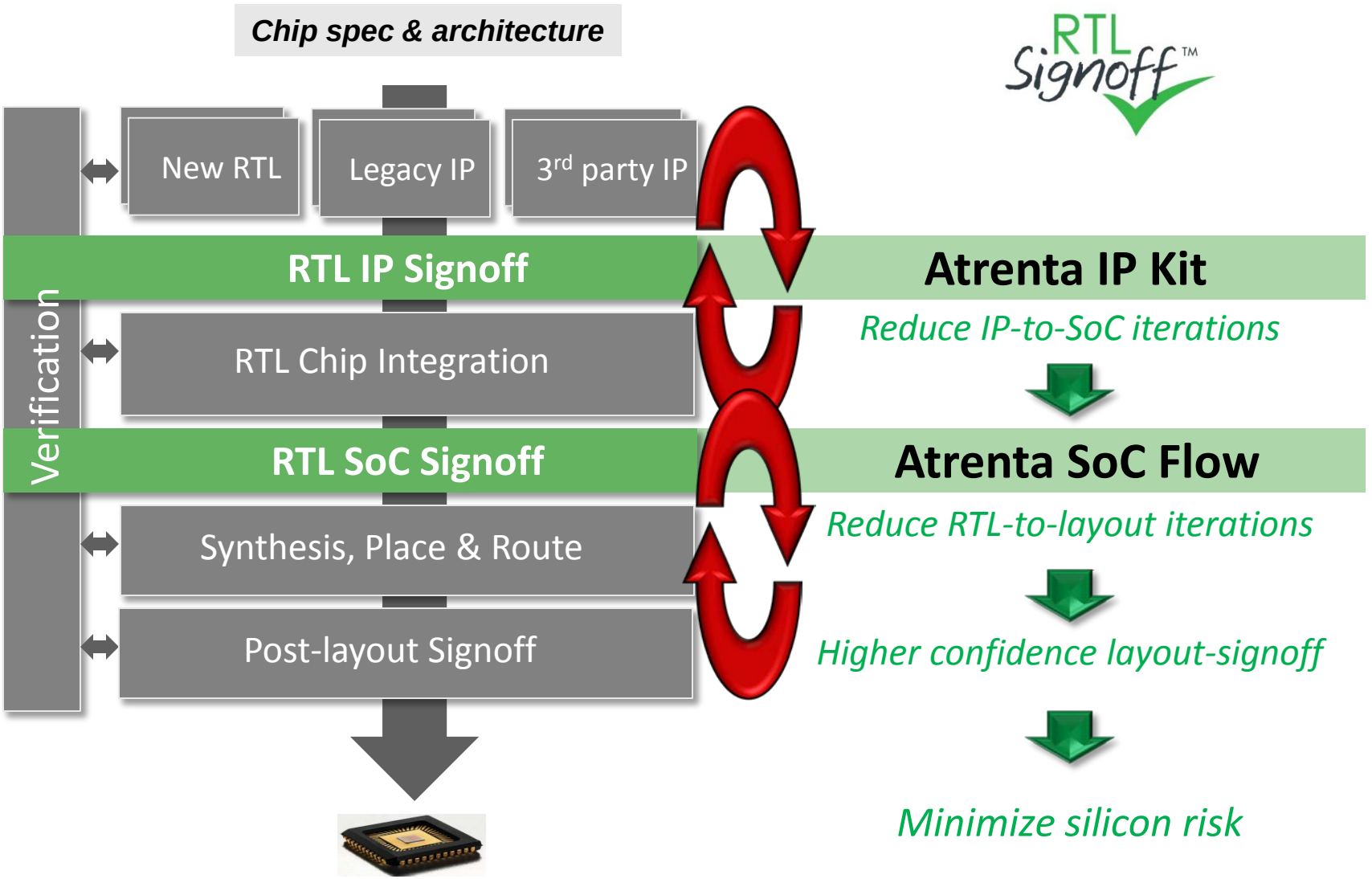

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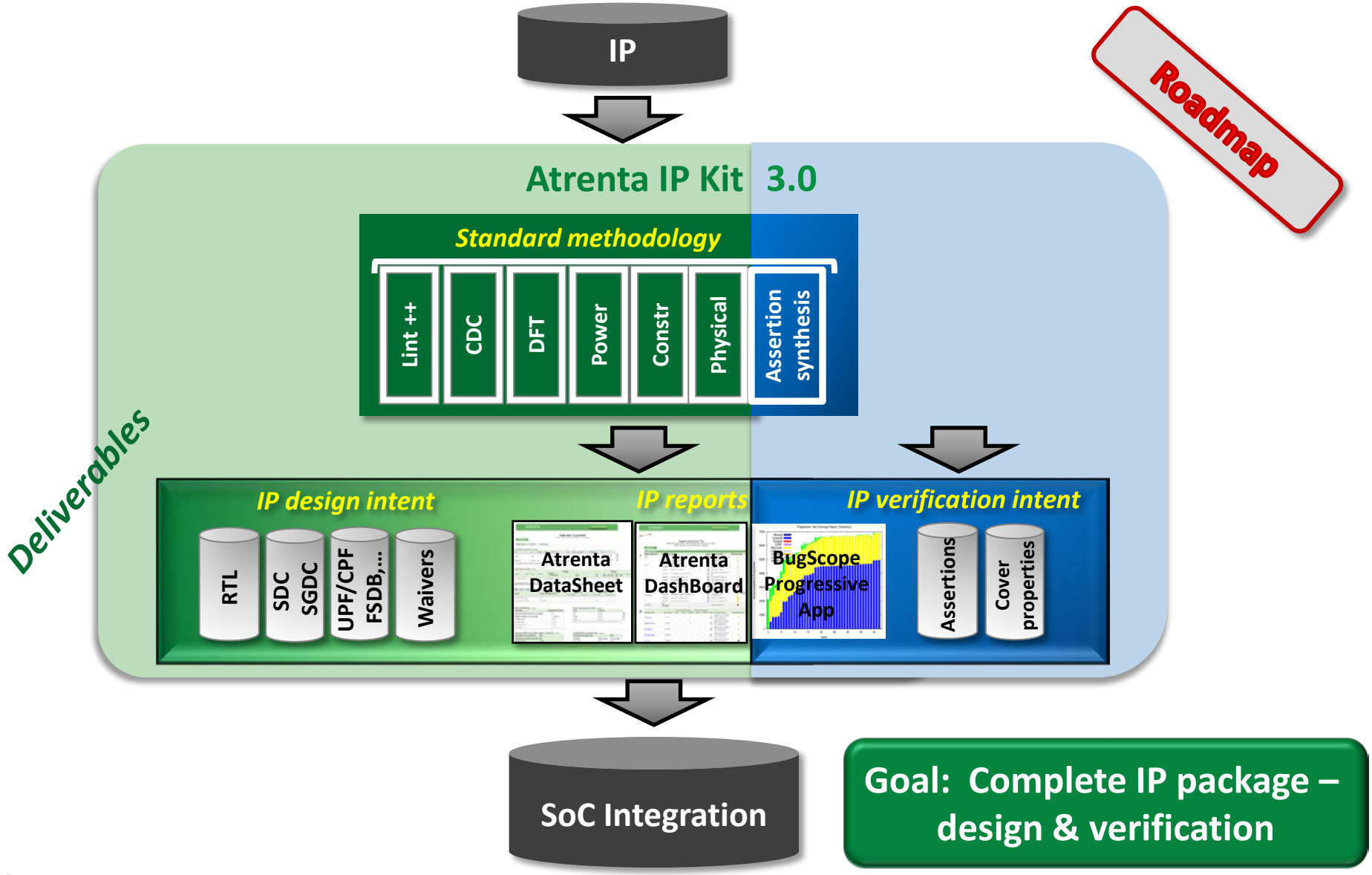
Atrenta IP Kit 3.0 – Includes Verification



Hierarchical SoC Abstraction Flow

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Design	Size [Gates]	# Blocks	Runtime [Hrs]		Memory GB		# Violations	
			Flat	Hier	Flat	Hier	Flat	Hier
Graphics chip	1.4 B	14	96	2	1300	100	> 1 M	346
Networking	155 M	12	20	0.5	300	30	6678	2
D-TV chip	110 M	26	33	1	400	50	1289	102
Mobile phone	100 M	9	8	0.5	200	40	1687	200

Billion+ gate capacity

15-50X faster

5-10X lower memory

10-100X reduction in noise

Goal:
Manage Complexity

Soft IP Reuse – The Big Picture

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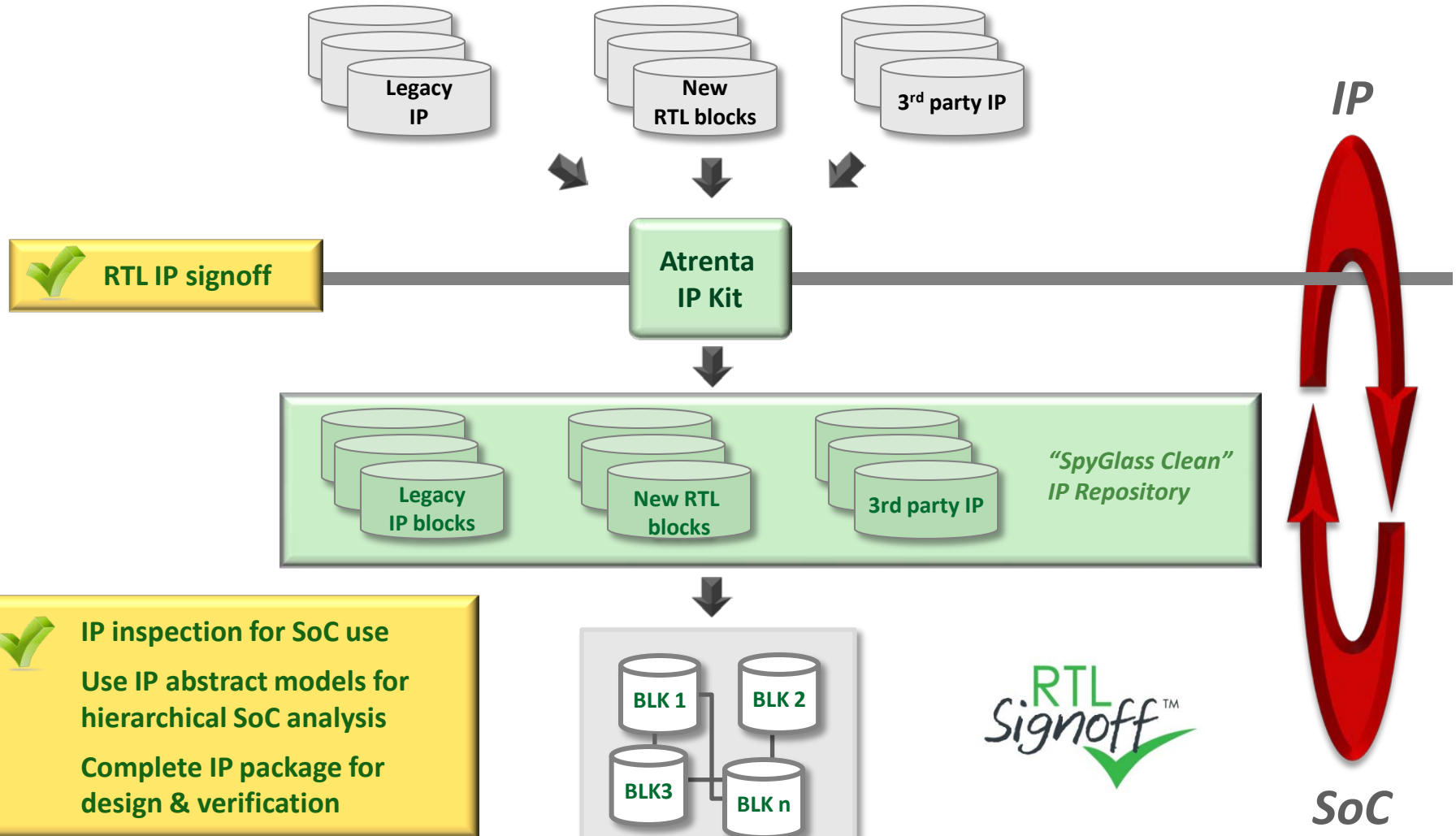

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Thank you!