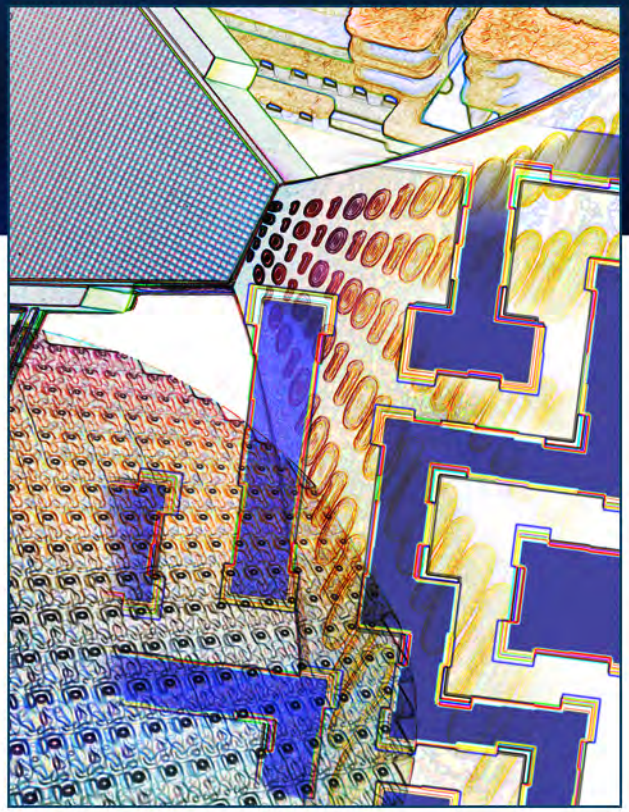


Improved Circuit Reliability / Robustness

Carey Robertson
Product Marketing Director
Mentor Graphics Corporation

Mentor Graphics®

Reliability Requirements are Growing in all Market Segments

Transportation

- Exhaustive specs/testing for reliability
- **Chips need to be robust against a number of extreme environmental factors**
- Stable platform for 10+ years

Mobile / Wireless

- Pushing the limits of low power, performance and functionality
- **Smaller nodes => smaller oxides**
- Heterogeneous on-chip content drives higher probability of latch-up, cross-power domain issues

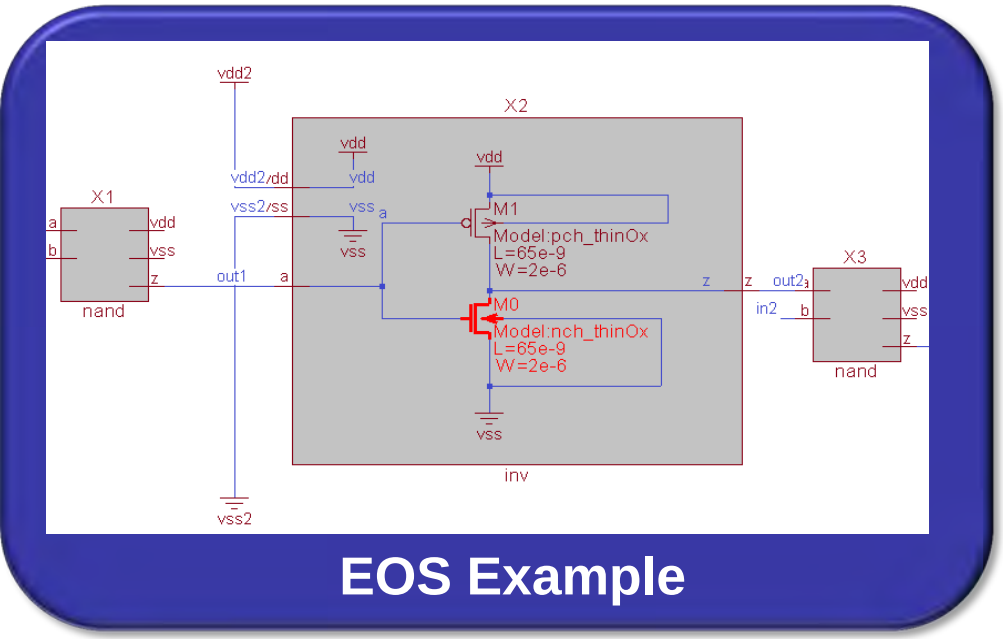
General CPU / Server Farms

- Aggressively pursuing smallest process node, performance and functionality. **.**
- Design complexity very high. Often an SoC with many (internal) IP providers. Higher probability of latch-up, cross-power domain issues

Limitations of Traditional Verification

Circuit Failure due to Electrical Overstress (EOS)

- Thinner-oxide ➡ lower voltage ➡ less power
  - — Some power domain design errors lead to oxide breakdown and failure over time. NBTI (PMOS), HCI (NMOS), SBD
- Complex Management of *bulk* and *power* pins
  - — IP blocks may have internal global signals



EOS Example

LVS:

Schematic Matches Layout X

Schematic Correct ?

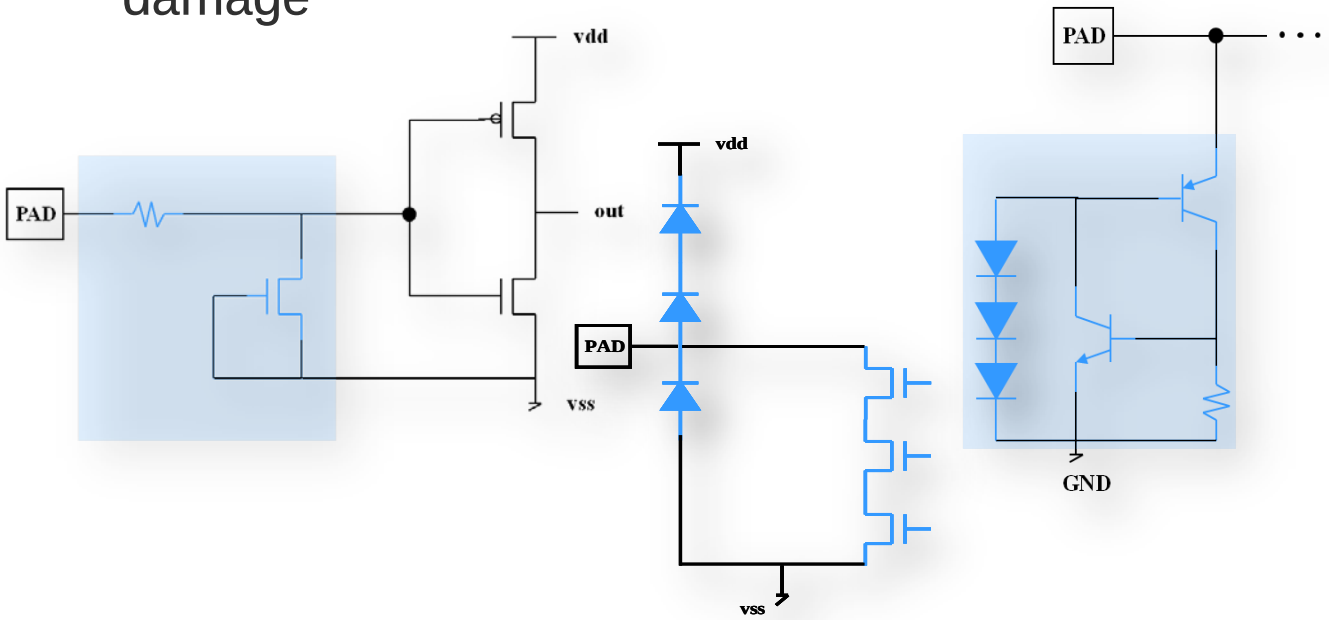
Simulation:

Static Timing X

Circuit Simulation X

ESD Design Rules

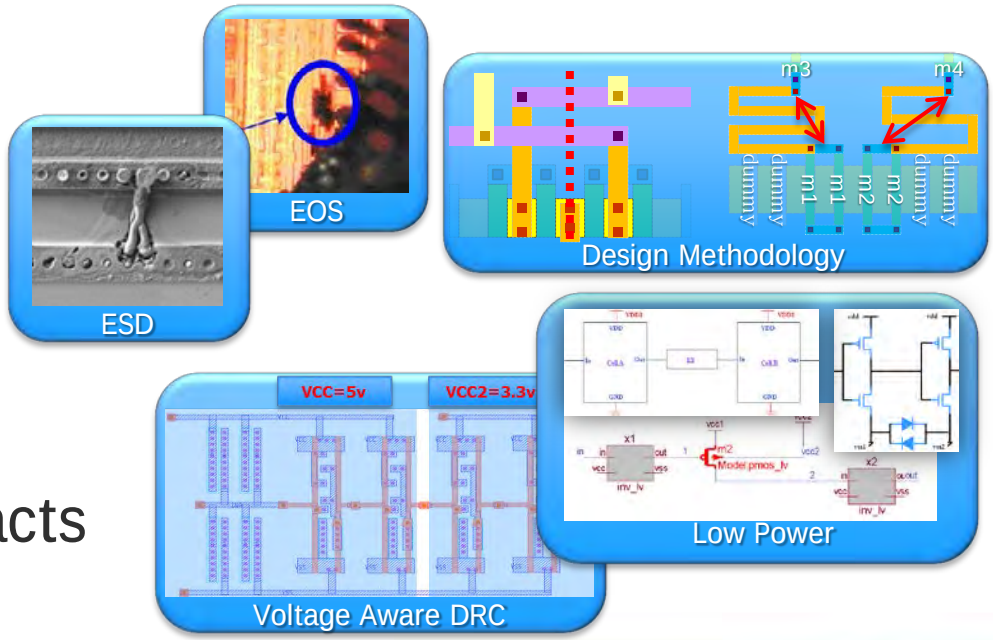
- Electrostatic discharge (ESD) causes severe damage to ICs
- Several protection schemes have been proposed to mitigate this damage



Checking for proper ESD protection circuits is needed for reliable design

A Reliability Verification Platform

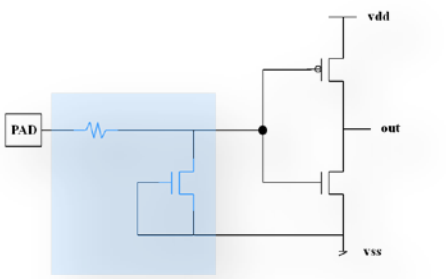
- Calibre PERC provides a robust platform for circuit reliability verification
- Not just a point tool solution
  - A system view of how design elements interact is needed
  - Used throughout the design flow: schematic, layout, final verification
- Typical application areas
  - ESD
  - EOS
  - Voltage-aware DRC
  - Low/Multi-power designs
  - Latch-up
- Understand IC layout impacts on device performance

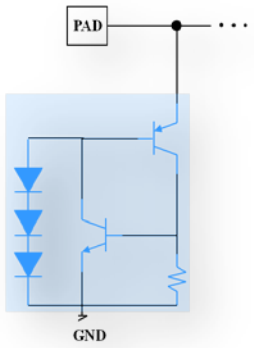


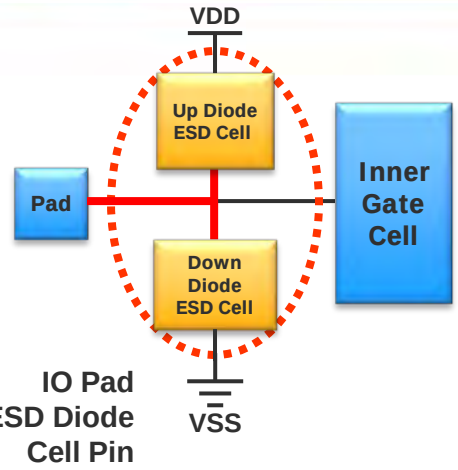
ESD Verification

Device and Cell Based Verifications

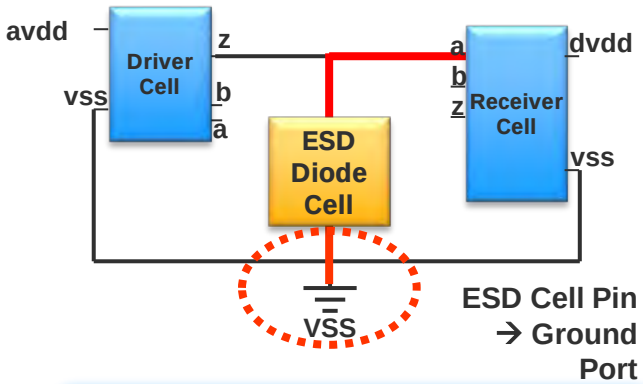
- Topological and Layout based checks
  - Reference cell names
  - Verify signals crossing multiple power domains
  - Addresses reliability concerns / EOS
- Layout centric verification with P2P, CD and DRC
  - Logic Driven Layout (LDL)
- User defined checks and feedback







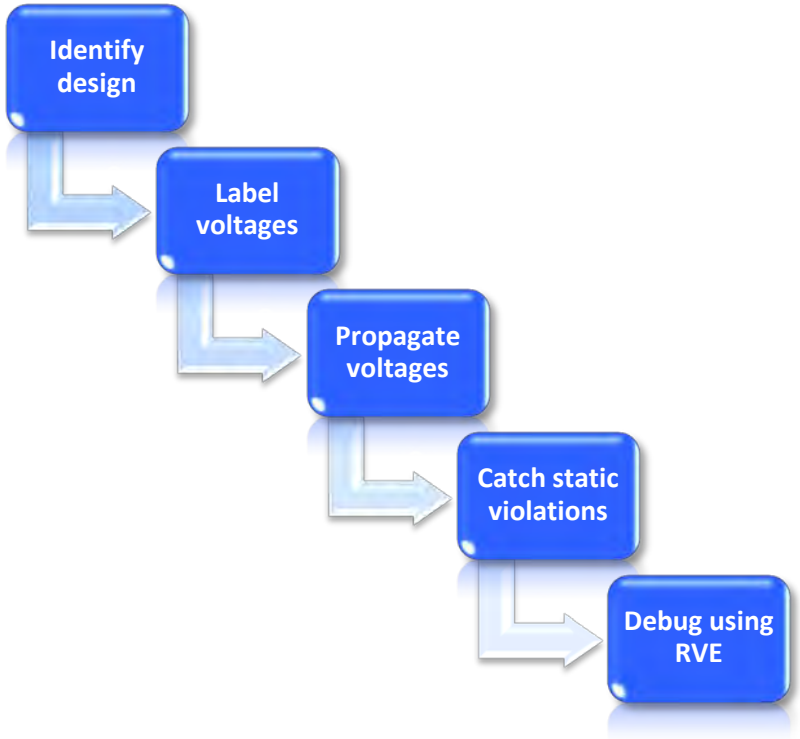
Current density simulation

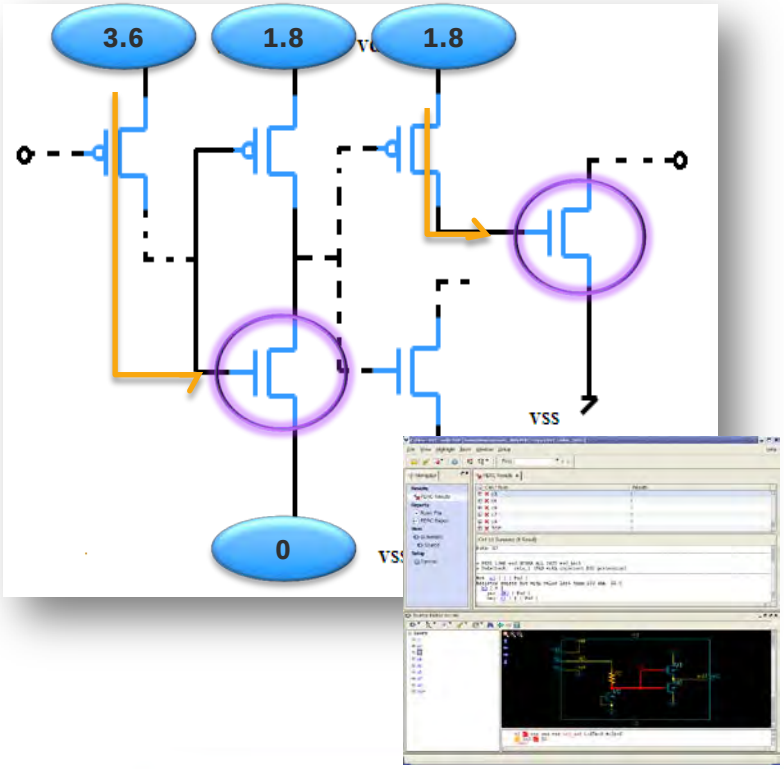


P2P resistance simulation

Understanding EOS without Simulation
Voltage Propagation

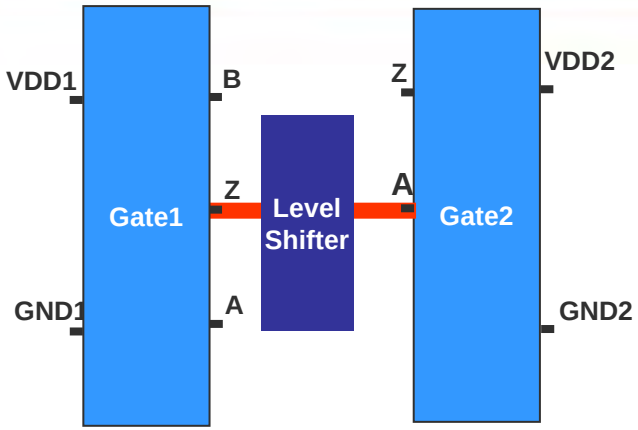
- EOS has historically been one of the leading causes of integrated circuit failures, regardless of the semiconductor manufacturer
- The result of an EOS event can range from no damage or degradation to the IC up to catastrophic damage where the IC is permanently non-functional

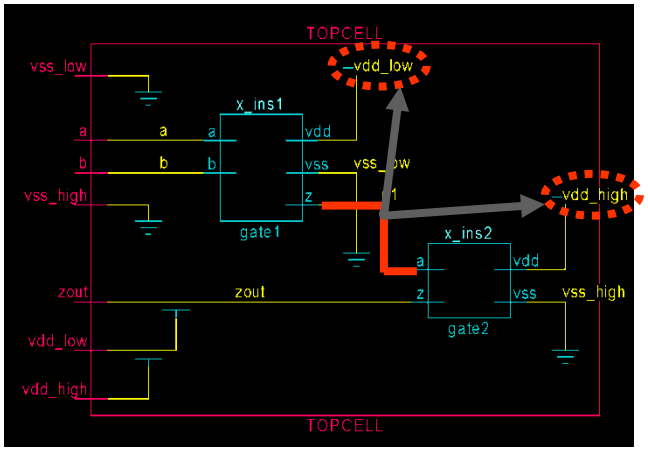




Power Domain Checking

- Multi-power verification requires system knowledge
- Tracking of large numbers of domains
- PERC identifies power regions
  - Verifies appropriate level-shifting circuitry

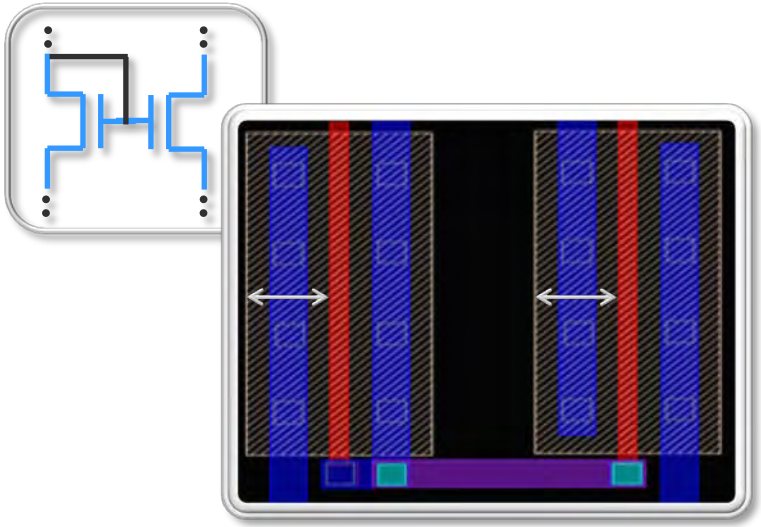




UNIFIED POWER FORMAT

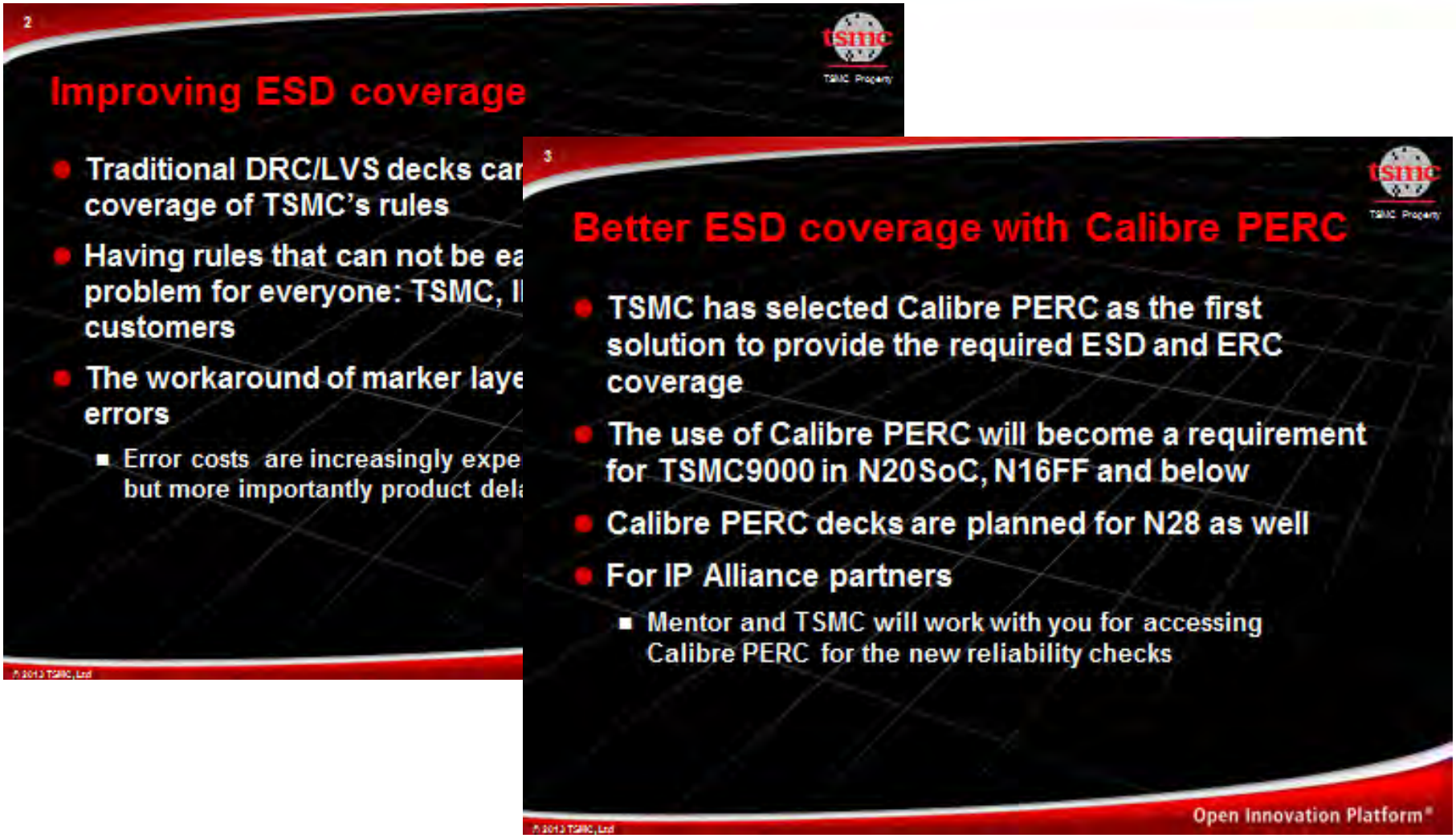
Post-Layout Verification
Topology-based Geometrical Checking

1. Search for the topology
2. Perform the geometrical measurement
3. Compare vs. a constraint & issue violations



Constraint Violation:
od_ext1 ≠ od_ext2
od_ext < 0.1µm

Partnering with TSMC



Reliability Rules Are Complex

- ESD/Latch-up Rules
  - 35% of ESD and latch-up rules “un-checkable” with standard EDA tools
  - The other 65% of rules need additional manually-placed marker layers

TSMC9000 with Calibre PERC

- Focus on three categories of rules
  - Example checks shown, final determination underway

	Rule Description
IO Cells	most of rules in DRM ESD/LUP kit are applicable
IP with multiple power domains	CDM rules are applicable
analog IP	No dangling input / output port
	MOS gate can't directly connect to power
	MOS can't directly connect to I/O port
	for logic gates in two different power domains, there must be appropriate protection
	MOS connect to pad through resistor can't connect it's gate directly to power or ground

- Analog IP here, includes Interface IP, mixed signal, etc.
- Other categories explored with additional IP

Industry Support
Customer Adoption / Industry Validation

Mentor Graphics

FOR IMMEDIATE RELEASE News Rel

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Mentor Graphics and TSMC Collaborate to Improve and Exp IC Physical Verification Offering

Calibre PERC Kit for N20 Now Available

WILSONVILLE, Ore., May 28, 2013—Mentor Graphics Corp. (NASDAQ: MEN announced significant achievements in its continued collaboration with TSMC on 2 verification kit optimizations. This joint effort has reduced Calibre® nmDRC™ 20 runtimes by at least a factor of 3X and memory requirements by 60% compared to kits released last year. In addition, Calibre PERC™ N20 design kits are now available to TSMC customers as part of the companies' ongoing collaboration for IC reliability improvement. The collaboration will continue as mutual customers ramp their releases of N20 production designs, with the goal of maintaining rapid turnaround on full-chip signoff runs for the largest SoC designs in the industry.

TOWERJAZZ Mentor Graphics

NEWS ANNOUNCEMENT ***FOR IMMEDIATE RELEASE***

TowerJazz Releases Rule Decks for Advanced ESD and Power Domain Checking Using Mentor's Calibre PERC

MIGDAL HAEMEK, Israel and WILSONVILLE, Ore., March 4, 2013 – TowerJazz, the global specialty foundry leader, has announced the Mentor®'s Calibre® PERC™ rule decks are now available for TowerJazz customers to perform circuit reliability verification for its latest 0.18 micron products, including highly customized electrostatic discharge (ESD) and power management circuit checks. Many of these checks have been automated for the first time by taking advantage of the Calibre PERC product's unique ability to combine schematic (netlist) and physical layout information

Winner of the Customers' Choice Award at TSMC's 2011 Open Innovation Platform® Ecosystem Forum

Electronic Products Magazine 2009 Product of the Year

Mentor Graphics

THANK YOU!