Best Practices of SoC Design

Electronic Design Process Symposium 2014

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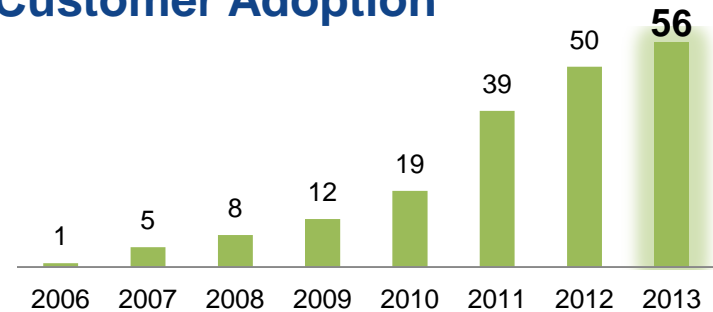
Arteris Snapshot

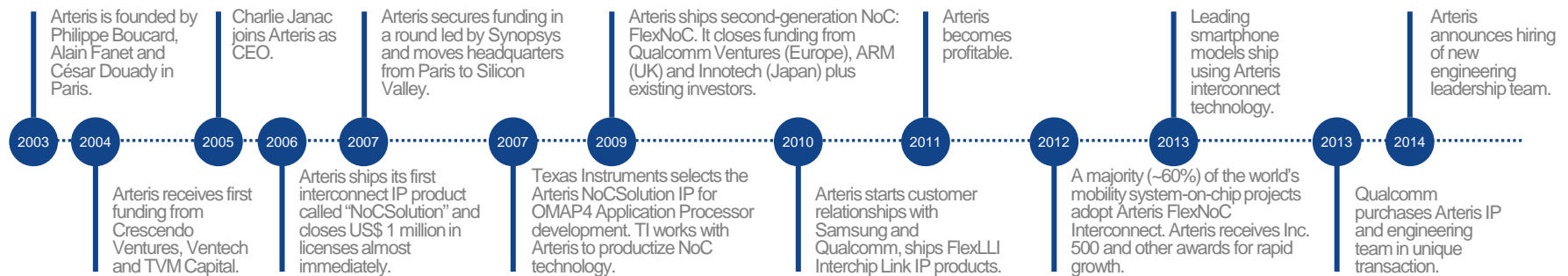## Founded in 2003; headquarters in Silicon Valley

Awards

Inc. 500

Deloitte. Technology Fast 500

Fast Private Awards 2012 Honoree

WORLD ECONOMIC FORUM

ACE AWARDS 2012 FINALIST — EETimes EDN

Customer Adoption

Year	Value
2006	1
2007	5
2008	8
2009	12
2010	19
2011	39
2012	50
2013	56

Timeline of Key Events*

2003 — Arteris is founded by Philippe Boucard, Alain Fanet and César Douady in Paris.

2004 — Arteris receives first funding from Crescendo Ventures, Ventech and TVM Capital.

2005 — Charlie Janac joins Arteris as CEO.

2006 — Arteris ships its first interconnect IP product called "NoCSolution" and closes US$ 1 million in licenses almost immediately.

2007 — Arteris secures funding in a round led by Synopsys and moves headquarters from Paris to Silicon Valley.

2007 — Texas Instruments selects the Arteris NoCSolution IP for OMAP4 Application Processor development. TI works with Arteris to productize NoC technology.

2009 — Arteris ships second-generation NoC: FlexNoC. It closes funding from Qualcomm Ventures (Europe), ARM (UK) and Innotech (Japan) plus existing investors.

2010 — Arteris starts customer relationships with Samsung and Qualcomm, ships FlexLLI Interchip Link IP products.

2011 — Arteris becomes profitable.

2012 — A majority (~60%) of the world's mobility system-on-chip projects adopt Arteris FlexNoC Interconnect. Arteris receives Inc. 500 and other awards for rapid growth.

2013 — Leading smartphone models ship using Arteris interconnect technology.

2013 — Qualcomm purchases Arteris IP and engineering team in unique transaction.

2014 — Arteris announces hiring of new engineering leadership team.

*Timeline graphic courtesy of World Economic Forum

Arteris — THE NETWORK-ON-CHIP COMPANY

Active Customers

+9 Unannounced Customers

IP is key to SoC assembly success
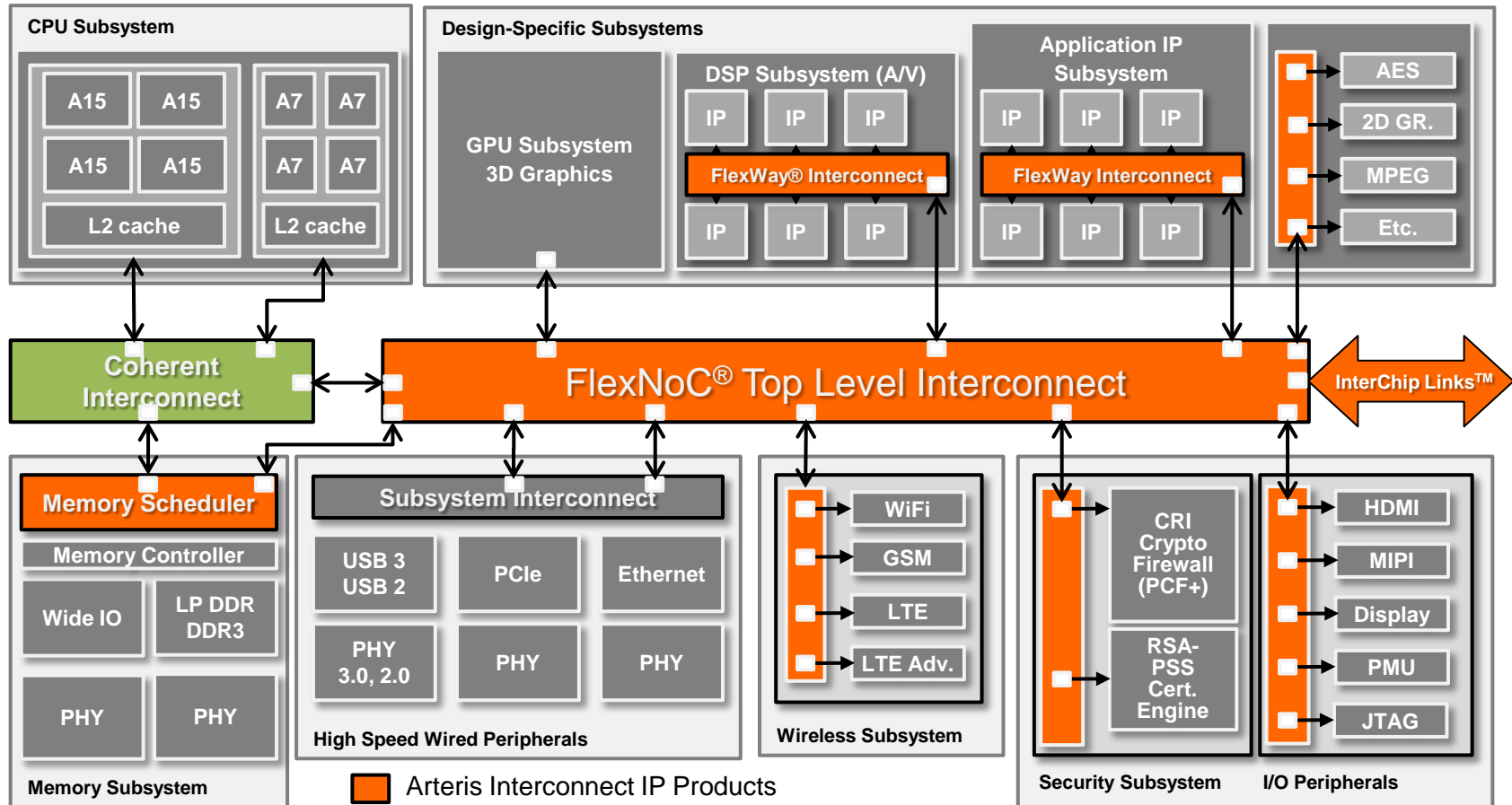
Accelerate TTM by 9 to 12 months

Standard TTM is 18-24 Months

Architecture — Interconnect Design — Interconnect Verification — SoC system Verification

IP Design — IP Integration — Physical Design — Platform Debug

18 – 24 months

Actual Customer Experience with Arteris NoC

FPGA Emulation Software Development

1-2 days iteration

9 – 12 months

Arteris™
THE NETWORK-ON-CHIP COMPANY
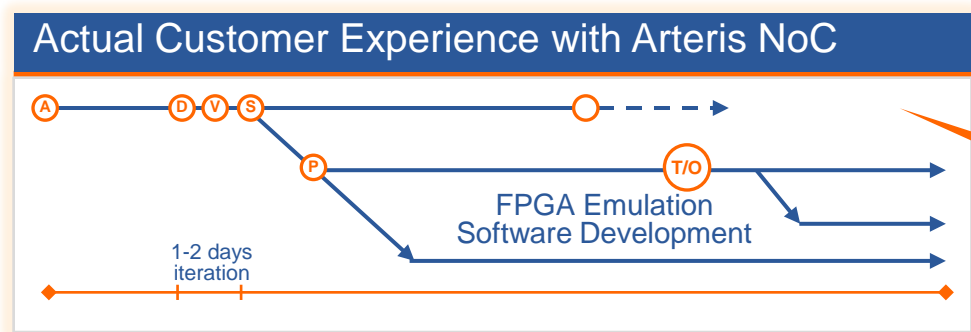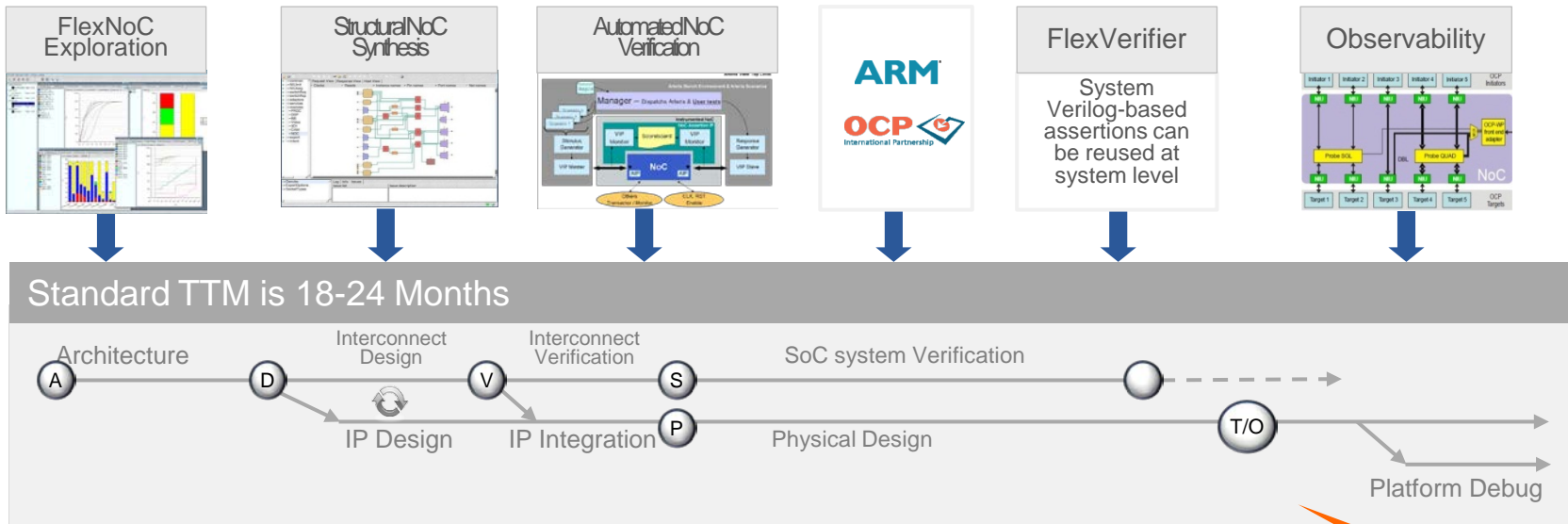
Best Practices

Lessons learned from the most successful SoC companies

1. Internally-develop <u>only</u> your most important IP

2. Create a <u>corporate</u> "IP library"

3. Develop <u>corporate</u> design and verification methodologies

4. Use a <u>platform</u> and derivatives approach

1. Internally-develop __only__ your most important IP

Benchmark yourself

Cost-benefit analysis

Opportunity cost

Politics

Ego

DISCIPLINE!

2. Create a corporate "IP library"

Document & categorize
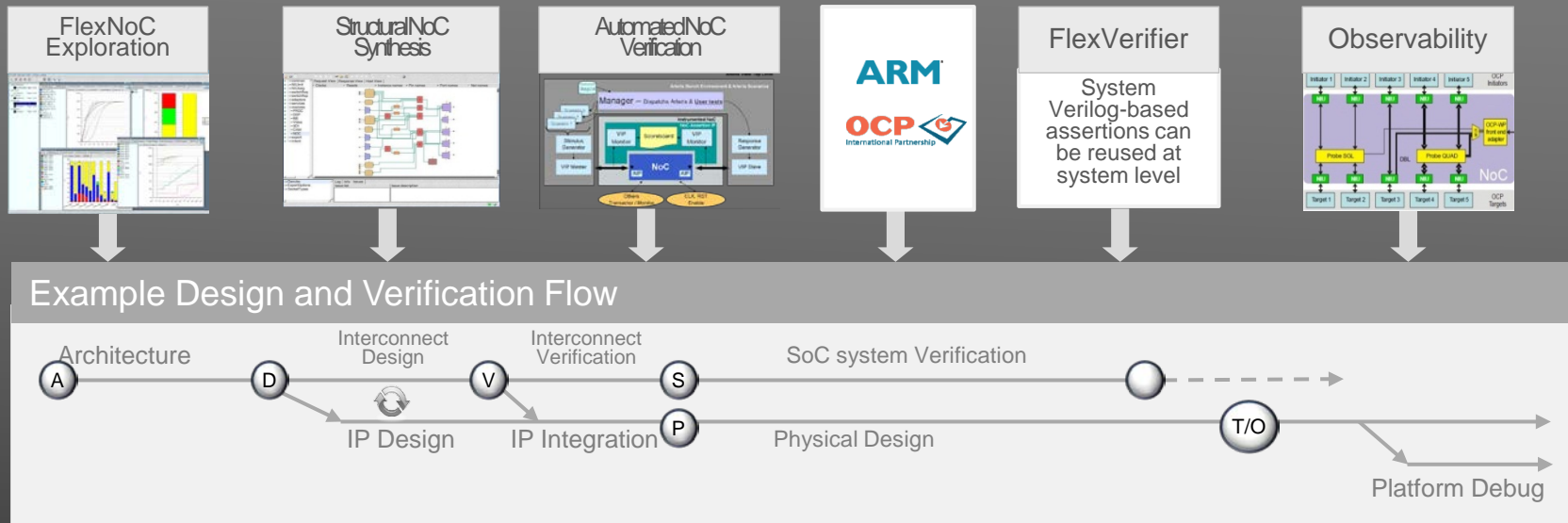
Know your rights

Documentation & Training

Accessibility

Software

Searchable

Best practices

SERVICE!

3. Develop <u>corporate</u> design and verification methodologies

Example Design and Verification Flow
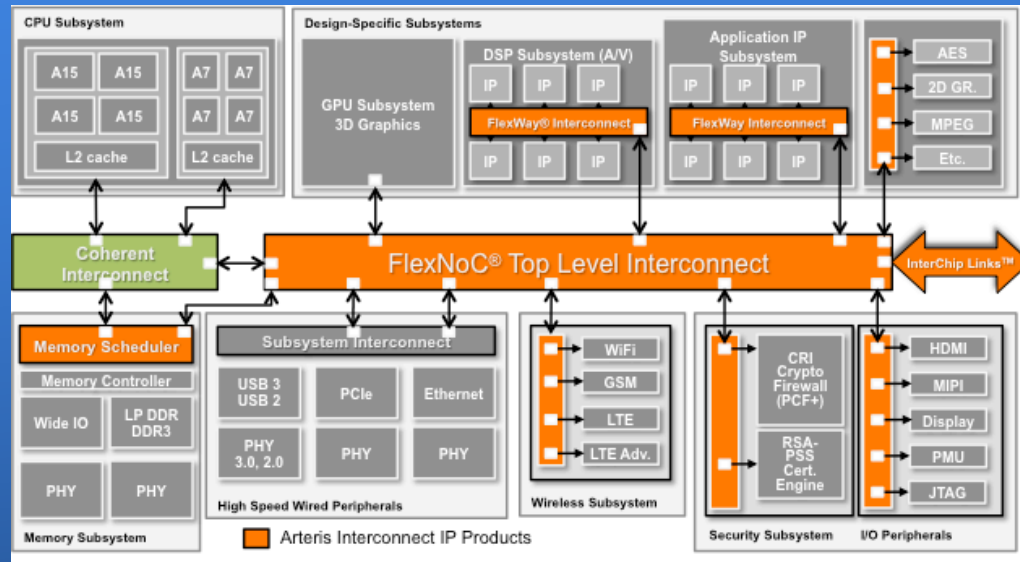

Global (vs. local) learning & optimization

Optimal tool and IP usage

Encourages more IP reuse

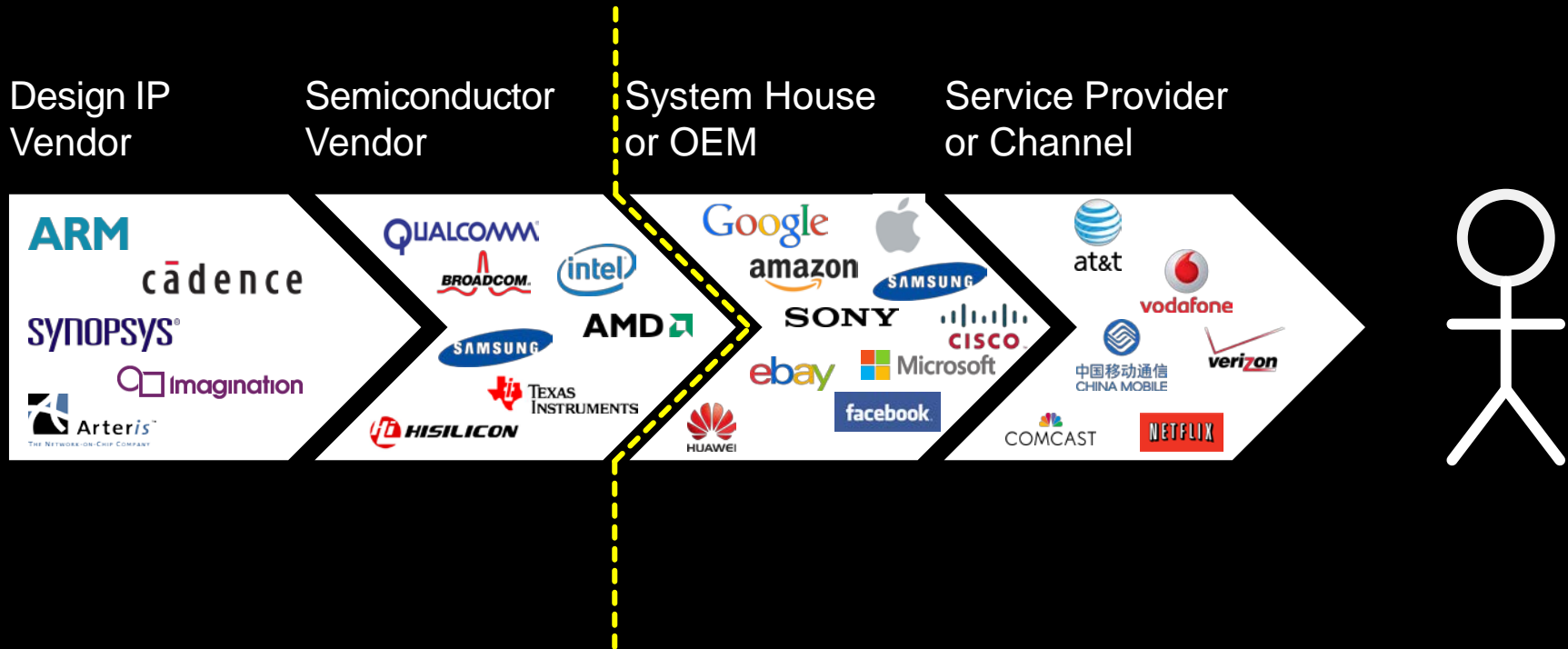# 4. Use a **<u>platform</u>** and derivatives approach

Flexibility to target more markets at reduced cost
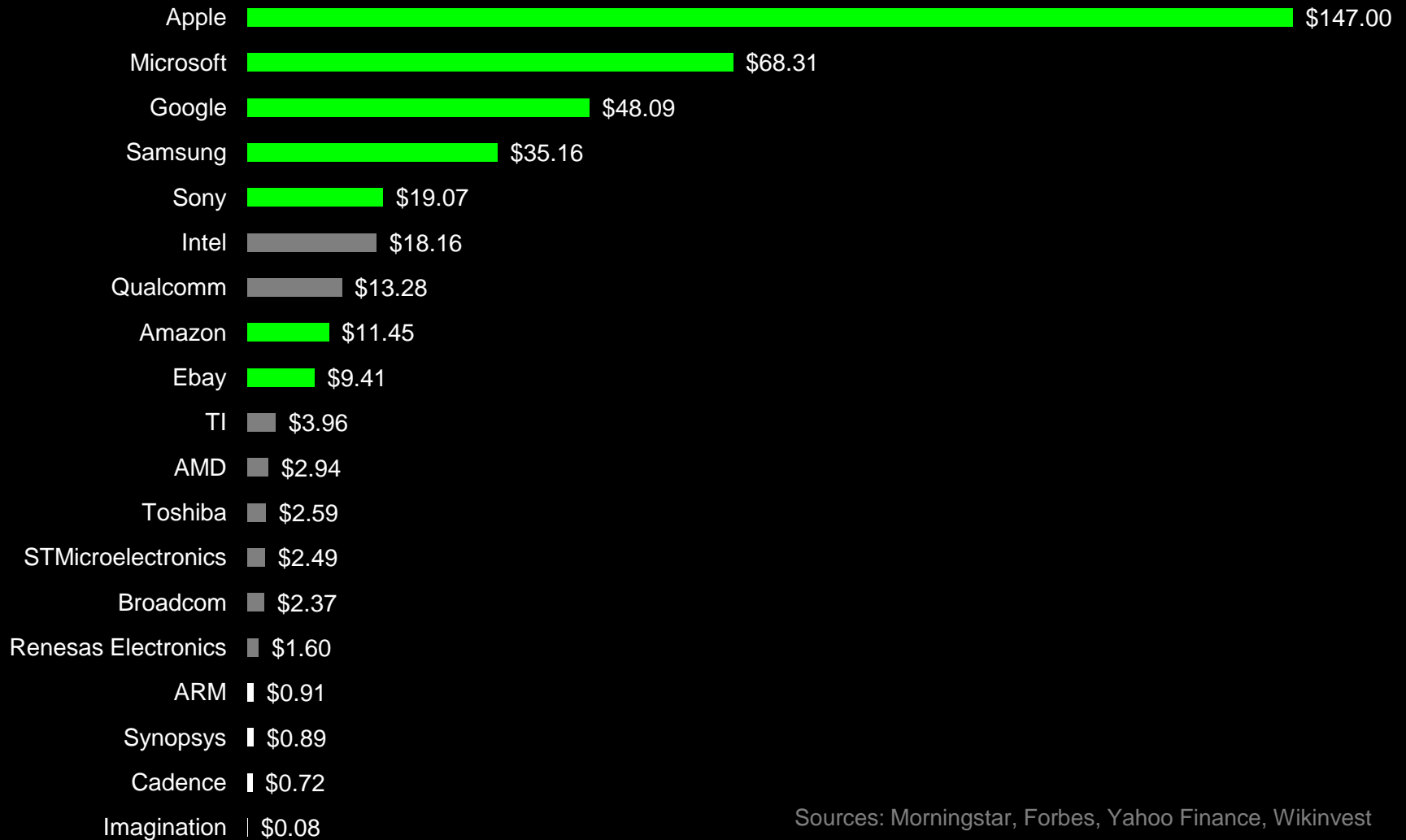
Speed to respond to threats and opportunities

More IP reuse to reduce cost

Semi vendors aren't the only one who make chips!

Design IP Vendor

Semiconductor Vendor

System House or OEM

Service Provider or Channel

Cash on Hand

Systems Houses, Semiconductor and Design IP Vendors, Billions ($B)

Company	Cash ($B)
Apple	$147.00
Microsoft	$68.31
Google	$48.09
Samsung	$35.16
Sony	$19.07
Intel	$18.16
Qualcomm	$13.28
Amazon	$11.45
Ebay	$9.41
TI	$3.96
AMD	$2.94
Toshiba	$2.59
STMicroelectronics	$2.49
Broadcom	$2.37
Renesas Electronics	$1.60
ARM	$0.91
Synopsys	$0.89
Cadence	$0.72
Imagination	$0.08

Sources: Morningstar, Forbes, Yahoo Finance, Wikinvest

Efficient SoC assembly & IP reuse must become core skills for all semi vendors

○ SoC assembly is more critical to success than creating custom IPs

○ Best practices can enable semi vendors to make more and better chips, more efficiently

○ Semi customers are becoming competitors as chip design "democratizes"

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Thank YOU