IP Qualification and Verification

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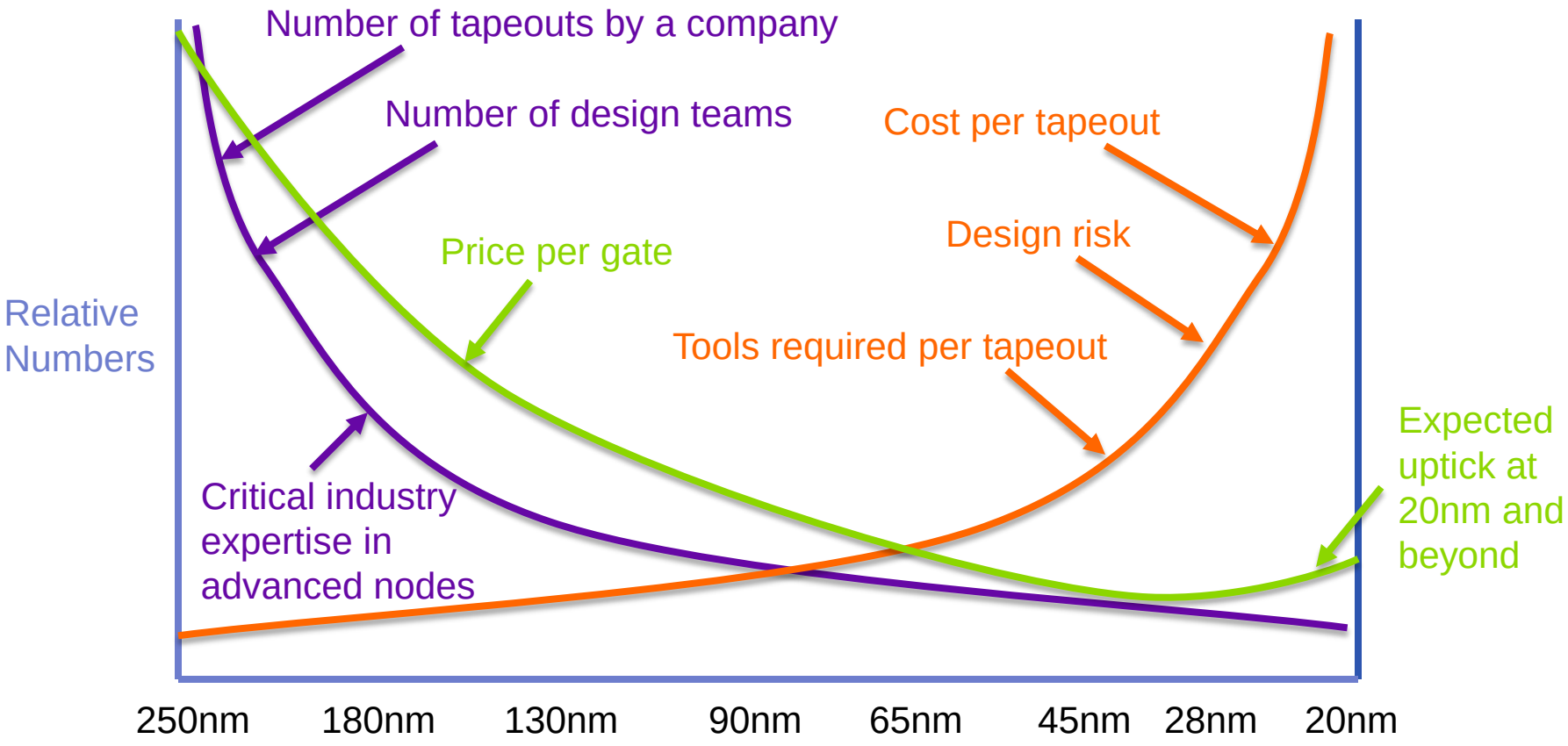
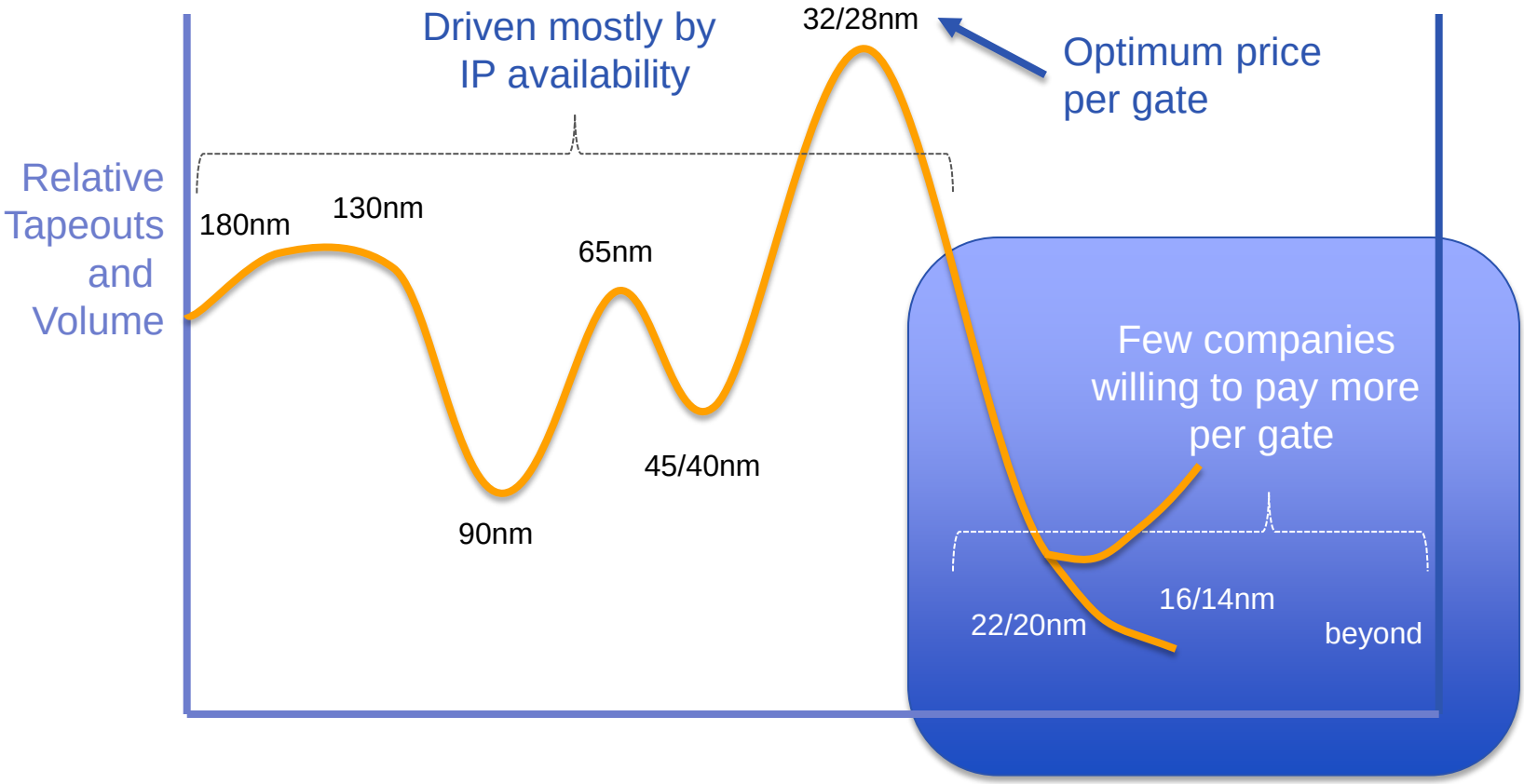
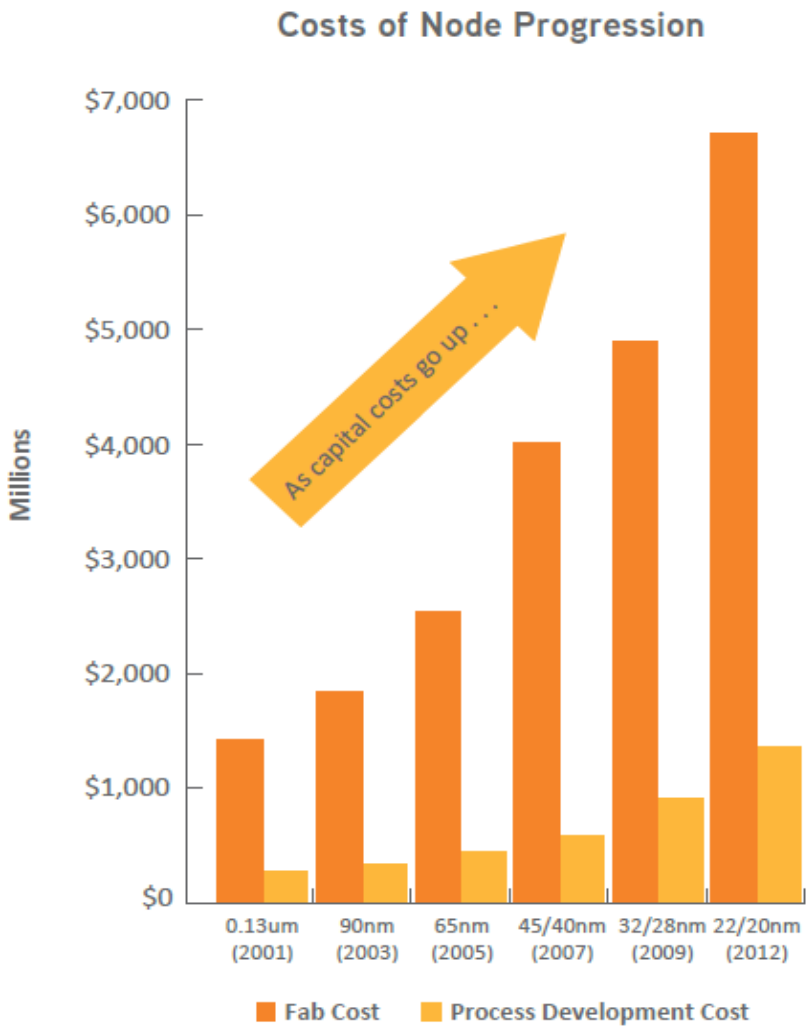
Increased Cost with Advanced Manufacturing

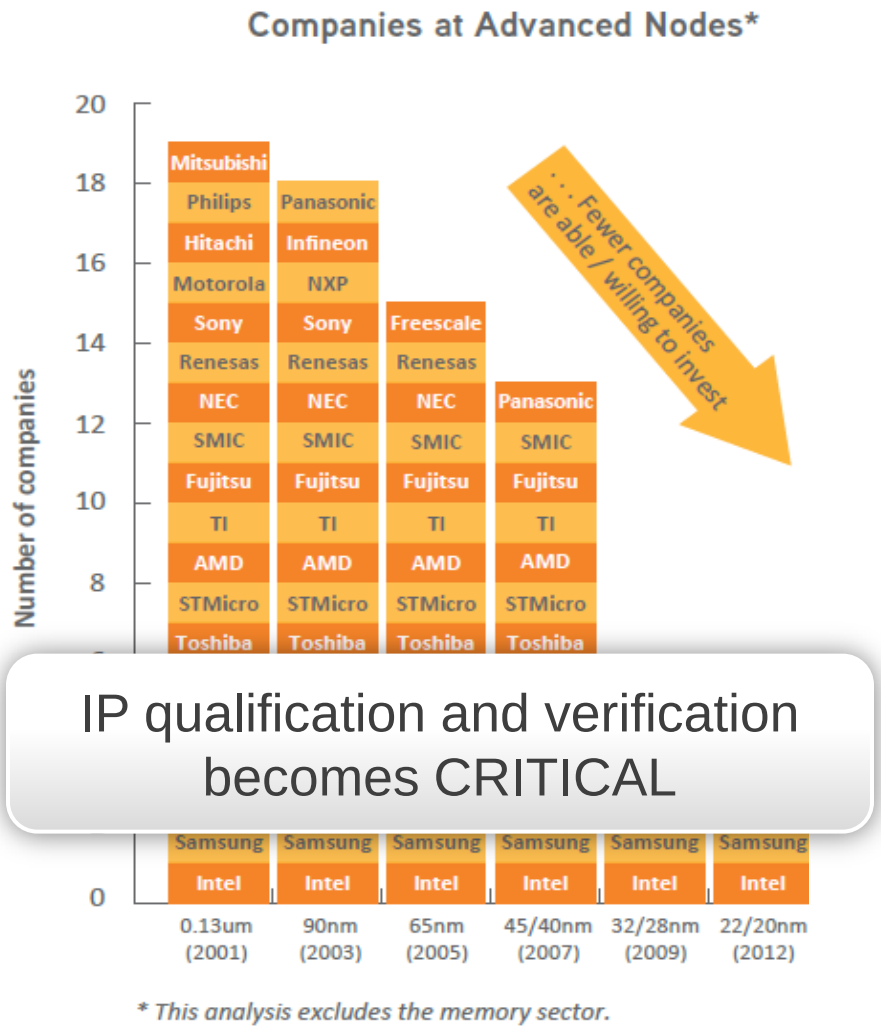


IP Availability
Critical to Moving to The Next Node



The Trends Are Clear

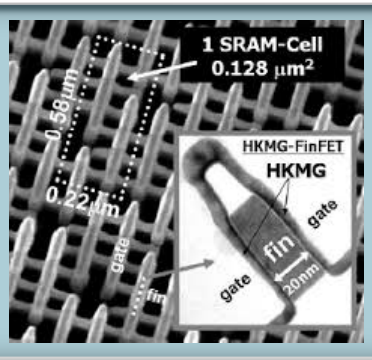




IP qualification and verification becomes CRITICAL

Sources: McKinsey & Company, ATREG

Design For Manufacturing and Yield at the Chip Level

Design	Repair Reduce Failures Parametric Yield Loss	• Redundancy • Test/diagnostic logic • Planarity of metals, litho-friendly design, redundant vias, wire spreading • On-chip variation guard banding or detect/adjust
Manufacturing		• 3D transistor • Self-aligned double patterning and self-aligned quadruple patterning • Germanium fin fabrication • Carbon-doped silicon source/drain
Packaging	Eliminate Shorts Minimize Warpage Minimize Delamination Stresses	• Bond-wire pattern • Lead-finger design and metal content balancing in substrate • Layout of silicon chips on a die pad in a multichip module
Reliability	ECC EMIR TDDB	• Time-dependent gate oxide breakdown (TDDB) • Model and compensate for local thermal effects • Error detection and correction • Compensate for line-edge roughness (LER) • Appropriate device length to meet reliability under OD conditions

Design Considerations at Advanced Technologies

Memory is dominating the chip

Need for increased bandwidth driving more interconnect

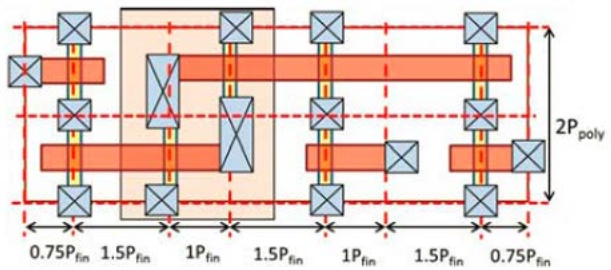
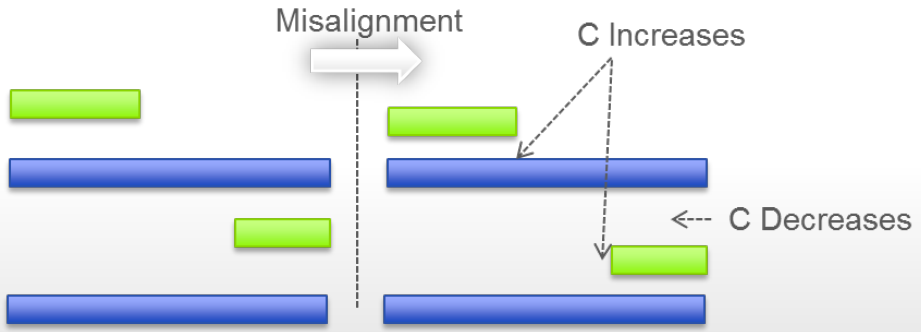


Figure 6: Layout of 8T FinFET SRAM.



Source: ITRS

Integrating more transistors, higher population requires moving from 3 sigma to 5/6 sigma and even 7 sigma!

- Run Monte Carlos simulations with sample size in the billions -> Impossible to do
- New tools emerging with proprietary algorithms to predict 5/6 sigma with sample size in the thousands

- As the number of bits in the memory increases, the number of redundant elements must increase to maintain the same level of yield
- Margining for variation
- More transistors, increased heat, EMIR analysis
- Double patterning – design challenges and LPE (interconnect is not scaling)

A Balancing Act…

- Additional time to plan, execute, & correct
  - Redundancy
  - Test/Diagnostic Logic
  - Planarity of Metals, litho-friendly design, redundant vias, wire spreading
  - On-chip variation guard banding or detect/adjust
- Additional EDA tools

Design For Yield

Bridging the Gap Between Designer and Foundry

Designer

- Intimately involved
- Chooses optimal trade-off in yield versus PPA that results in choices for specific design parameters, including transistor widths and lengths

Foundry

- Implements design for yield (DFY)
- Establishes and shares best practices and techniques to manage sub-nanometer effects to improve yield and also manufacturability

Improving the design both to achieve higher yield and to increase the performance of the devices that can be achieved for a given process

Addressing co-optimization issues during the design phase means reaching out to all the ecosystem players

Design For Yield

Bridging the Gap Between Designer and Foundry

IP Providers

- Need to provide fully validated IP to their customers
- Use model is critical because it is quite common for IP to be “abused” in a way or mode that the IP vendor never expected
- Need standardized quality metric
- The “clean” IP can then be used with more confidence
  - ✓ Power
  - ✓ Clock domains
  - ✓ Testability
  - ✓ Physical

Design-Manufacturing Co-Optimization

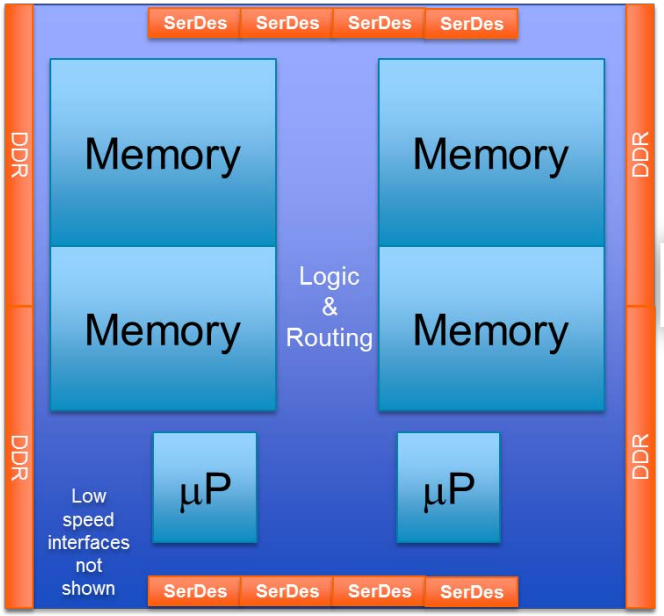
- "Design-manufacturing co-optimization" is dependent on:
  - Quality of information available
  - Effective feedback loop that involves all the stakeholders in the entire supply chain

Sharing design data, process data, test failure diagnosis and field failure data

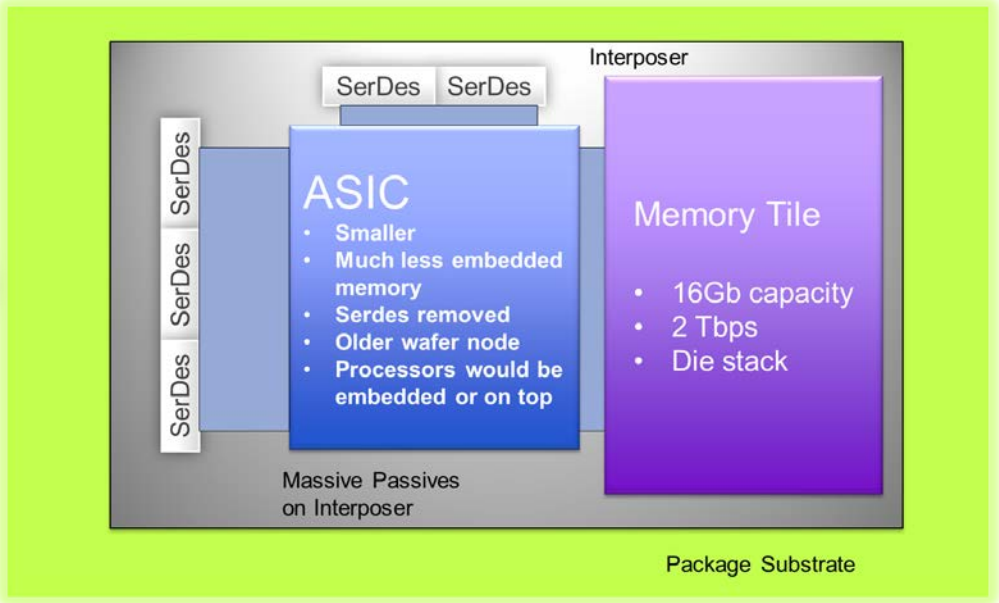
Another Option to Balance Cost

2.5D/3D

Traditional ASIC



2.5D Implementation



- Partition the IP
- Stretch out 90-28nm life
- Adequately tested – “known good die”
- Methodology for integration

$$Y = e^{(-AD)}$$ **(Poisson Model)**

A = Area of the chip
D = Defect Density

$$Y = Y_{ASIC} + Y_{Mem\ Tile} + Y_{SerDes} + Y_{N}$$

We're In This Together

- Costly and intricate manufacturing as we move past 28nm
- Challenging lithography and new EDA tools
- Need to work together – design, EDA vendors, IP vendors, foundries
- New emerging solutions to extend existing IP and technology have new challenges

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