

# Delivering IP the Way Chip Designers Want

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Monterey, CA  
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# Big trends are driving market growth

## Mobility

250M+ tablets in 2014



## Internet of Things

50B devices by 2020



## Cloud Computing

3.3 ZB traffic with 25% CAGR



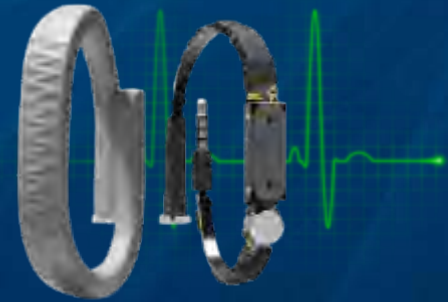
Sources:

[idc.com](http://idc.com)

[cisco.com](http://cisco.com)

[marketsandmarkets.com](http://marketsandmarkets.com)

# Great opportunities for creative technology



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# Challenges



# Incredible pace of innovation



Samsung photos courtesy of <http://www.pcmag.com/slideshow/story/309047/samsung-s-smartphone-history-from-zero-to-galaxy-s4/10>  
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# Increasing time-to-market pressures

1st June 2007



3G July 2008

3GS June 2009

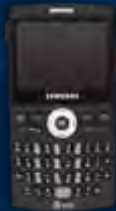
4 June 2010

4S Oct. 2011

5 Sept. 2012

5S 5C Sept 2013

Black Jack Jan 2007

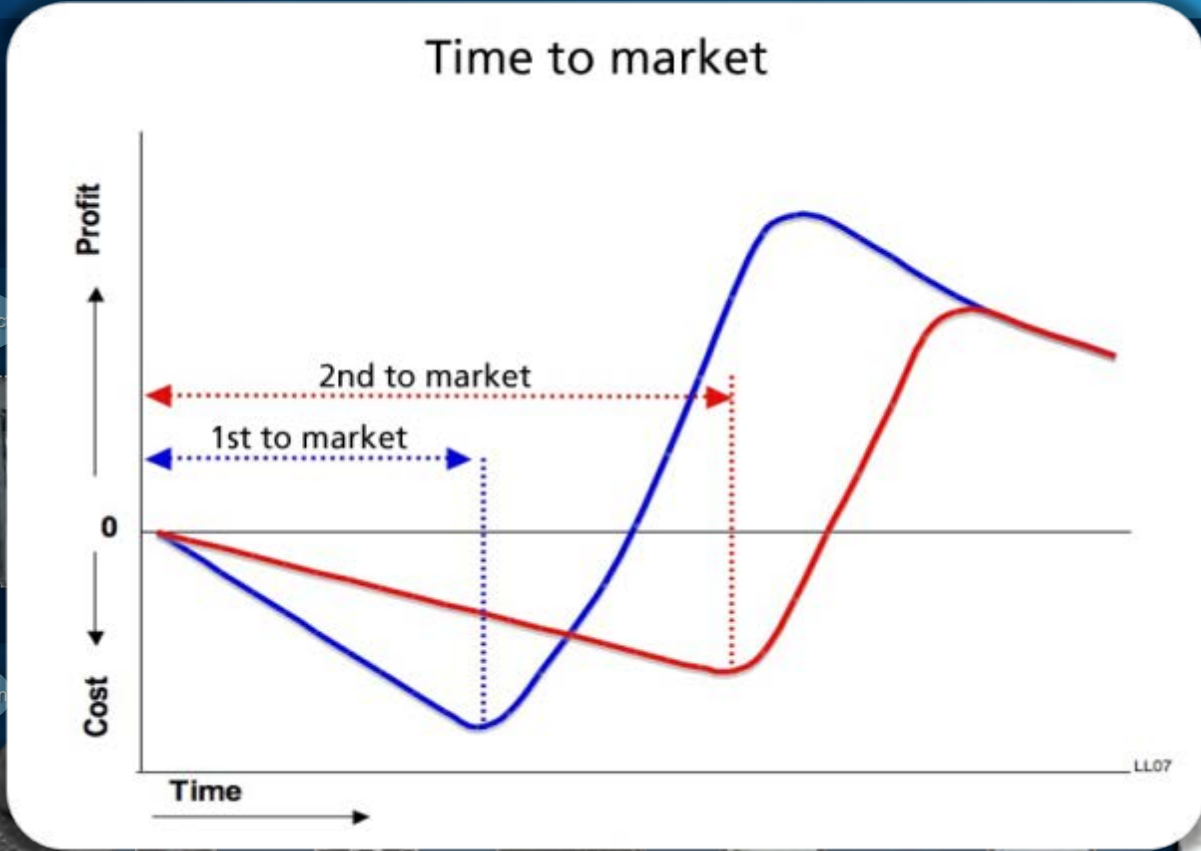


Instinct

Shine Feb 2007



Symbian



Galaxy S4 Mar 2013



Oct 2012

G Flex Oct 2013



# Big changes with each new generation

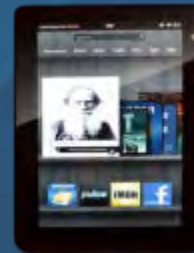
Kindle  
2007



Kindle Touch  
2011



Kindle Fire HD  
2012



Kindle Fire HDX  
2013



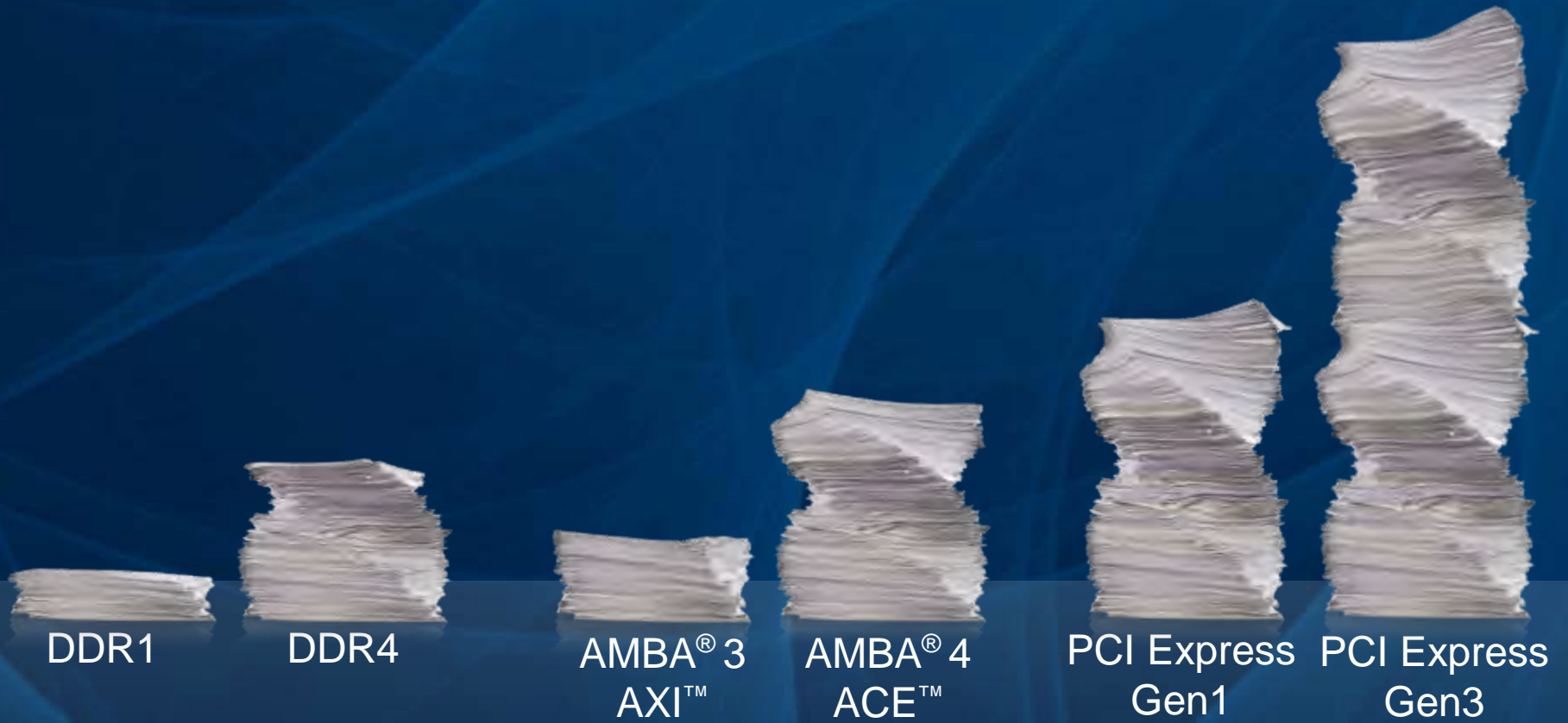
Processor	1 x ARM 11*	1 x ARM A8	2 x ARM A9	4x ARM A15**
Storage	250MB	4GB	Up to 64GB	Up to 64GB
Display	4 grayscale levels	16 grayscale levels	1920x1200 HD	2560x1600 HD
Interfaces	Keyboard, CDMA	Touch screen, 3G, Wi-Fi	Touch screen, 4G LTE, dual-band Wi-Fi, Bluetooth, HDMI, accelerometer, gyro, Dolby audio, HD front camera	Touch screen, 4G LTE, dual-band Wi-Fi, Bluetooth, HDMI, accelerometer, gyro, Dolby audio, HD front camera, 8MP rear camera

Notes: \* Kindle's Marvell Xscale CPU core comparable to ARM 11

\*\* Kindle Fire HDX's Qualcomm Snapdragon CPU cores comparable to ARM A15



# Ever changing standards





# New packaging technologies

## 2.5D and 3D packaging

Much more complexity

Thermal constraints

Reliability

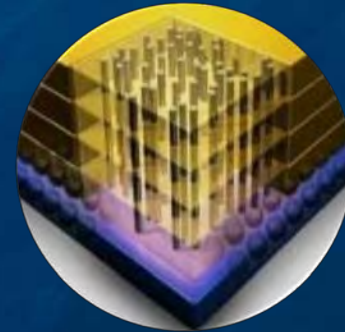
Cost



Package-on-package

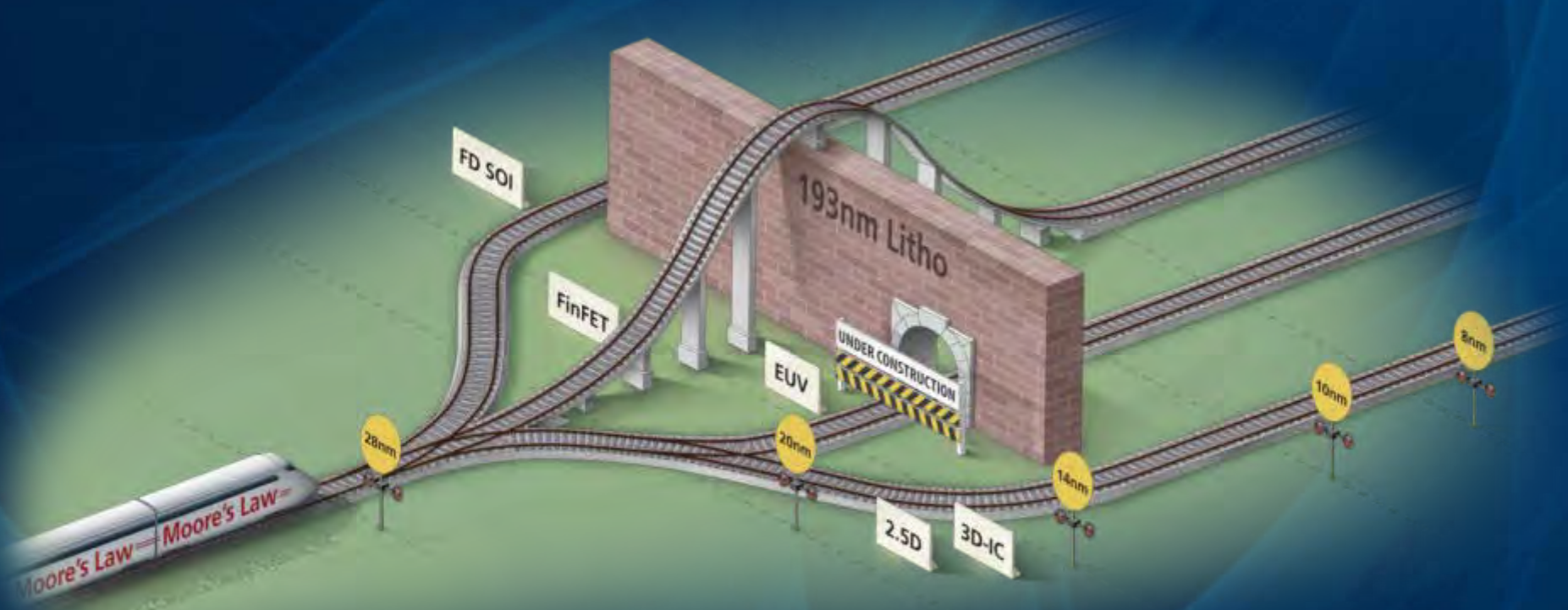


Stacked die



Through Silicon Vias

# New semiconductor technologies





**Creative Solutions Required**

# Systems oriented design approach

## IP

DSP

Memory

Interfaces

Protocols

Standards

Constraints

## Systems Verification

Features

Power

Software

## Implementation

Silicon

Package

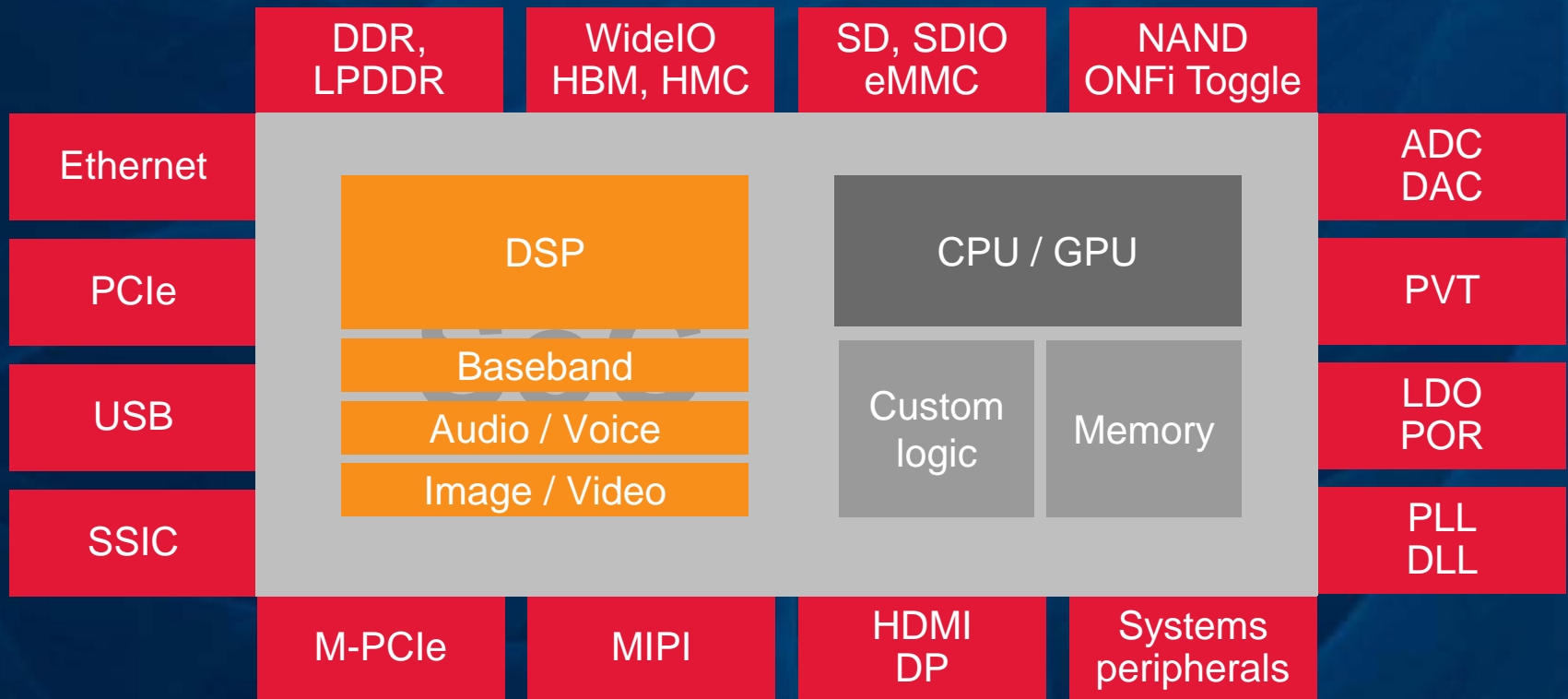
Cost



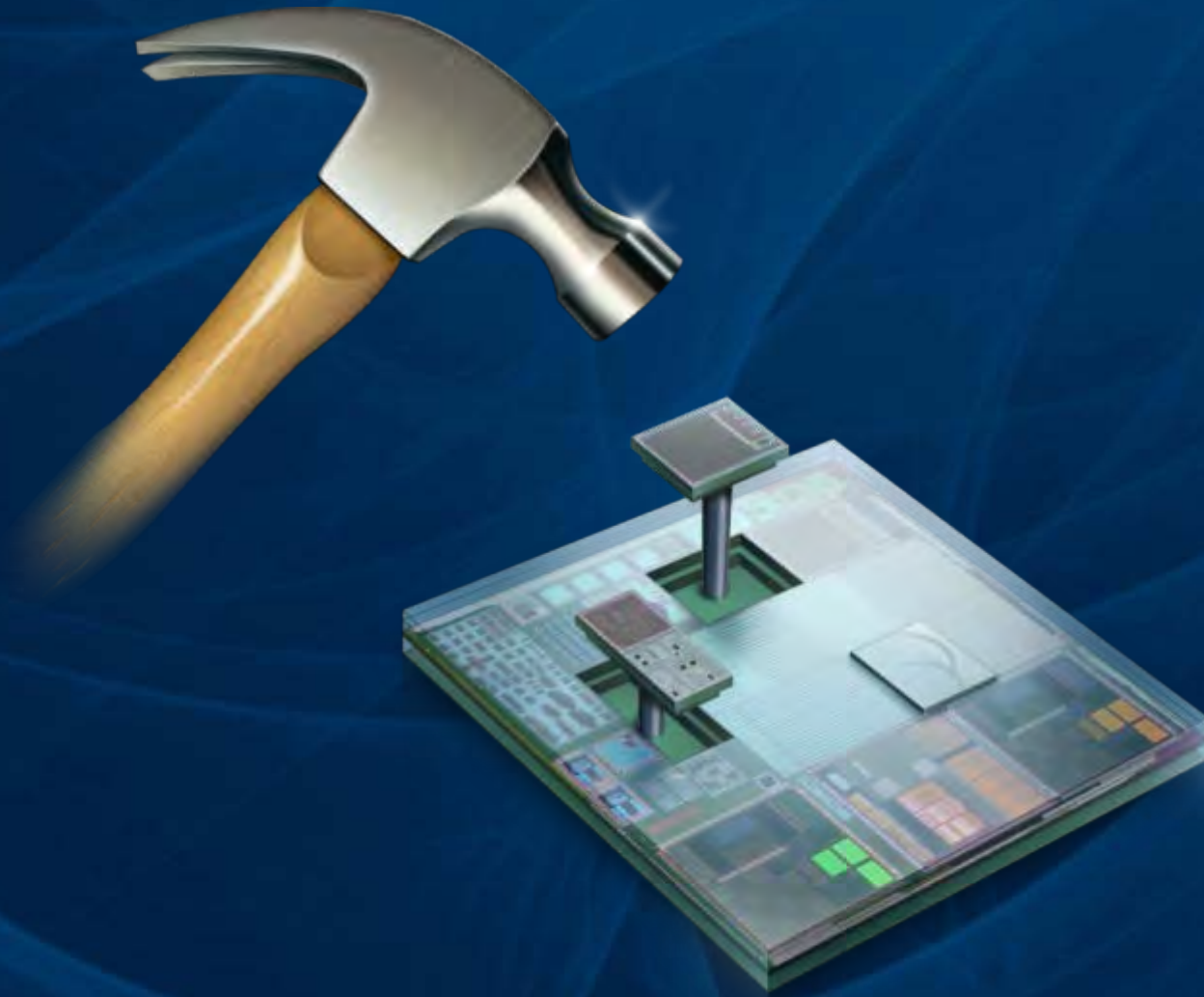


IP

# Typical SoC design

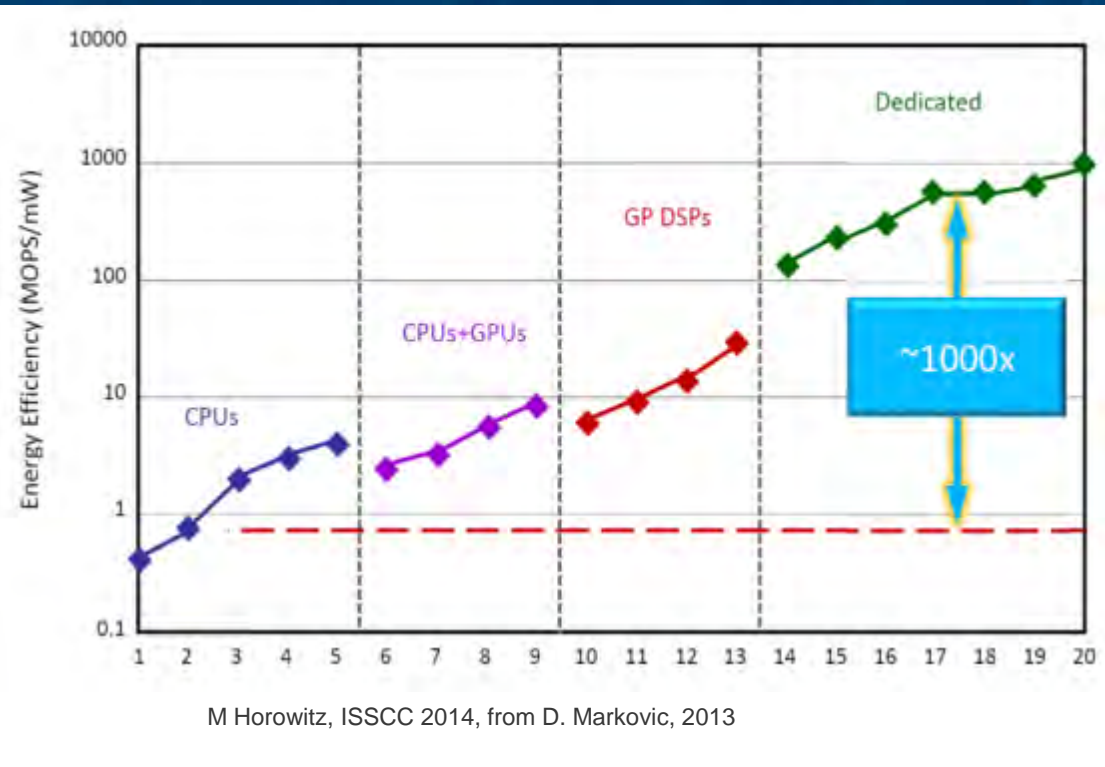


If all you have is a hammer –  
everything looks like a nail



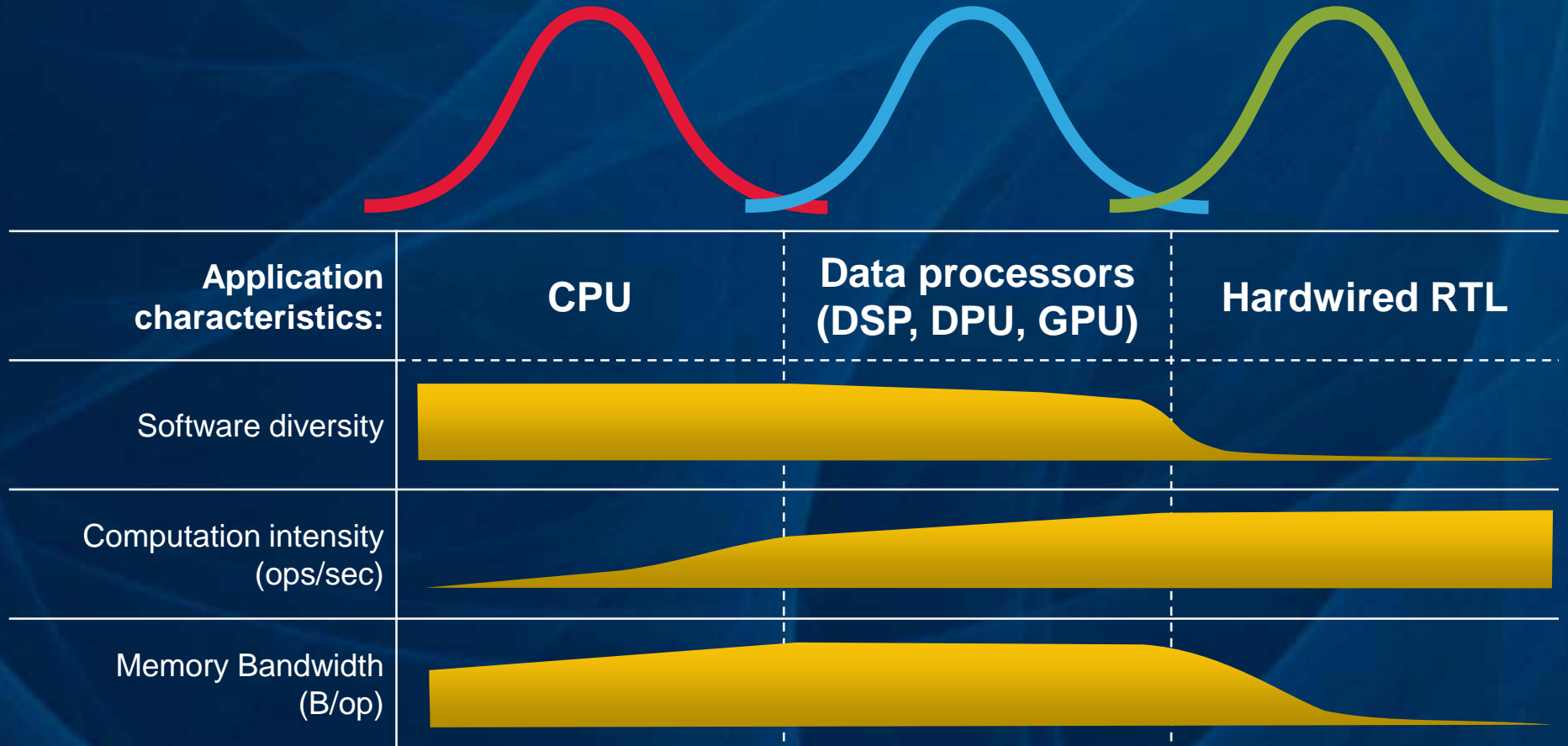
# Dedicated logic is the most efficient answer, right?

- Conventional wisdom: dedicated logic up to **1000x** more efficient than CPUs
- True only in special circumstances: **minimal** memory references per op
- For memory-intensive tasks, fixed logic little better than best processor methods





# Data processing and the three sweet-spots

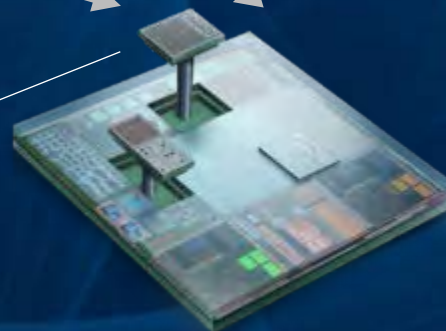


# Integrating multiple functions onto one core

## Flexibility and efficiency

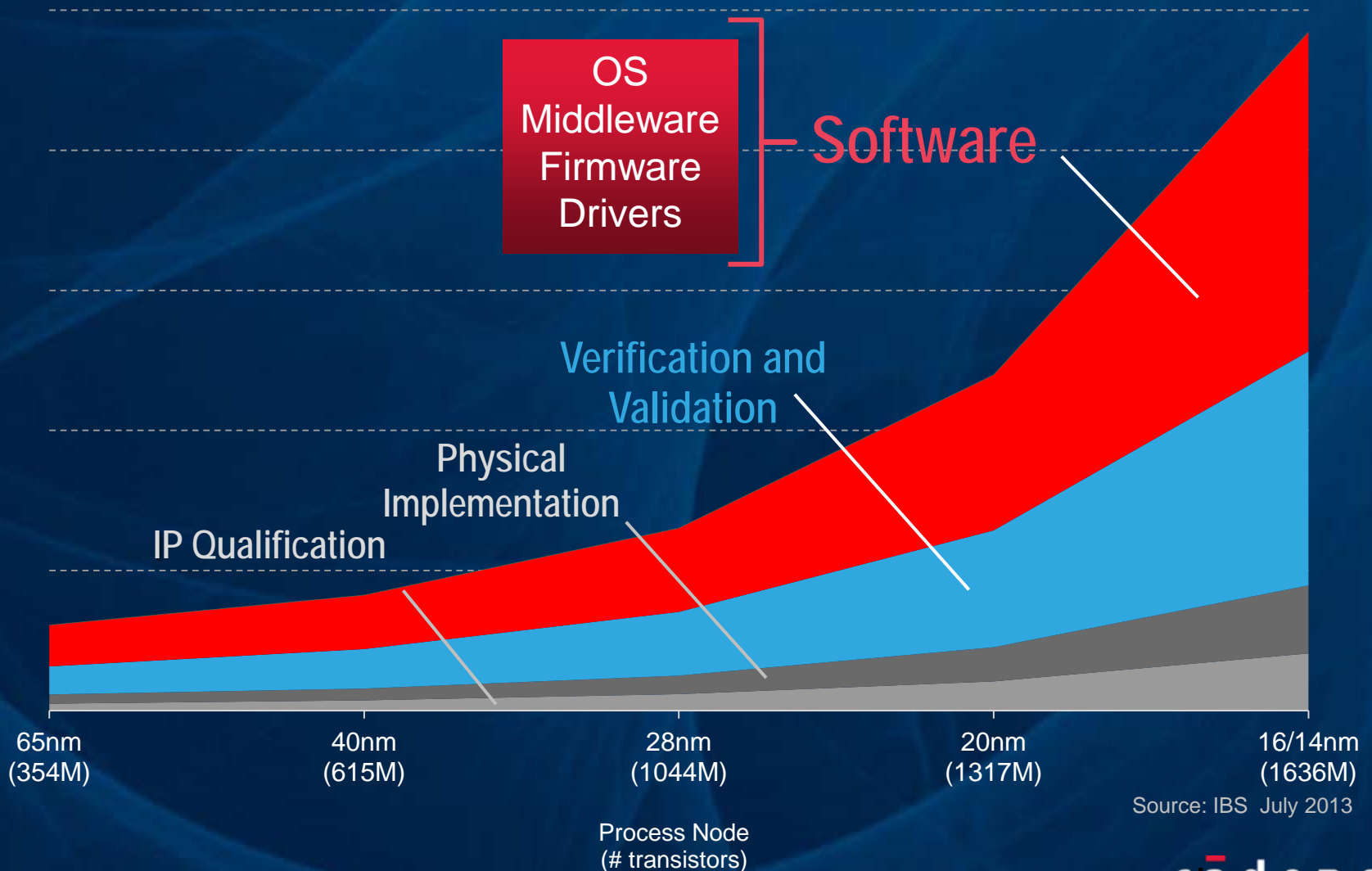
AEC Wideband	AMR Wideband	DAB/MP2
DRM	Dolby Digital	Dolby DM3Plus
Dolby MS10	Dolby Prologic	Dolby TrueHD
DRA	DTS Boost	DTS HD
DTS Symmetry	FLAC	MP3
MPEG-4 aacPlus	mSBC	Ogg Vorbis
SBC Bluetooth	WMA	WMA 10 Pro
AMR Speech	G722 Speech	G.729AB Speech
SILK Speech	GSM-FR Speech	G726 Speech

Tensilica HiFi DSP



# Systems Verification

# 80% of SoC development costs come from software, verification, and validation



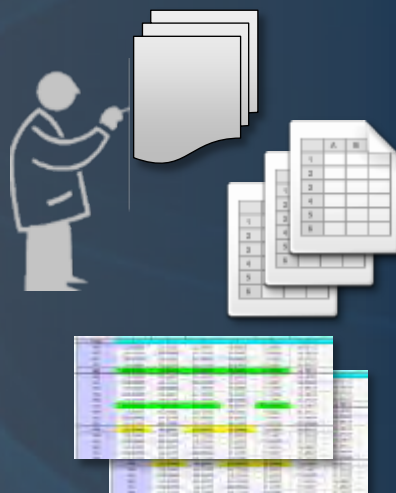
Source: IBS July 2013



# Need scalable solution for metric-driven verification

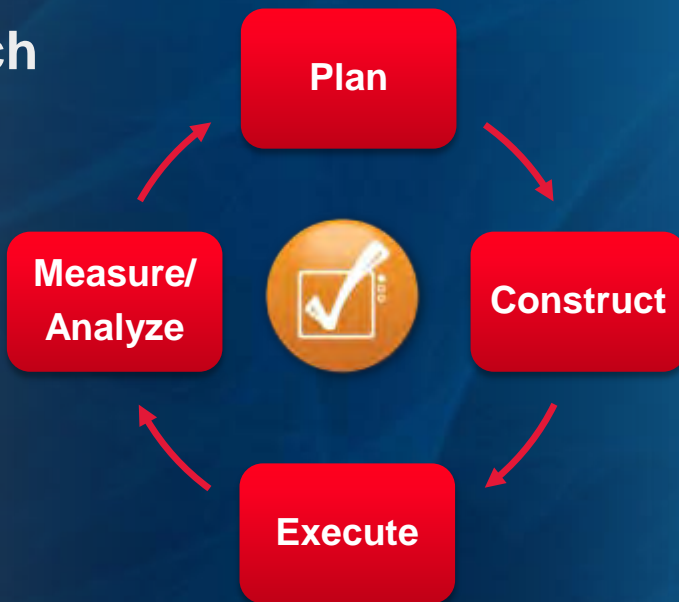
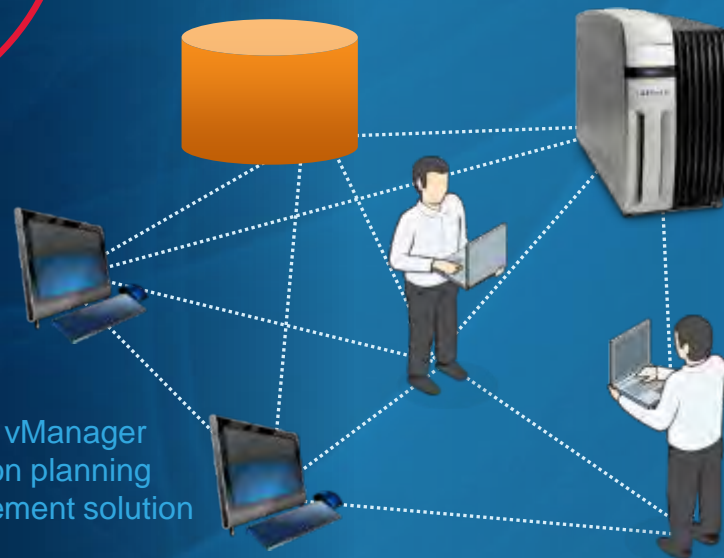
## Traditional approach

Spreadsheets  
Scripts  
Lists



## Scalable approach

Robust SQL database  
Synchronous data  
Real-time reports  
2X Productivity



Incisive® vManager  
verification planning  
and management solution

# Hardware acceleration is essential for today's SoCs

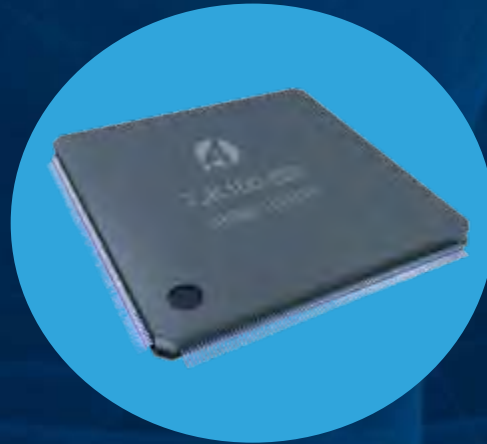
## Palladium<sup>®</sup> XP II

Verification  
Computing  
Platform



# Concurrent software development with hybrid verification technology

Start SW validation up to six months earlier



60 X faster OS boot



Virtual Prototyping

ARM® Fast Models



Acceleration & Emulation



SpeedBridge Adapters



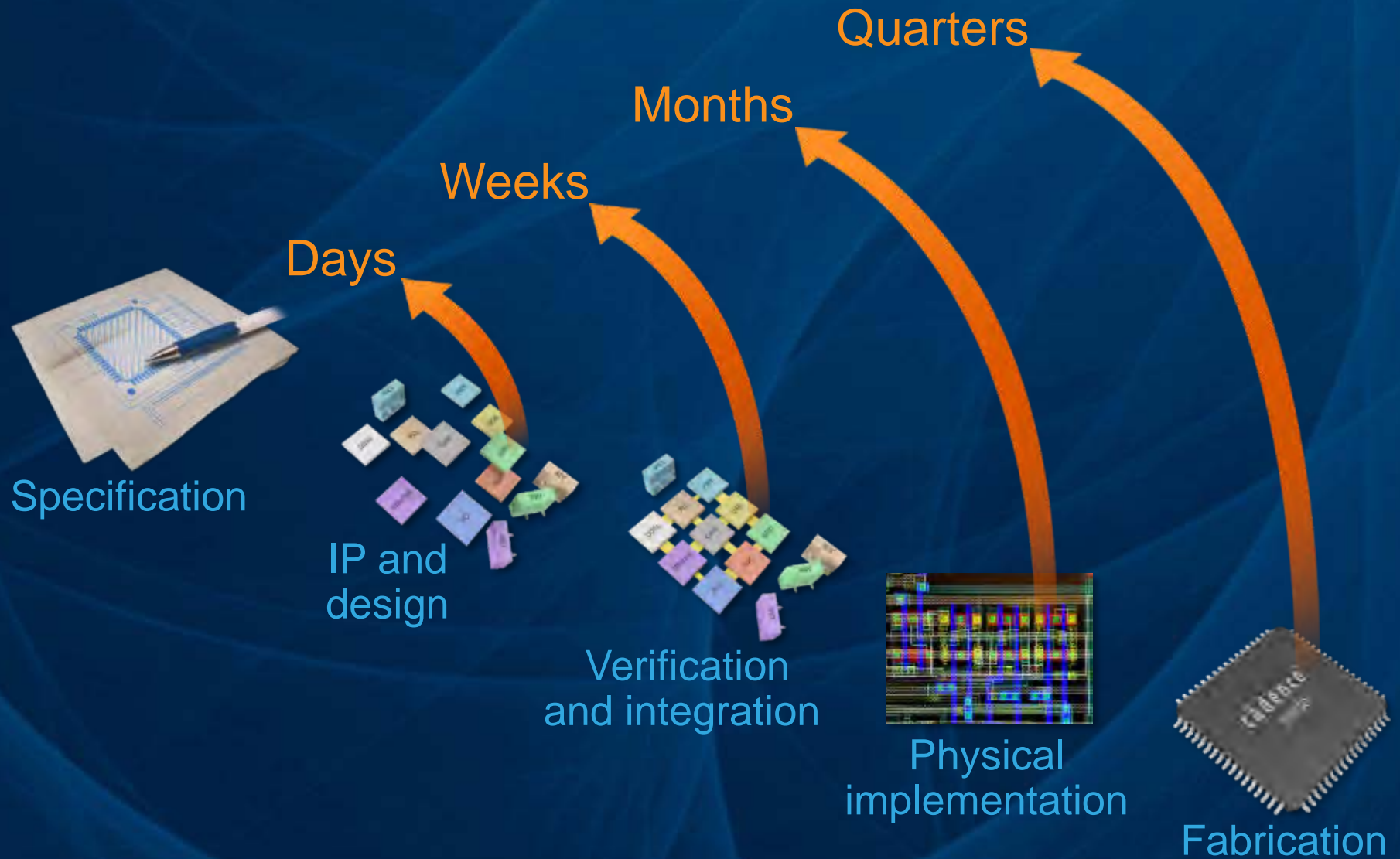
FPGA Prototyping



# Implementation

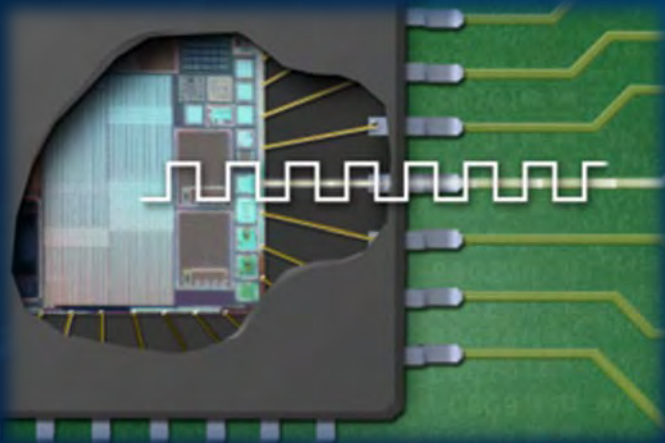


# Late bugs kill time-to-market



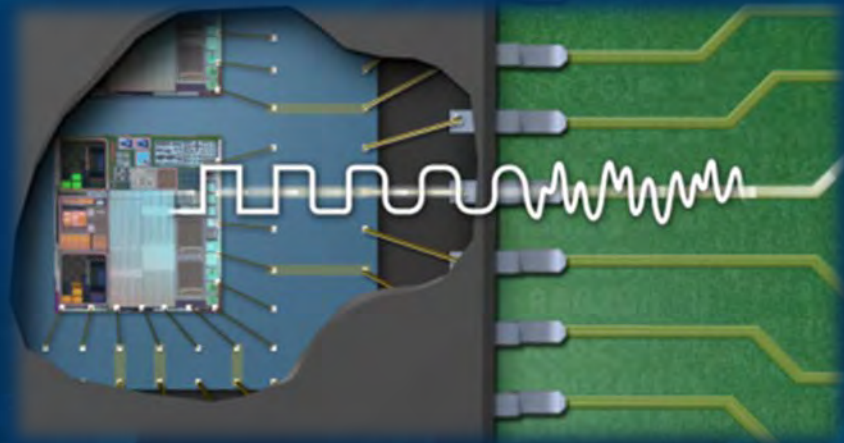
# IP implementation is increasingly complex

PAST



Megahertz signals  
Simple static timing analysis  
Static power analysis

TODAY



Gigahertz signals  
Package and board effects  
Signal integrity analysis  
Analog channel models  
Dynamic power analysis  
Advanced library characterization

# Requirements for IP today

- 
- IP-XACT
  - LEF
  - IBIS
  - Lib

- VIP
- Transaction-level model
- Drivers
- FPGA prototype
- Documentation
- Scripts
- Power models

# IP requires comprehensive EDA support

## System design

**HW/SW  
co-design**

DDR,  
LPDDR

WideIO  
HBM, HMC

SD, SDIO  
eMMC

NAND  
ONFi Toggle

**Custom,  
analog,**

Ethernet

ADC  
DAC

**mixed-signal  
design and  
implementation**

**Logic des**

PCIe

DSP

CPU / GPU

PVT

Baseband

Audio / Voice

Image / Video

Custom  
logic

Memory

LDO  
POR

**Digital  
implementation**

SSIC

PLL  
DLL

**PCB and  
package  
design**

M-PCIe

MIPI

HDMI  
DP

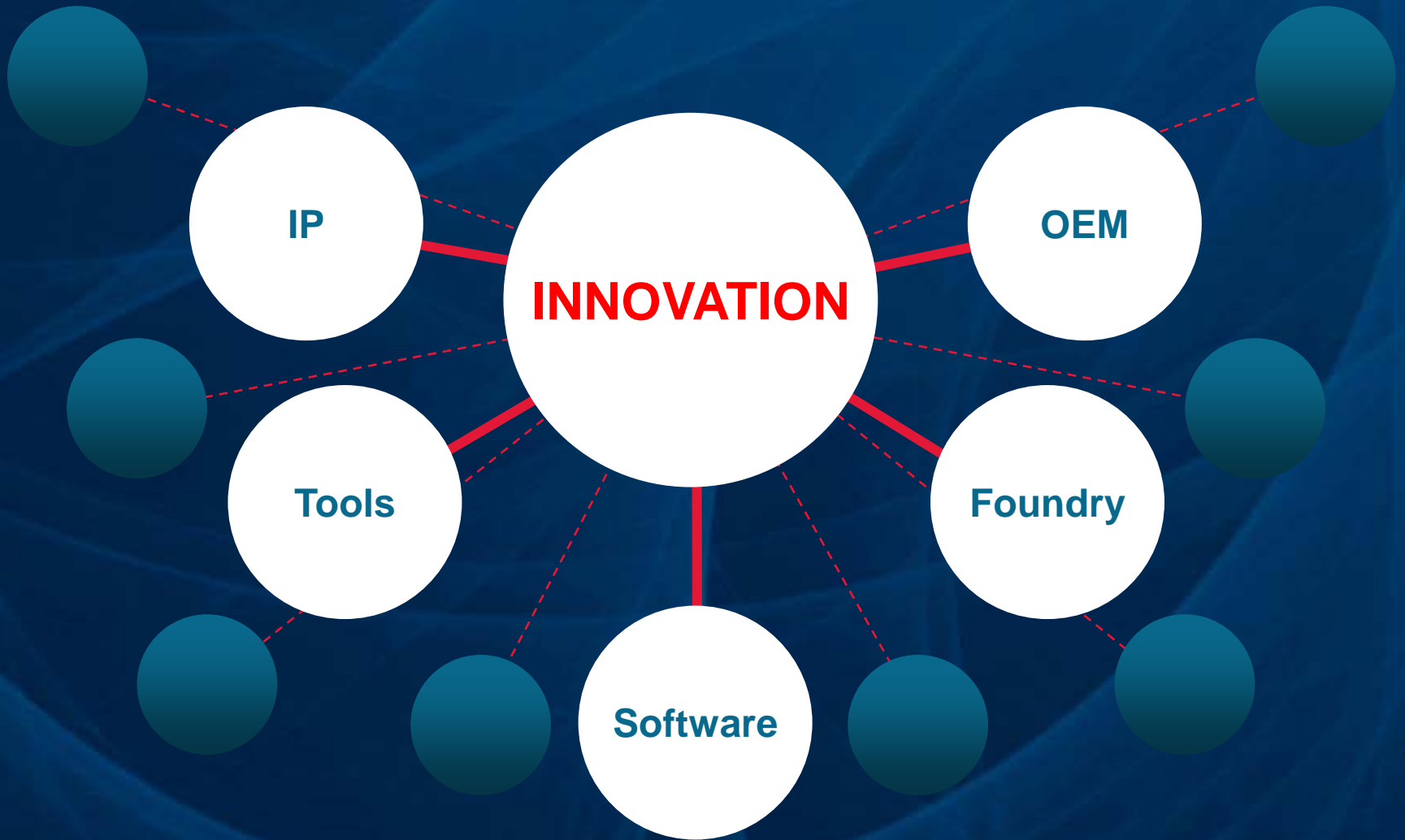
Systems  
peripherals

**Signoff and manufacturing**

**Verification**



# Today's SoCs require closer collaboration than ever before – from IP through manufacturing



The logo for Cadence, featuring the word "cadence" in a lowercase, white, sans-serif font. A small red horizontal bar is positioned above the letter "a". A registered trademark symbol (®) is located to the upper right of the word.

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