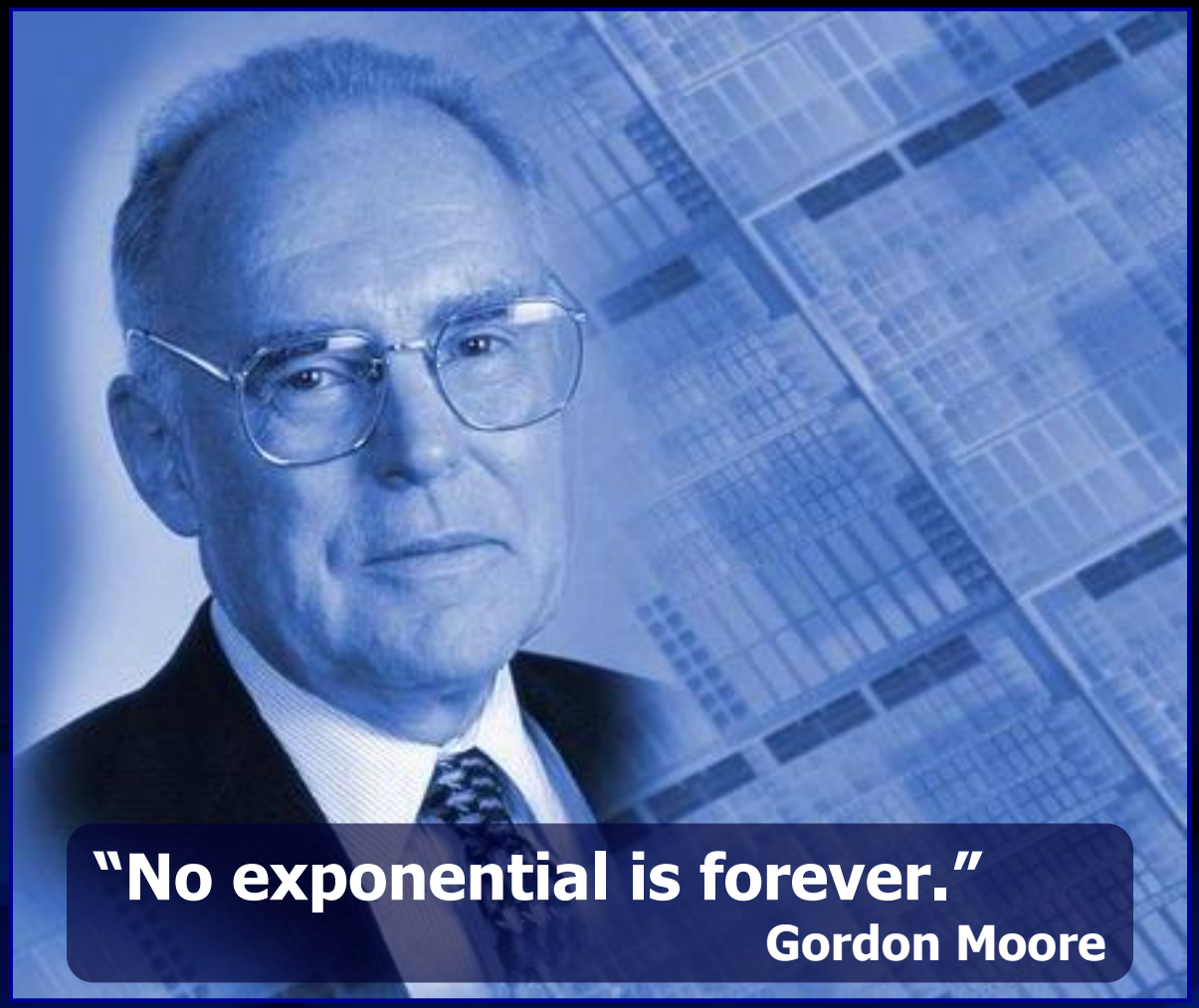
The Big Squeeze

Walden C. Rhines
Chairman and CEO

April 2014

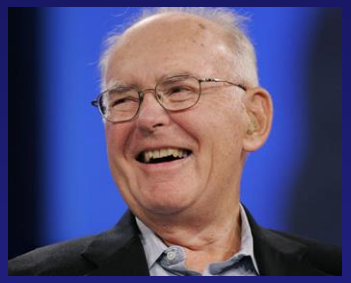
Mentor Graphics®

Moore's Law Coming to an End?



Source: ISSCC Keynote, 2003

Moore's Law – The Number of Transistors

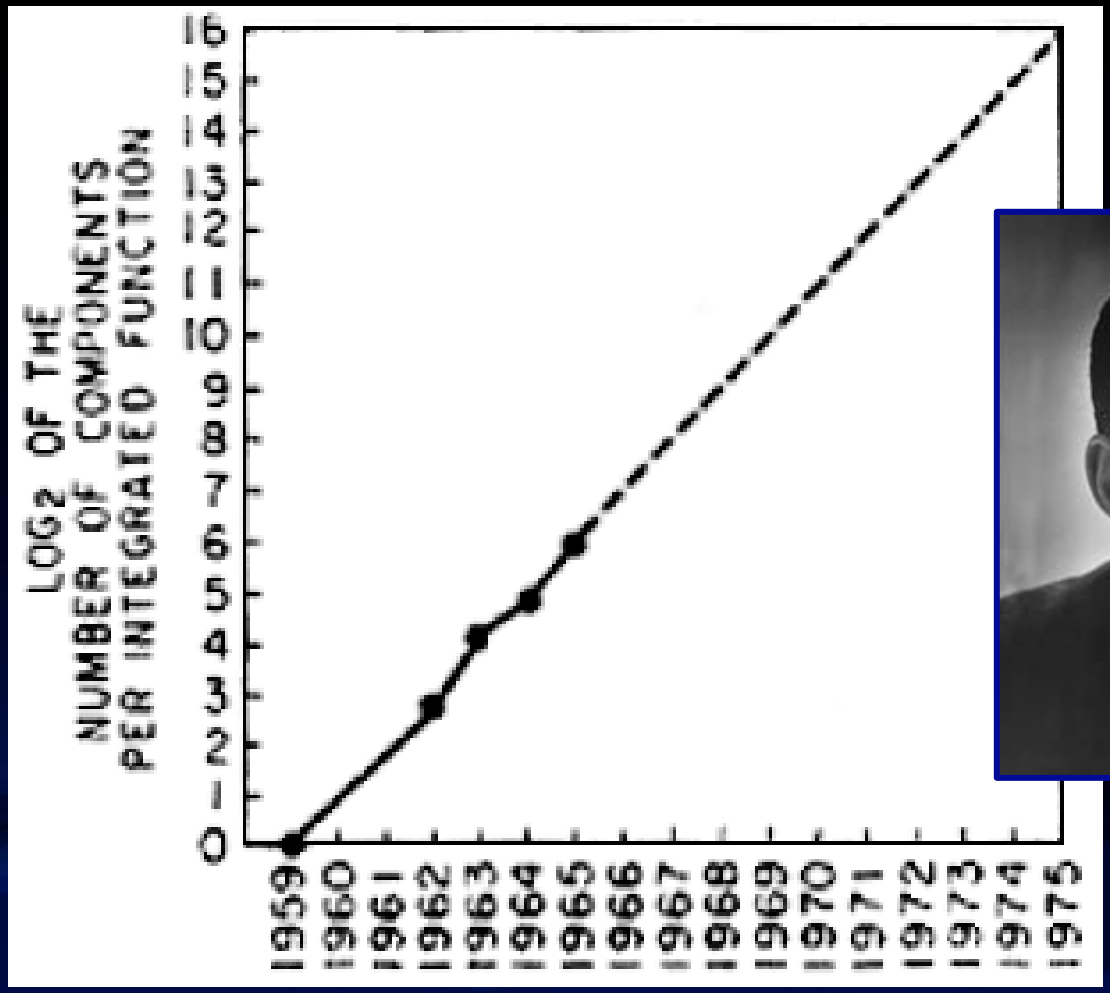


What would you like your legacy to be?

"…Anything but Moore's Law."

Gordon Moore, May 2008

Moore's "Law" = 4 Data Points from 1962 to 1965

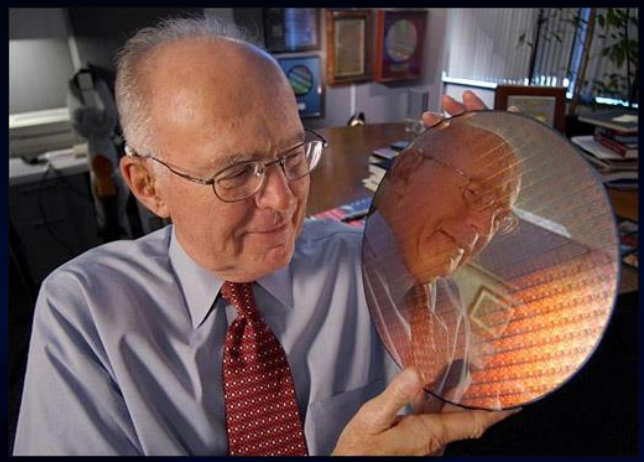


Why Has Moore's Law Been a Useful Approximation for Almost 50 Years?

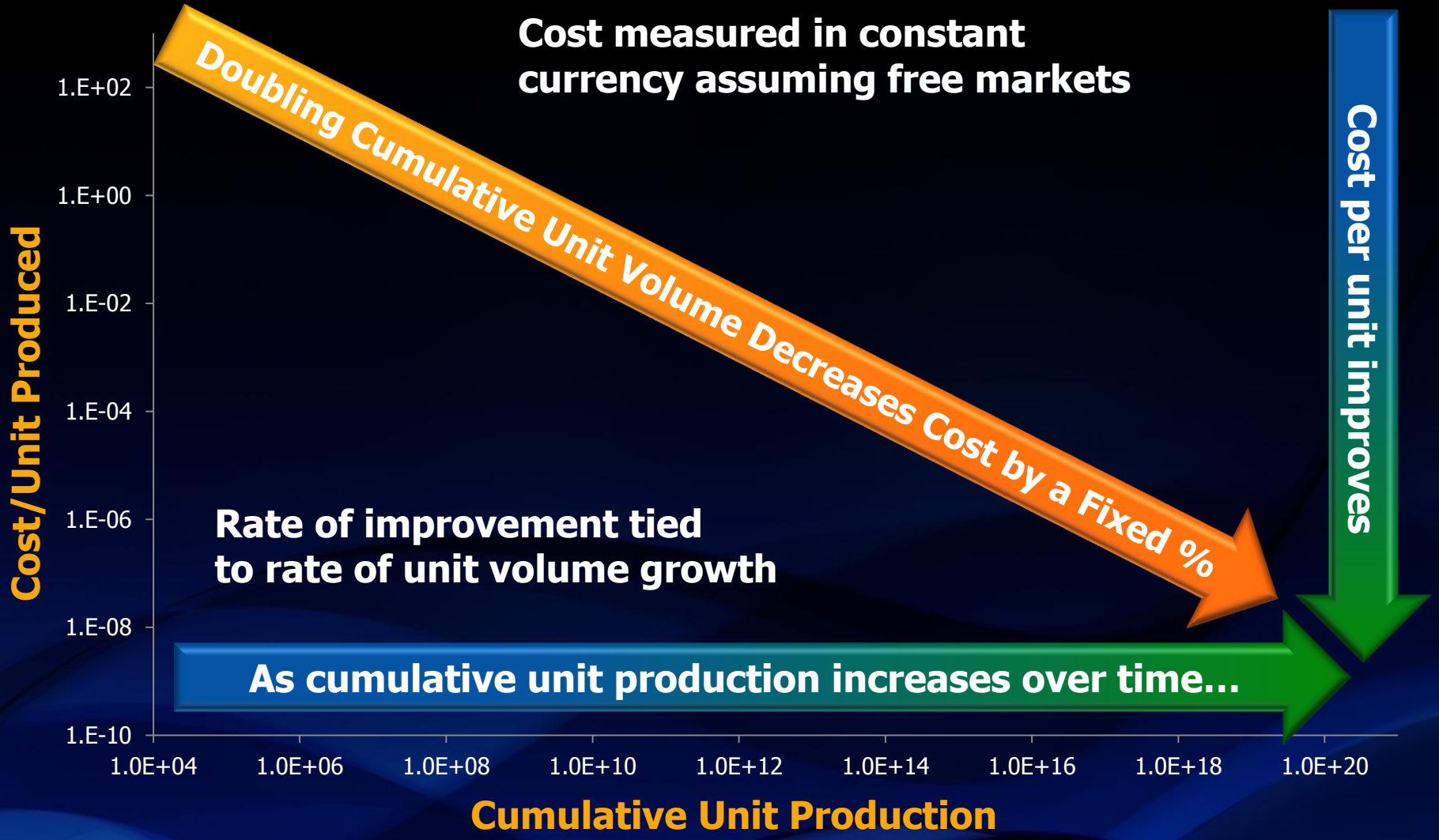
Based on a real "law" of nature, the "Learning Curve", when two things are true:

1. Cumulative transistors produced increase exponentially with time (e.g. 2x cum volume ➔ fixed % cost decrease)

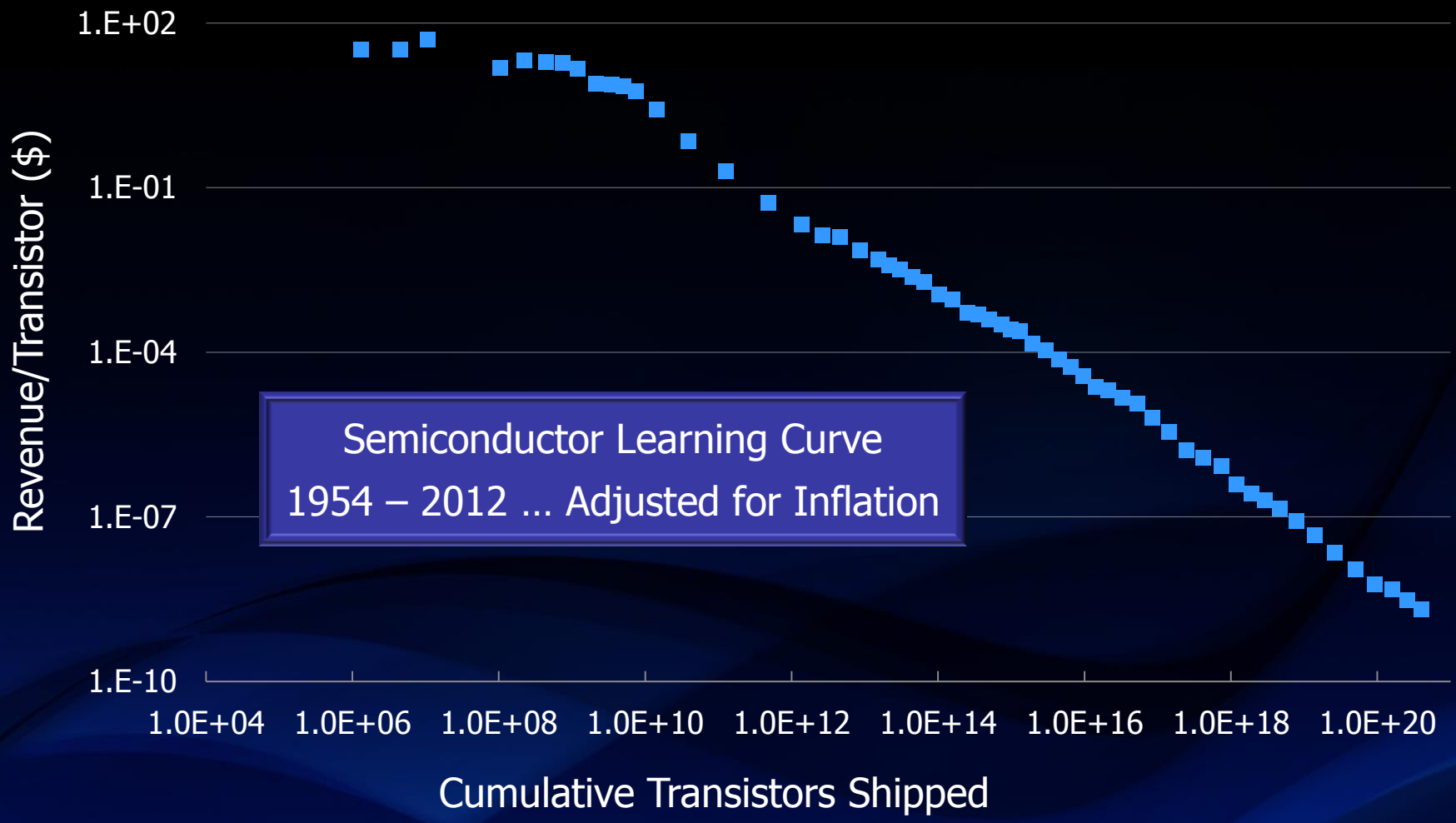
2. Almost all cost reduction comes from shrinking feature sizes (and growing wafer diameter)



Learning Curve

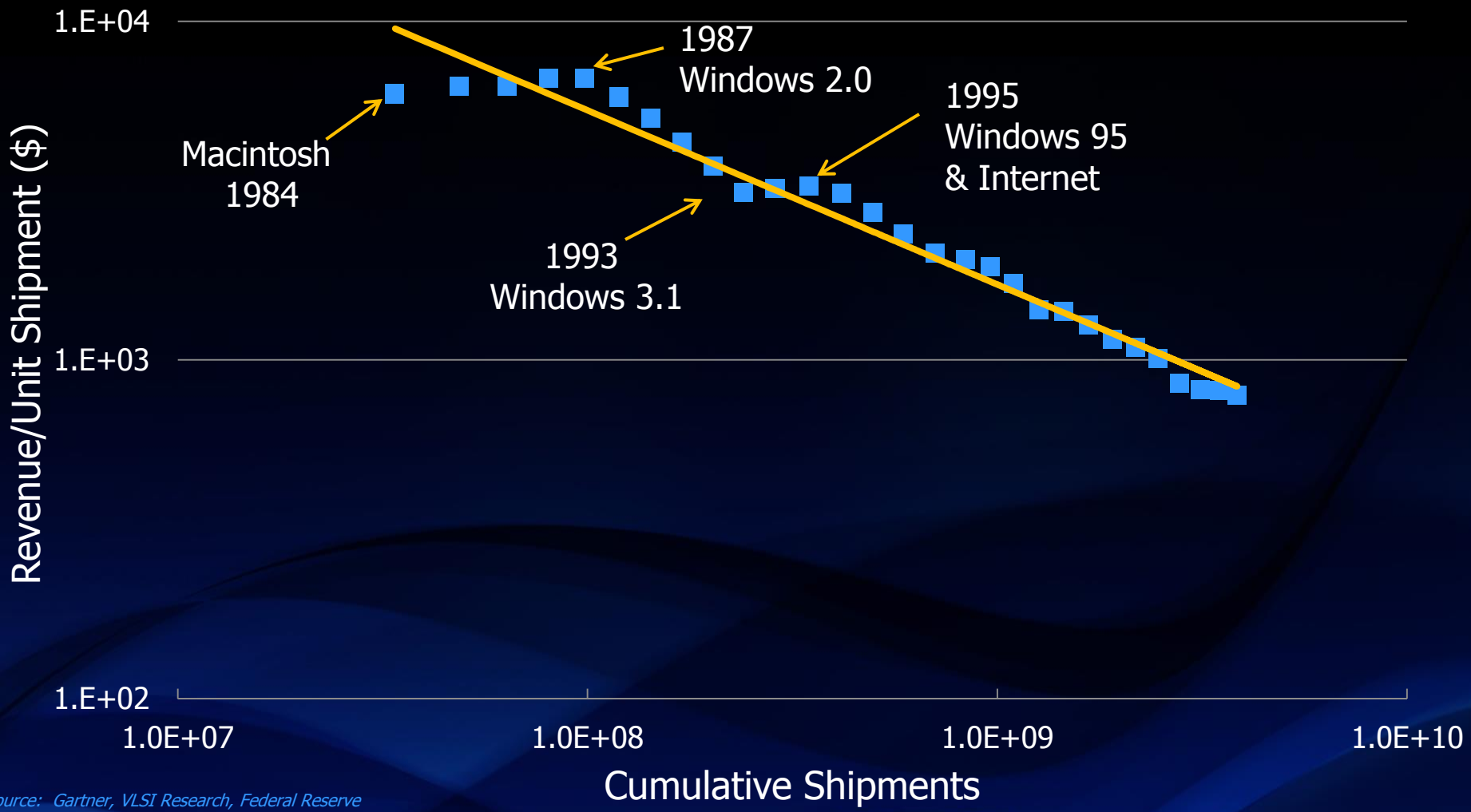


Growth of Transistor Unit Volume Leads to Sustained ~30% per Year Cost Reduction



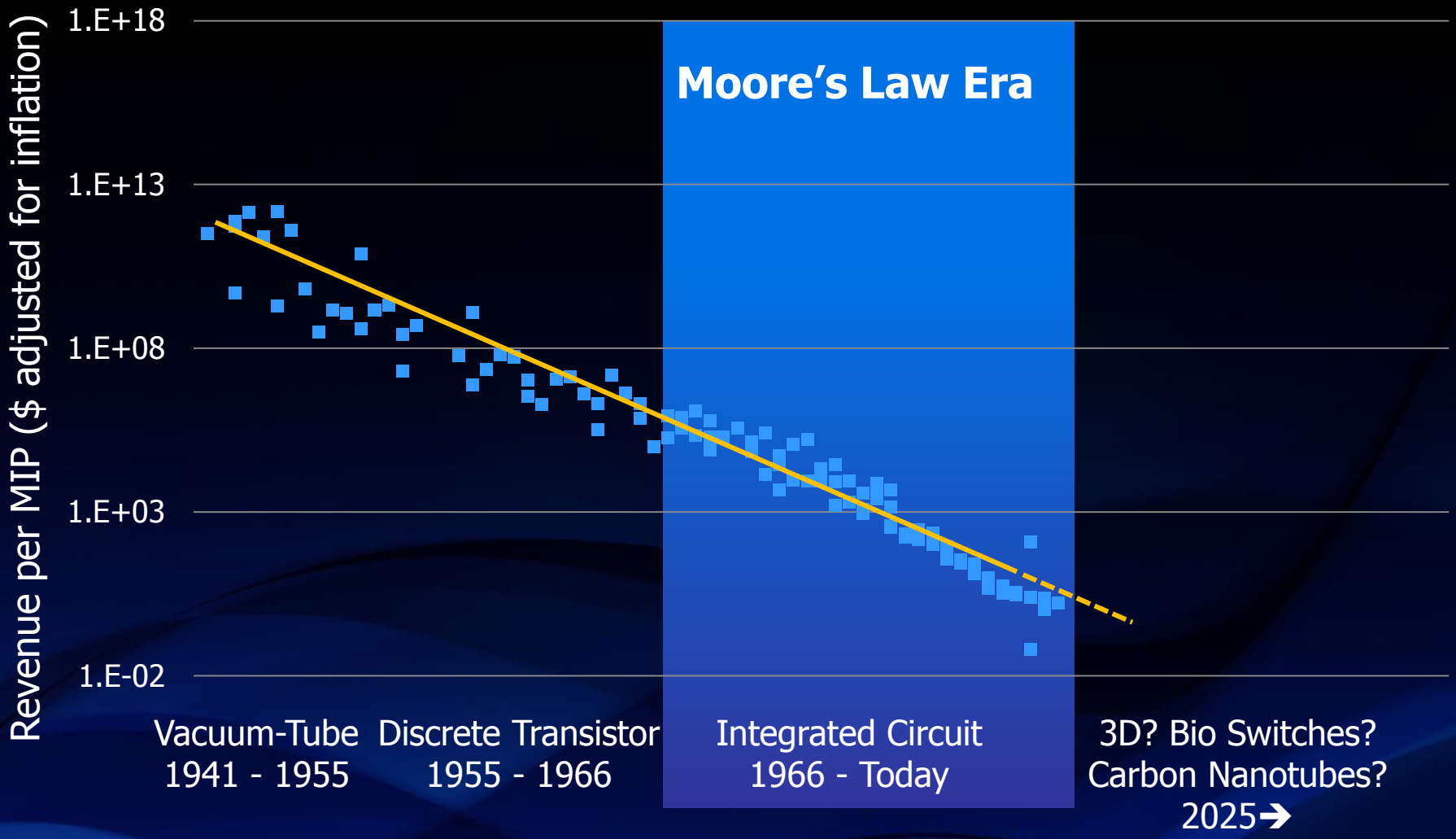
Source: VLSI Research, SIA, Federal Reserve
Note: Revenue adjusted for Inflation… 1954-2012

Personal Computer Learning Curve: 1984-2012

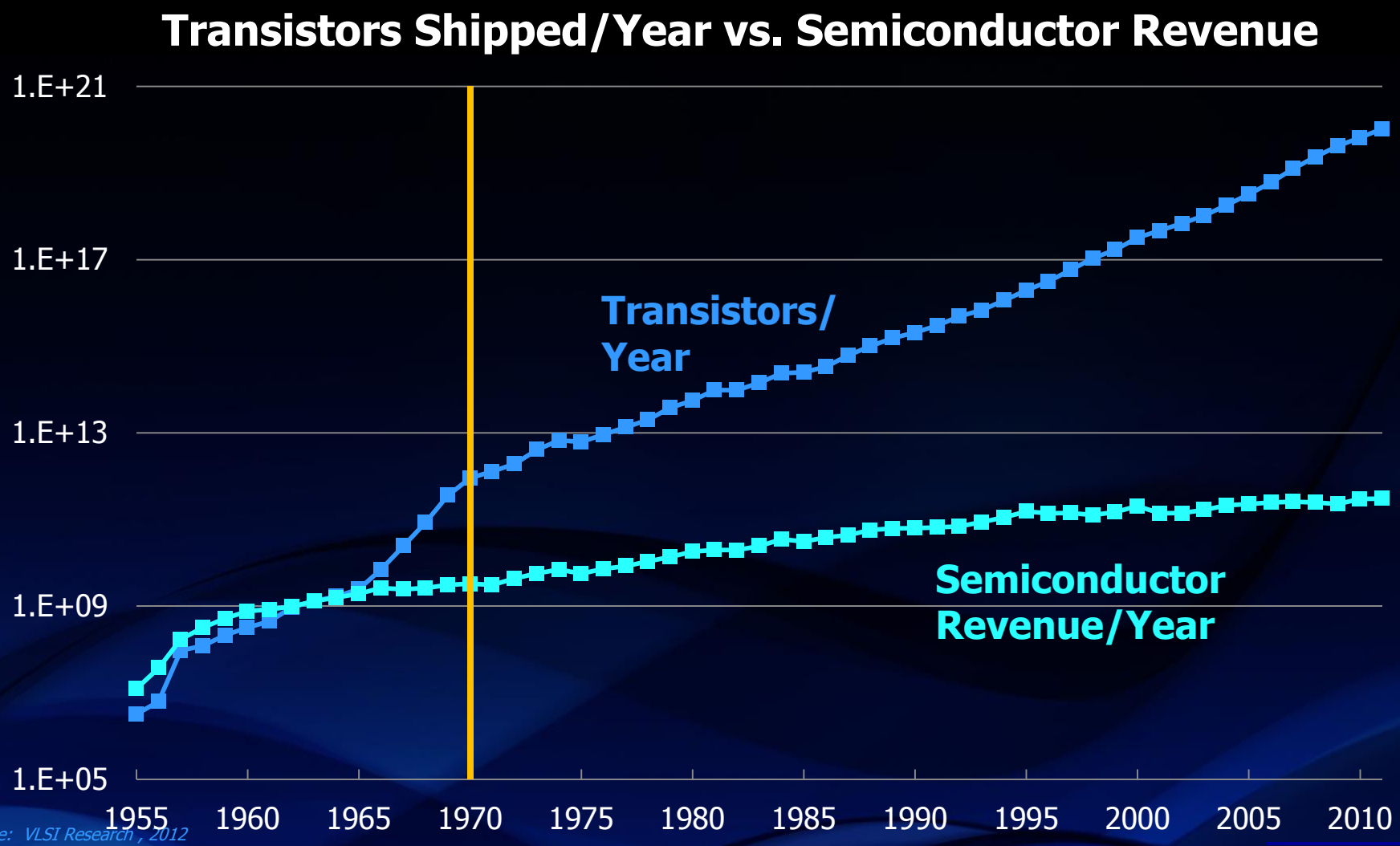


Source: Gartner, VLSI Research, Federal Reserve
Note: Revenue adjusted for Inflation… 1984-2012

Cost per Function Will Continue to Decline Long after Moore's Law Is Obsolete



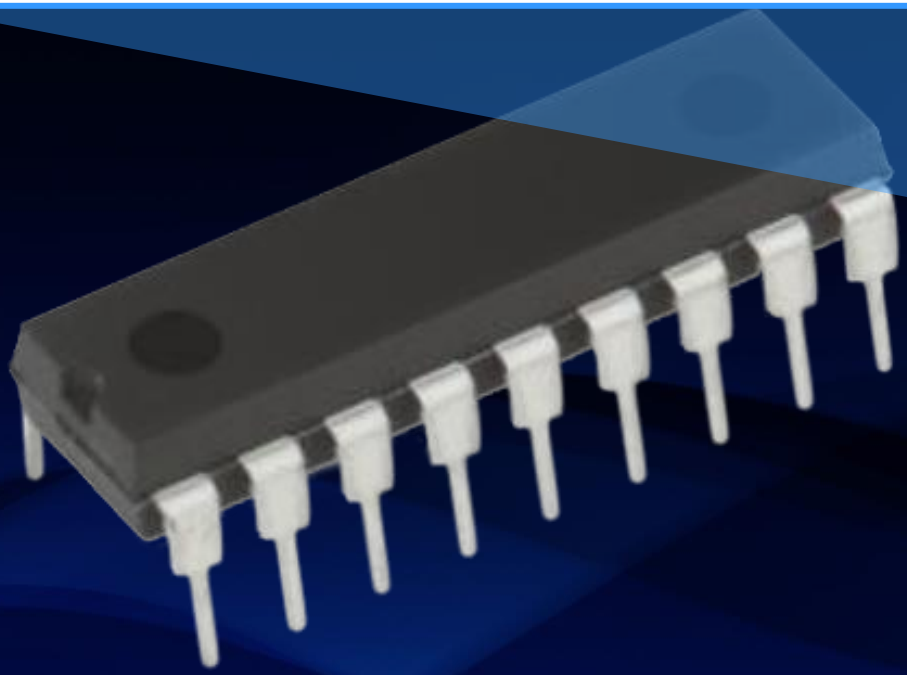
Unit Volume Scale (log) Same as Time (years)
Due to Exponential Growth in Transistors/Year since 1970

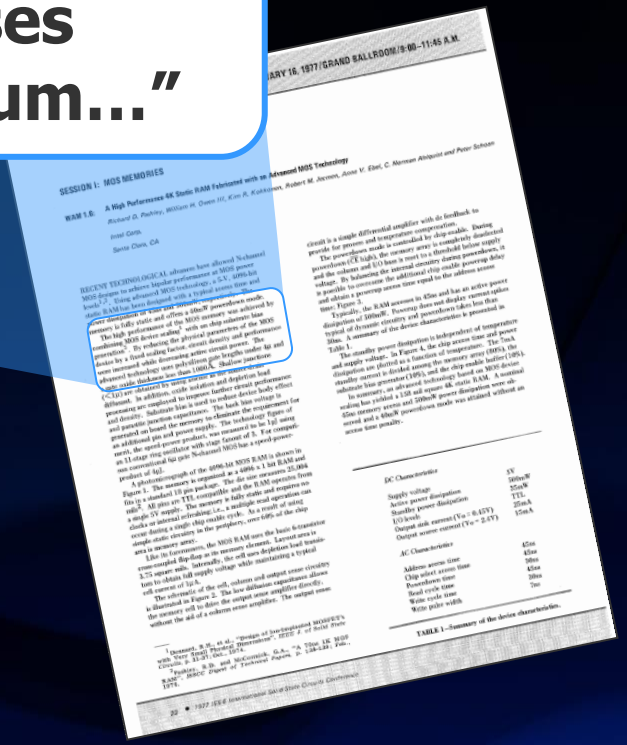


Source: VLSI Research , 2012

With Focus on Moore's "Law", Feature Sizes Became the Metric of Success

"The advanced technology uses polysilicon gate lengths under 4um…"





SESSION I: MOS MEMORIES

WAM 1.6: A High Performance 4K Static RAM Fabricated with an Advanced MOS Technology

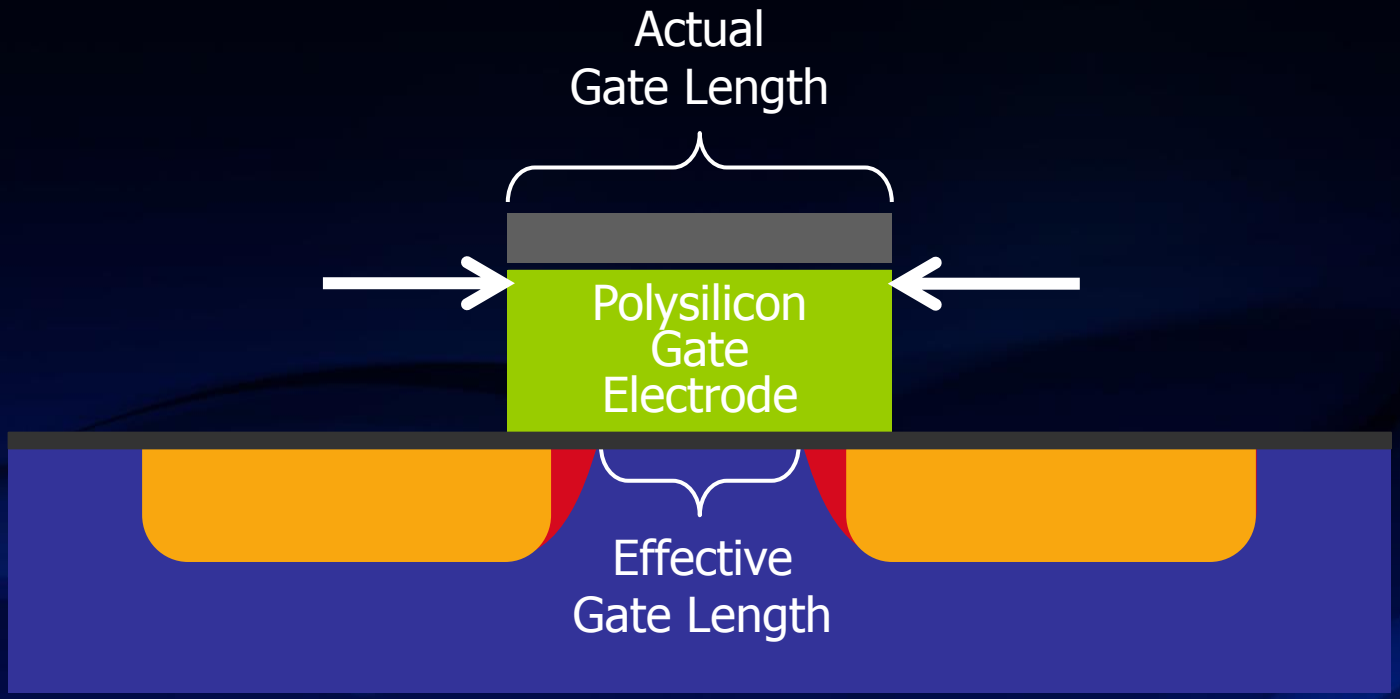
Marketing Takes Over Engineering Definitions

Drawn gate length L_{drawn} ~ Width specified by layout engineer

Actual gate length L_{actual} ~ Actual physical width of gate material

Effective gate length $L_{effective}$ ~ Over etch shortens physical width of gate

Effective gate length $L_{effective}$ ~ Dopant migration shortens effective gate length



NTRS Roadmap (1994) Attacks the Need to Define Technology Generations

TECHNOLOGY GENERATIONS DEFINED BY:

- Year of first **DRAM** shipment (10k+)
- Minimum feature size (nm)
  - "Smallest feature printed, **usually poly gate**"

1994 DRAM Projections						
First DRAM Shipment	**1995**	**1998**	**2001**	**2004**	**2007**	**2010**
Minimum Feature Size (μm)	**0.35**	**0.25**	**0.18**	**0.13**	**0.10**	**0.07**

Source: NTRS Roadmap, 1994

Refined Again in the 1997 NTRS Roadmap

TECHNOLOGY GENERATIONS DEFINED BY:

- Year of first **product** shipment
- Minimum feature size (nm)
  - DRAM: "…The half-pitch of first-level interconnect dense lines"
  - LOGIC: "….gate length…"

Technology Generation 1997 Predictions							
First Product Shipment	**1997**	**1999**	**2001**	**2003**	**2006**	**2009**	**2012**
DRAM Half-Pitch (nm)	**250**	**180**	**150**	**130**	**100**	**70**	**50**
MPU Gates (nm)	**200**	**140**	**120**	**100**	**70**	**50**	**35**

Source: NTRS Roadmap, 1997

ITRS Gives Up…

"**Significant confusion relative to the historical ITRS node definition** continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria…

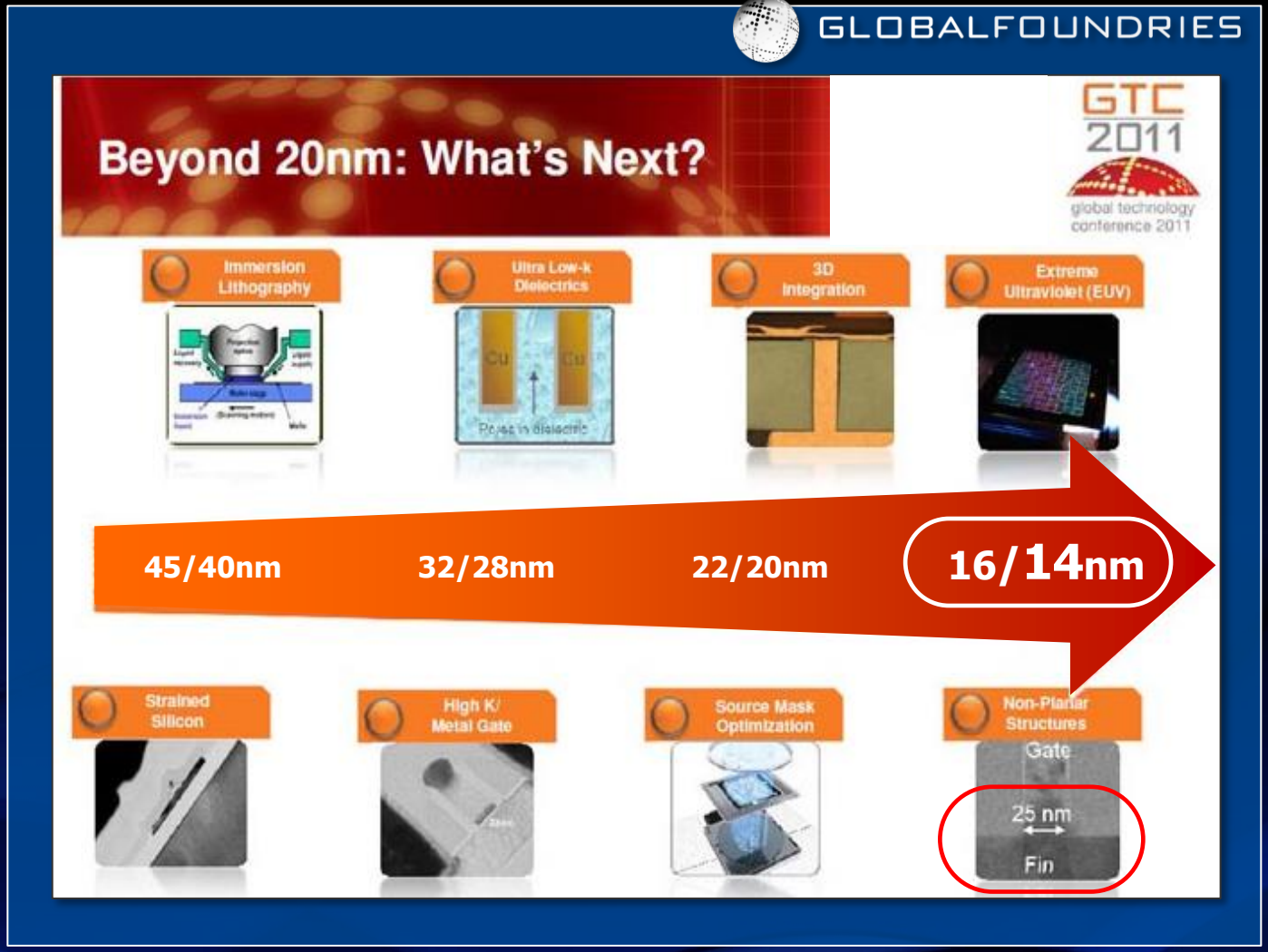
In the 2009 ITRS, we will discontinue the practice, thus **eliminating references to the term 'technology node.'**

ITRS Roadmap, 2009

Source: http://scsong.wordpress.com/2009/10/13/looking-forward-to-22-nm/

TSMC Technology Roadmap – 20nm with FinFET

GlobalFoundries Technology Roadmap – 20nm with FinFET



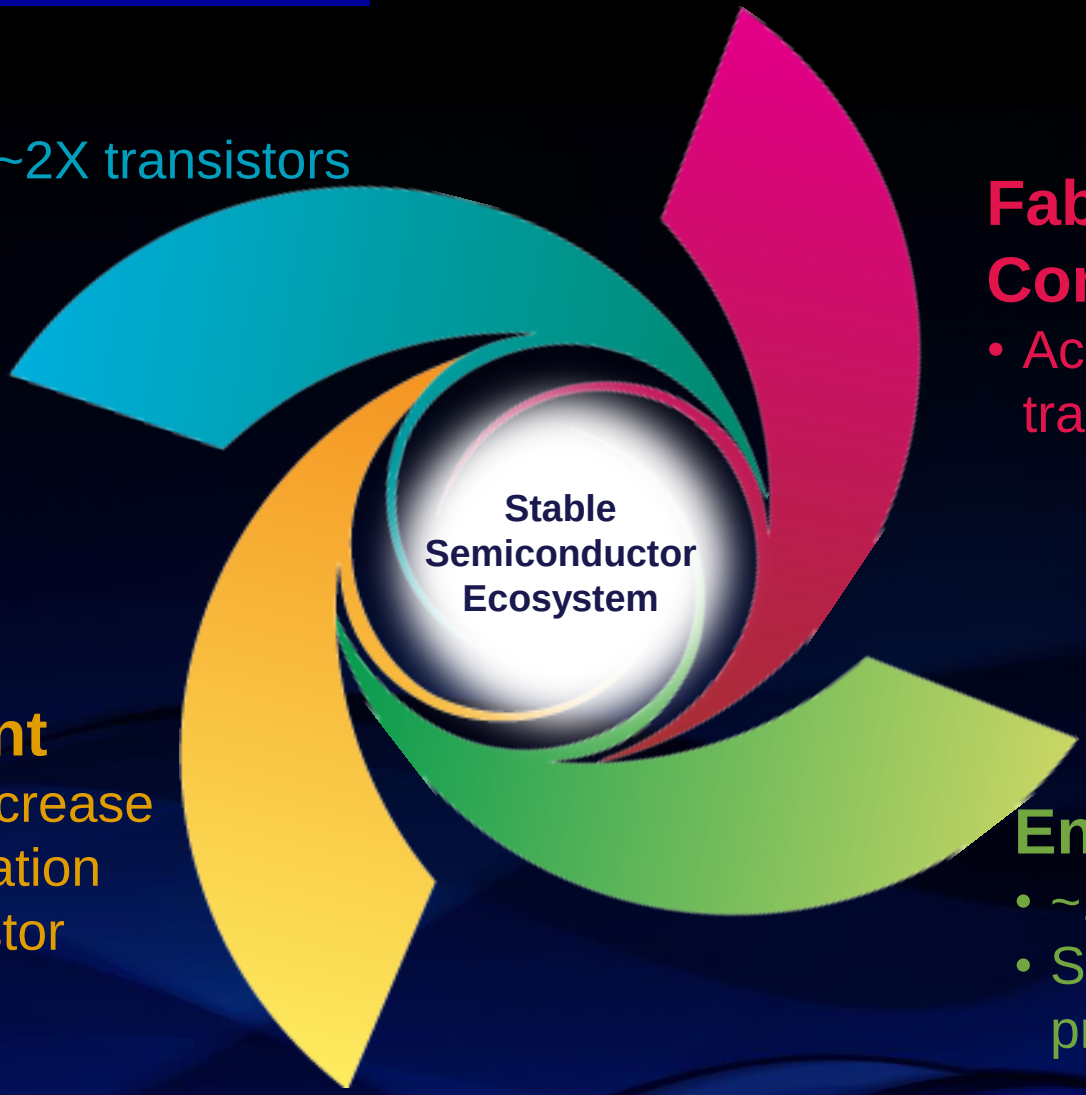
Stable Ecosystem Keeps Supplier Margins Healthy while Growing Functionality 1.7X…

Technology Node (μm)	Linear Shrink Scale Factor (k)	Area Shrink (%)	Transistor Multiple
1.5	--	--	--
1	0.67	44%	2.3 X
0.8	0.80	64%	1.6 X
0.6	0.75	56%	1.8 X
0.5	0.83	69%	1.4 X
0.35	0.70	49%	2.0 X
0.25	0.71	51%	2.0 X
0.18	0.72	52%	1.9 X
0.13	0.72	52%	1.9 X
0.09	0.69	48%	2.1 X
0.065	0.72	52%	1.9 X
0.045	0.69	48%	2.1 X
0.032	0.71	51%	2.0 X

Cost Reduction Keeps Ecosystem Healthy

Foundry
- Potential ~2X transistors per wafer

Fabless Companies
- Achieves ~1.7X transistors in design

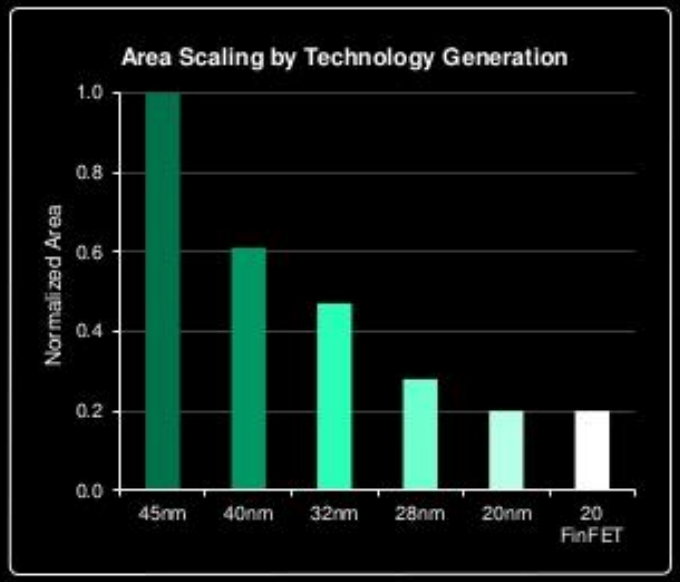


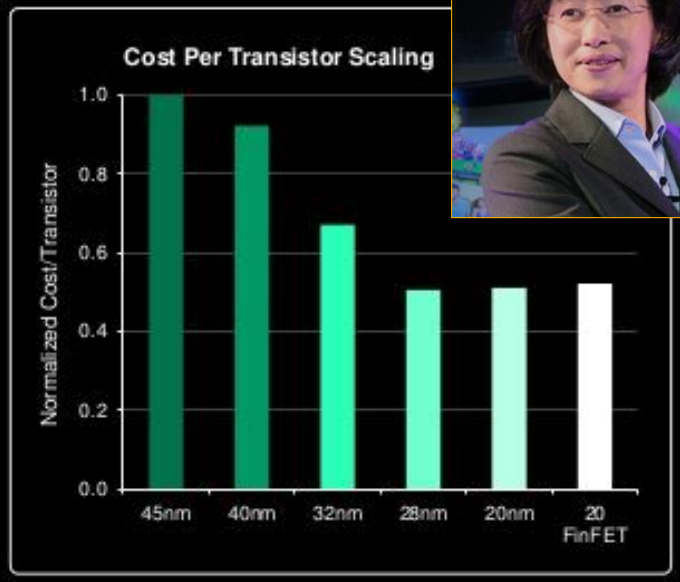
Capital Equipment
- 35%/yr decrease in depreciation per transistor

End User
- ~1.7X functionality
- Same price as previous generation

...Until the 20nm Node?

CHALLENGES TO MOORE'S LAW SCALING





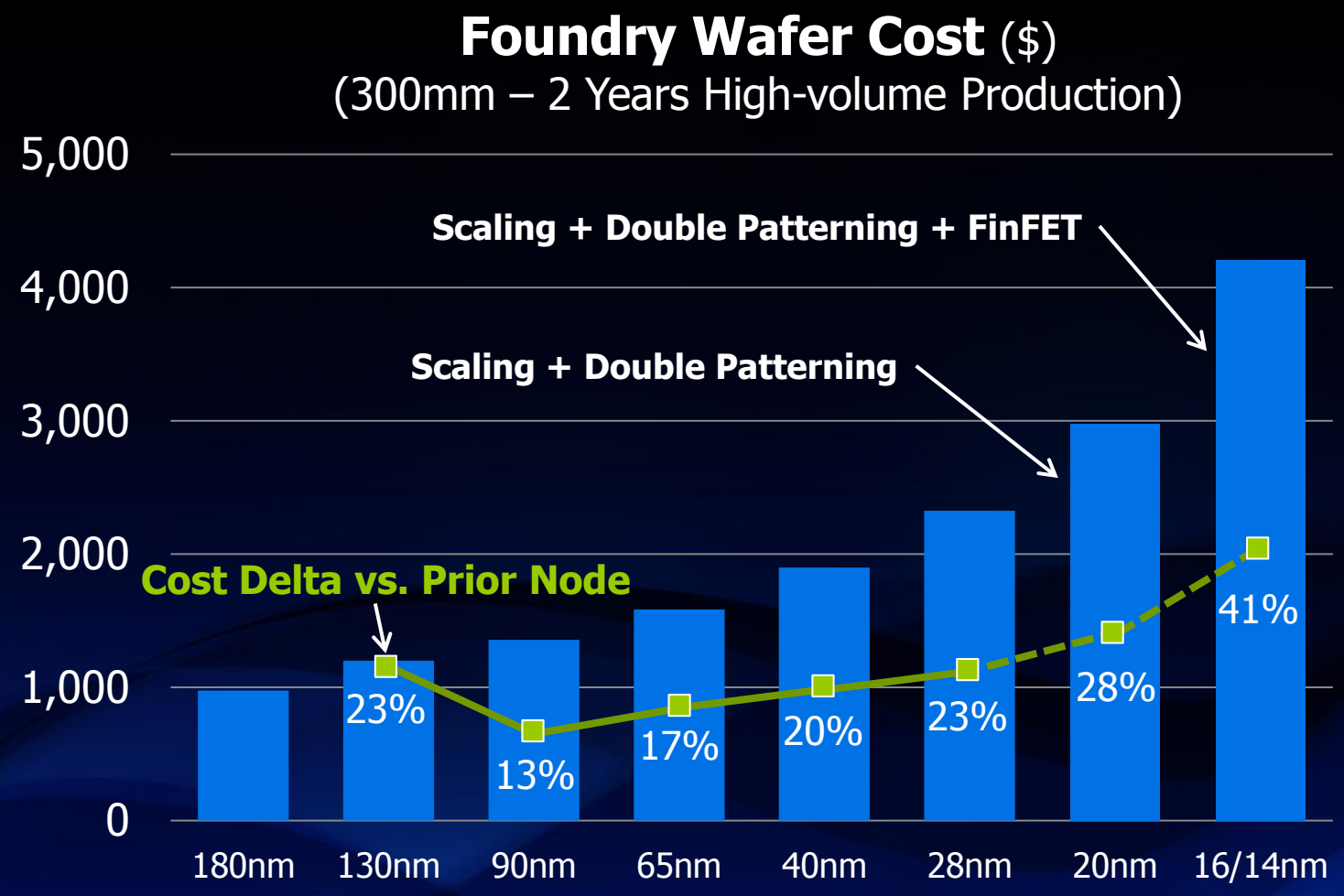
- Lithography challenges begin severely limiting area scaling at 20nm node

2 | ISSCC Keynote | February 18th, 2013

Lisa Su, AMD ISSCC '13 Keynote

"No cost/transistor crossover for first time at 28→ 20nm transition"

Traditionally, Cost-per-Wafer Increases 15-20% at Each New Technology Node



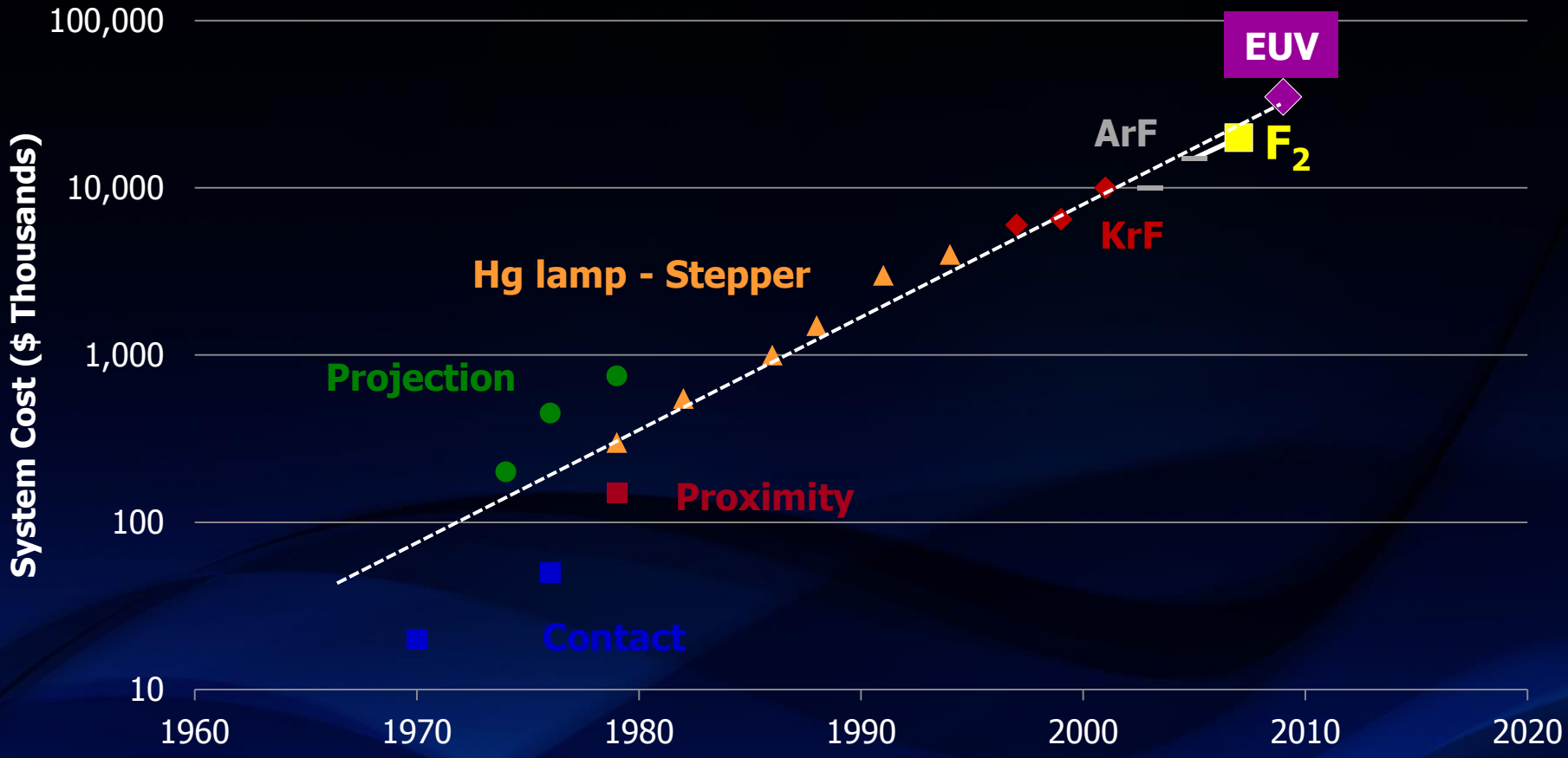
Source: IBS, IC Insights, Mentor Graphics Analysis

What's Happening at 20nm and Beyond?

20nm	Additional cost of double pattern/etch
14/16nm	FinFET More double pattern/etch EUV delay
10nm	FinFET More double pattern/etch Triple pattern/etch SADP layers More EUV delay

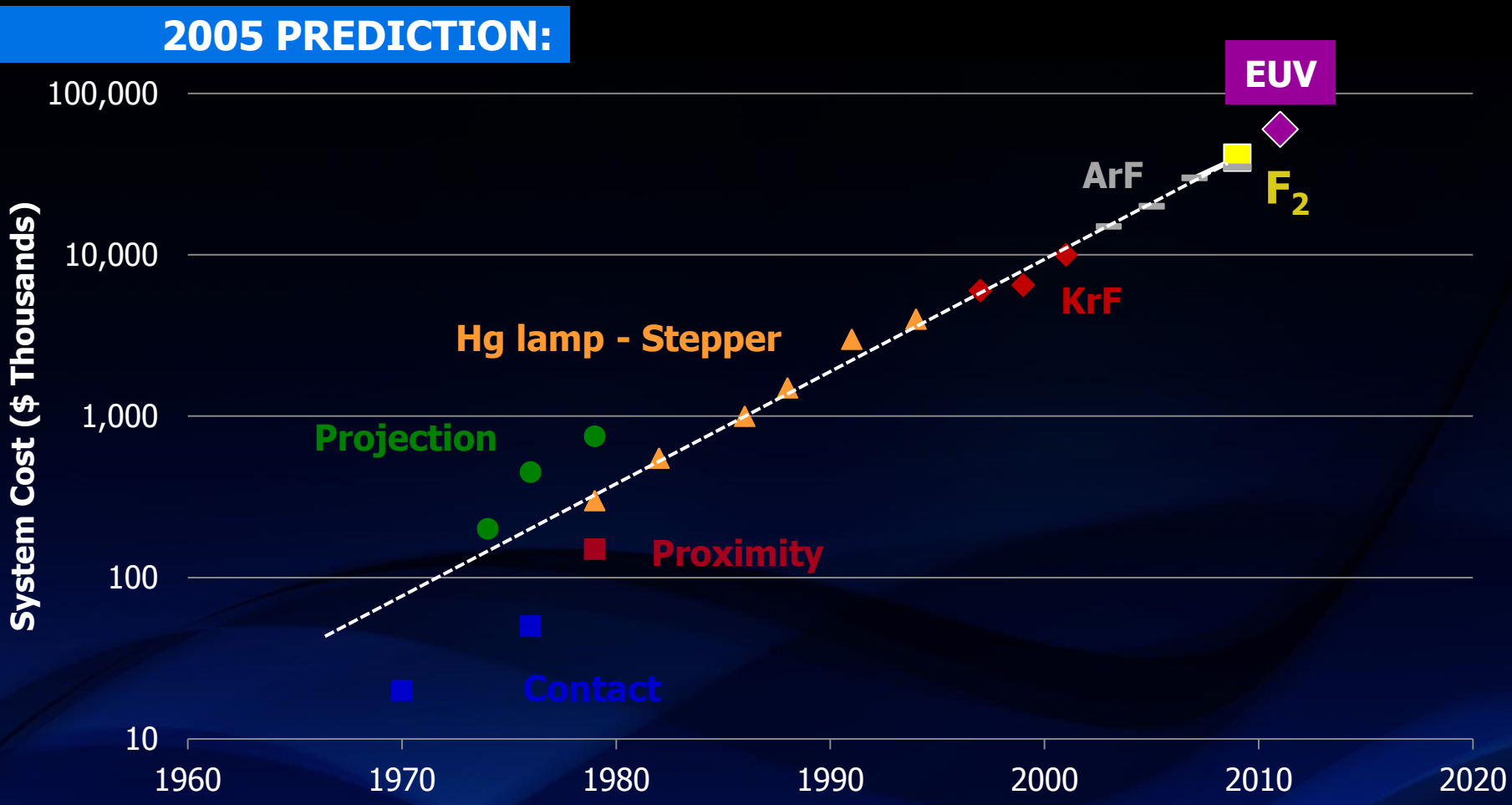
Move to 157nm in 2007 and EUV in 2009

2003 PREDICTION:



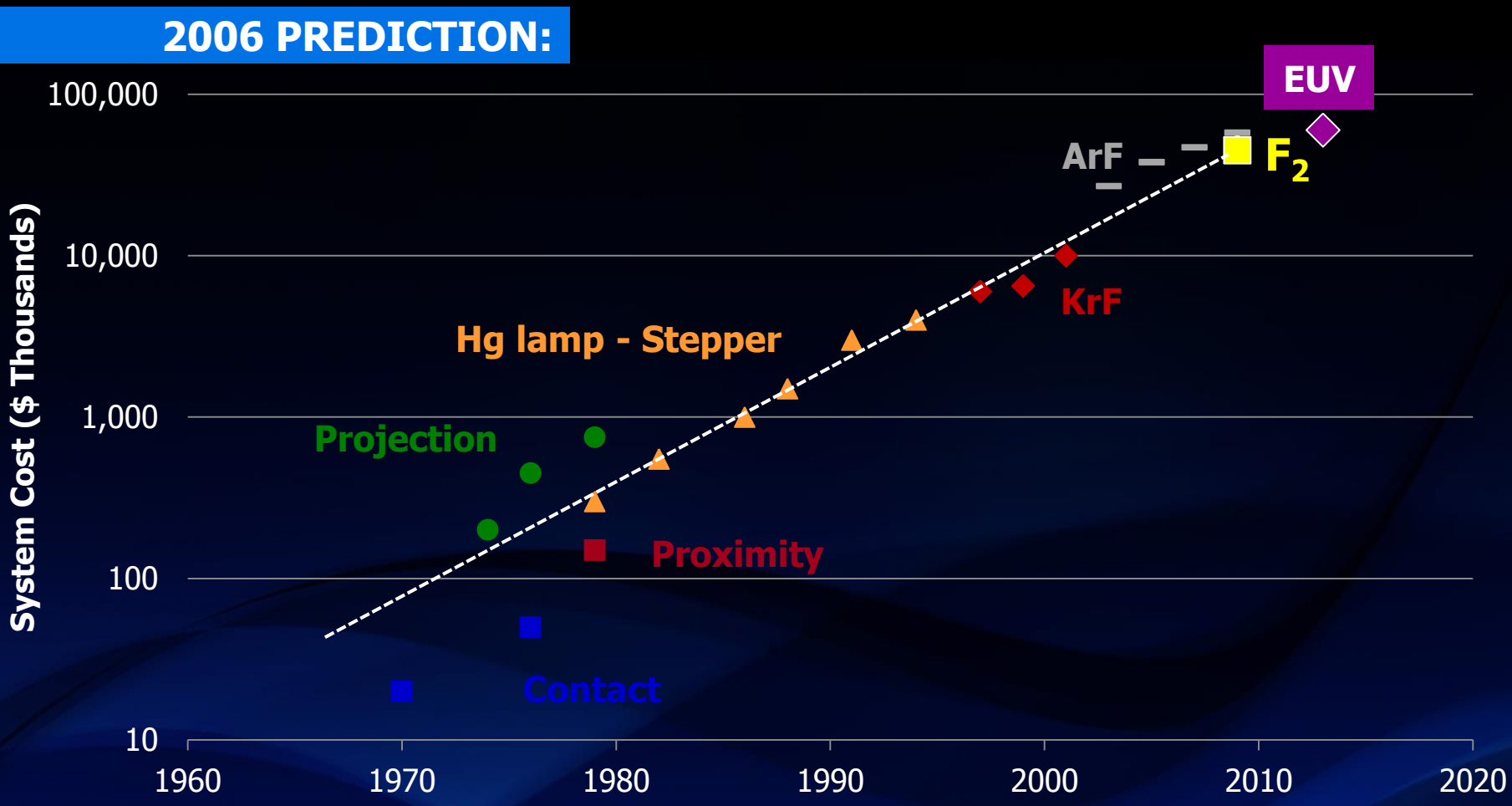
Source: Industry Sources, 2003

2-Year Slip in 2 Years — Analysts' Prediction: 157nm in 2009 & EUV in 2011



Source: Industry Sources, 2005

Another 2-Year Slip in Only 1 Year
Analysts' Prediction: EUV in 2013

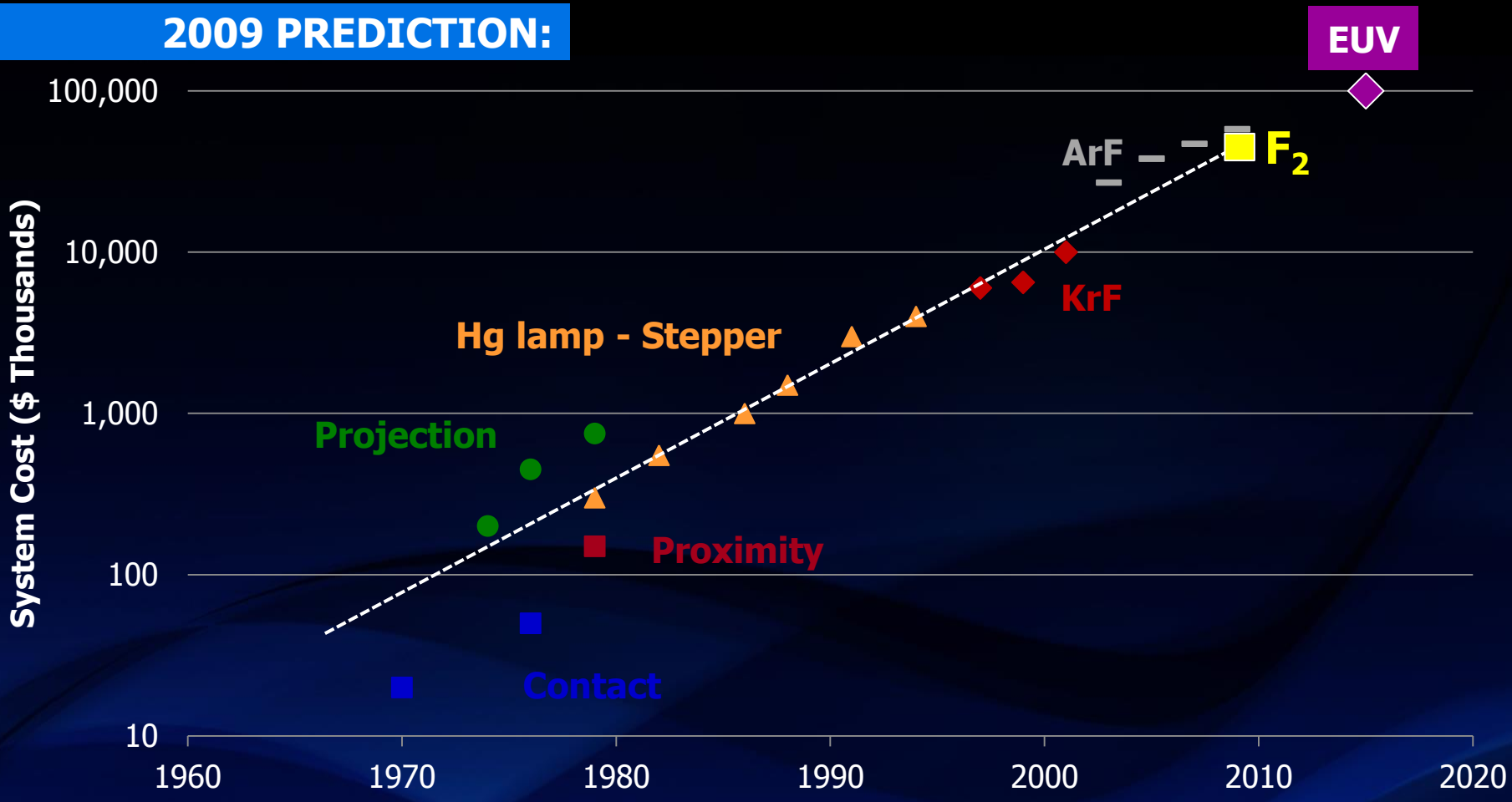


Source: Industry Sources, 2006

157nm Misses the Adoption Window…*

EUV Volume Production 2015

2009 PREDICTION:



Source: Industry Sources, 2009

Some Progress, But a Long Way to Go

ASML customers 'intensify' EUV development

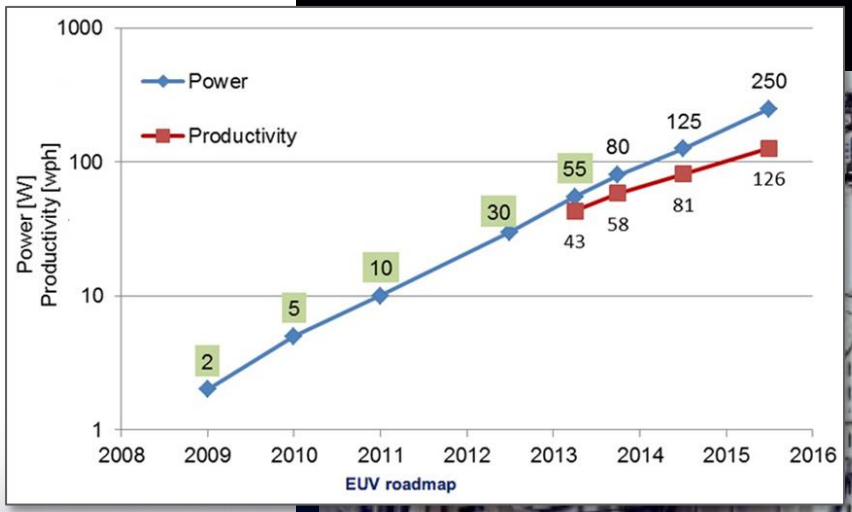
17 Jul 2013 optics.org

Extreme ultraviolet sources now routinely supporting 40 wafers per hour throughput, says the lithography company.

ASML has reiterated its confidence in the successful deployment of extreme ultraviolet (EUV) lithography by chip manufacturers over the next few years, with **outgoing CEO Eric Meurice** saying that the technology had "confirmed" its capability for the forthcoming 10 nm node in logic applications.

Key light source developer Cymer is **now a division of ASML** after the Netherlands-based company decided to in-source that capability following a period of under-investment in EUV. Cymer reported earlier this year that it had reached an EUV output of 55W – enough to support the production of 40 wafers per hour.

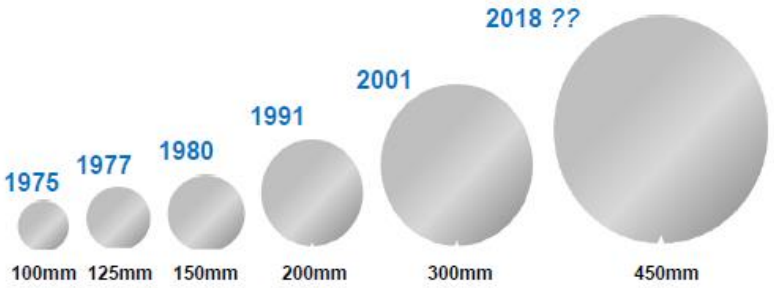
During a conference call to discuss ASML's latest financial results, Meuri... ...routinely" running at 55 W and with the sort of reliability and consist...



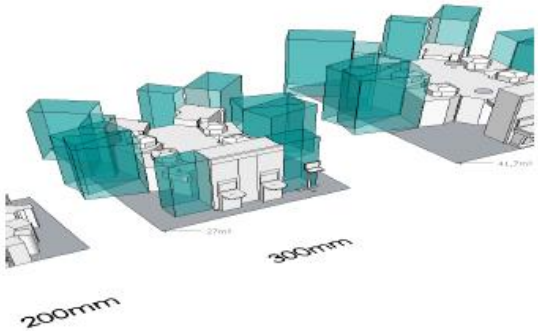
Source: ARS Technica, 8/7/2013

What about 450mm Cost Savings?

450mm Transition



Wafer Transition	Area Increase
100mm → 125mm	56%
100mm → 150mm	125%
125mm → 150mm	44%
150mm → 200mm	78%
200mm → 300mm	125%
300mm → 450mm	125%



SEMI Industry Strategy Symposium (ISS) - January 15, 2013: Intel Corporation executives make first public presentation of 450mm silicon wafer patterned with 26nm features using nano imprint lithography.

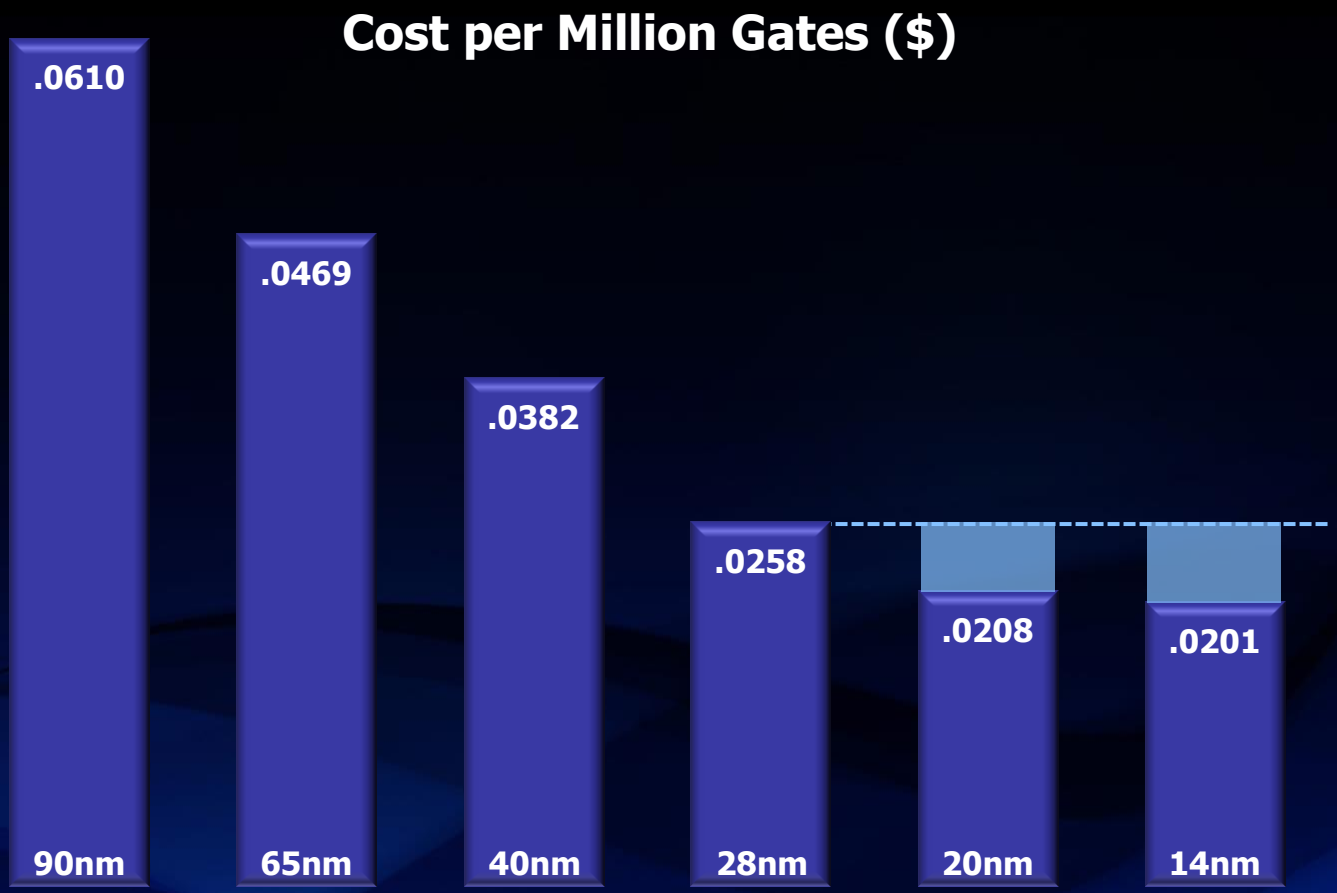
Wafer Diameter Helps Cost

- 2.0 – 2.3 X number of devices (2.25x wafer area)
- Economies of scale with fewer factories
- Lower device costs

Gross Dice per Wafer		
Die Size (mm)	450mm	Delta vs 300mm
1.0 x 1.0	134,357	**1.97 X**
2.0 x 2.0	35,857	**2.12 X**
3.0 x 3.0	16,241	**2.18 X**
5.0 x 5.0	5,889	**2.23 X**
7.0 x 7.0	2,997	**2.27 X**
10 x 10	1,449	**2.32 X**
20 x 20	337	**2.27 X**

Source: Intel, Applied Materials, IC Knowledge

450mm Wafer Impact — Significant but Too Little, Too Late



Source: IBS

WHOSE MARGIN GETS THE BIG SQUEEZE ?

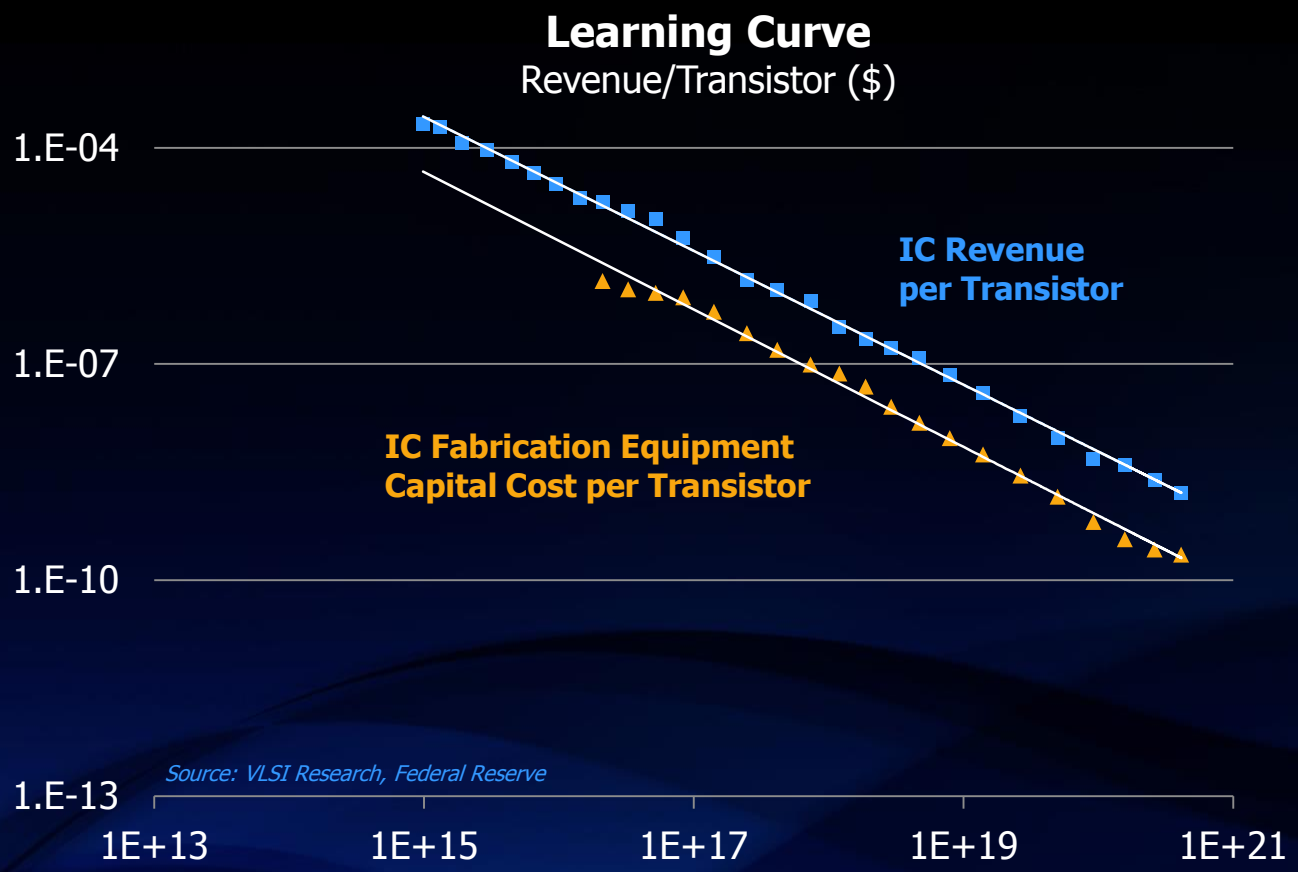
The Candidates

- "Food chain" suppliers (other than foundries)?
- Silicon foundries?
- Semiconductor companies?
- End users and system companies?

"Food Chain" Suppliers (other than Foundries)?

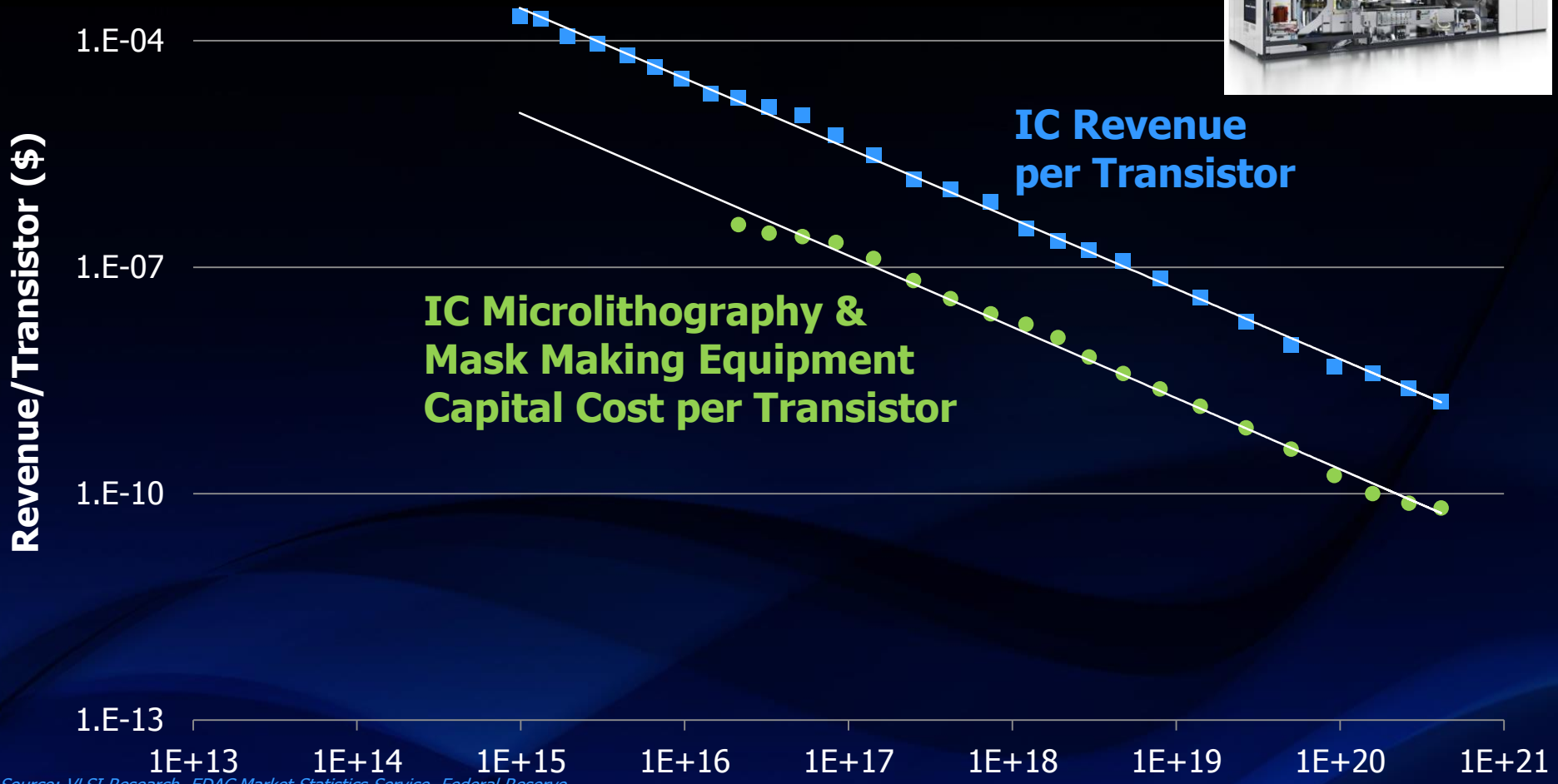
- Silicon foundries?
  - Wafer fab
  - Lithography
  - Assembly
  - Test
  - EDA software
- Semiconductor companies?
- End users and system companies?

IC Fabrication Equipment (Front End)



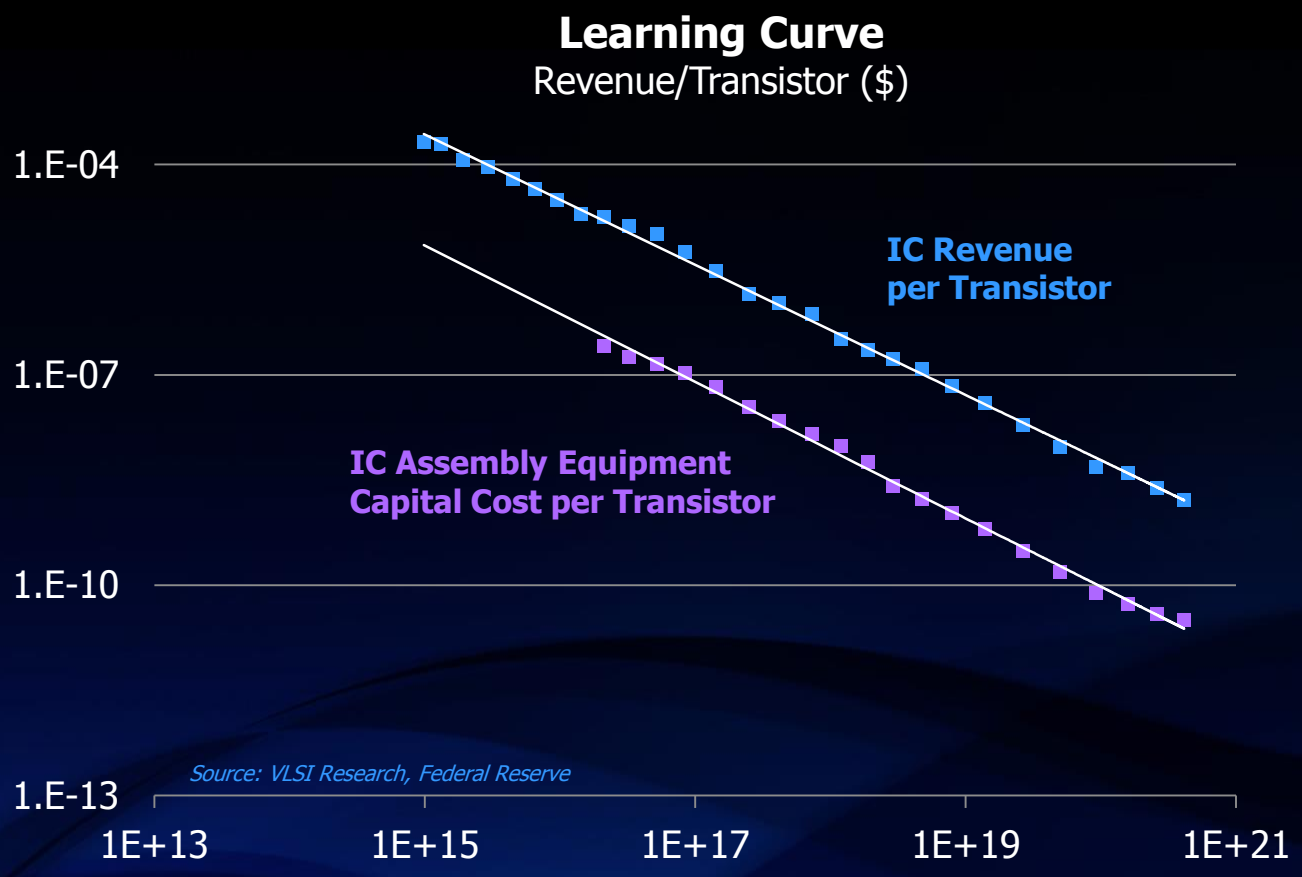
Note (Gross Profit Margin): Includes Applied Materials, ASML, Tokyo Electron, Lam, KLA-Tencor, Dainippon Screen, Hitachi Kokusai, Daifuku

Lithography & Mask Making Equipment



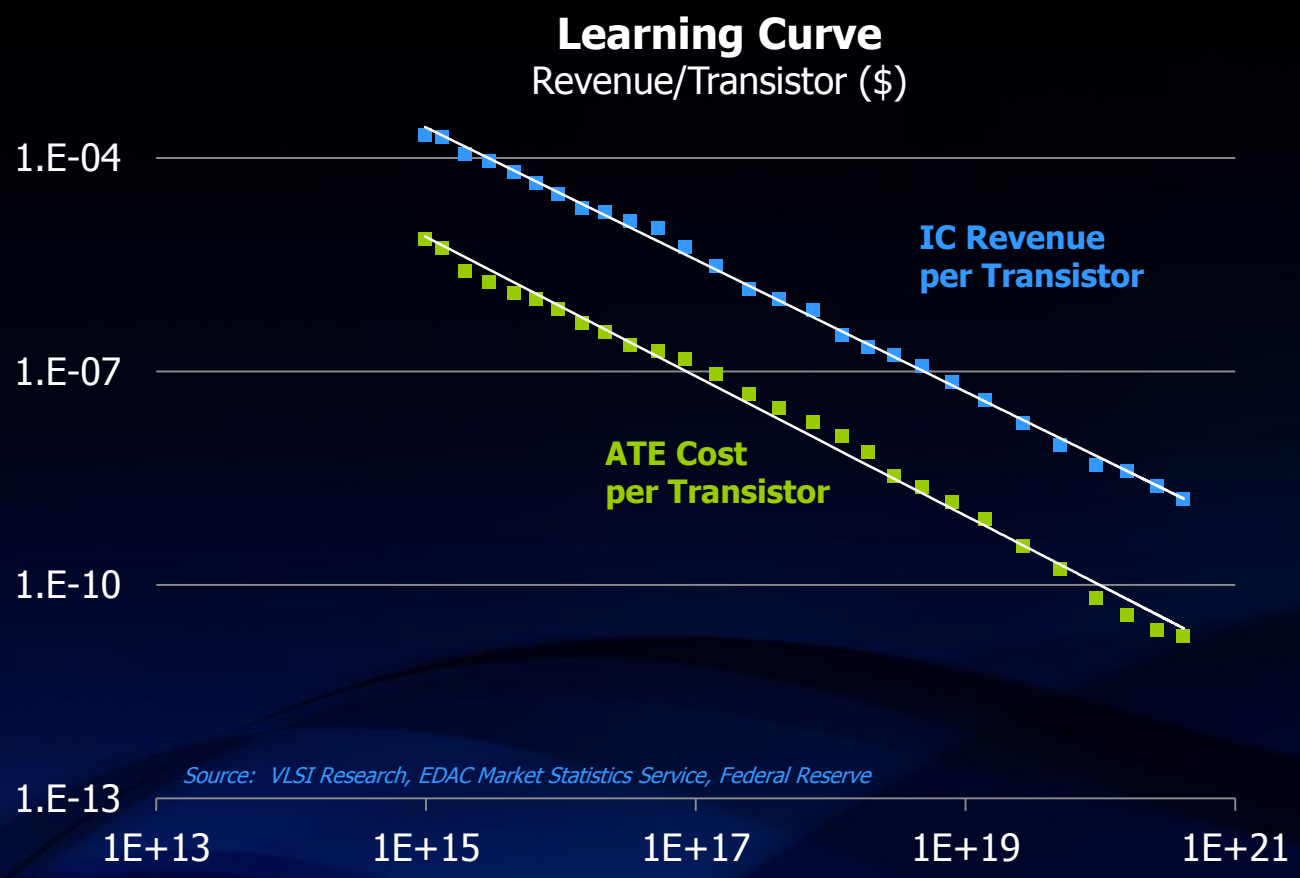
Source: VLSI Research, EDAC Market Statistics Service, Federal Reserve
Note: Revenue adjusted for Inflation... IC Revenue:1985-2012, Equipment Revenue: 1993-2012

Assembly Equipment



Note (Gross Profit Margin): Includes Kulicke & Soffa, ASM Int., DISCO Corp., BE Semiconductor, TOWA Corp., Shinkawa Ltd., Samsung Techwin, HANMI Semiconductor, KLA-Tencor, Rudolph Technologies

ATE Equipment



Note (Learning Curve): Revenue adjusted for Inflation… IC Revenue:1985-2012, Equipment Revenue: 1985-2012
Note (Gross Profit Margin): Includes Advantest, Teradyne, Tokyo Seimitsu, Tokyo Electron, LTX – Credence, FEI Company

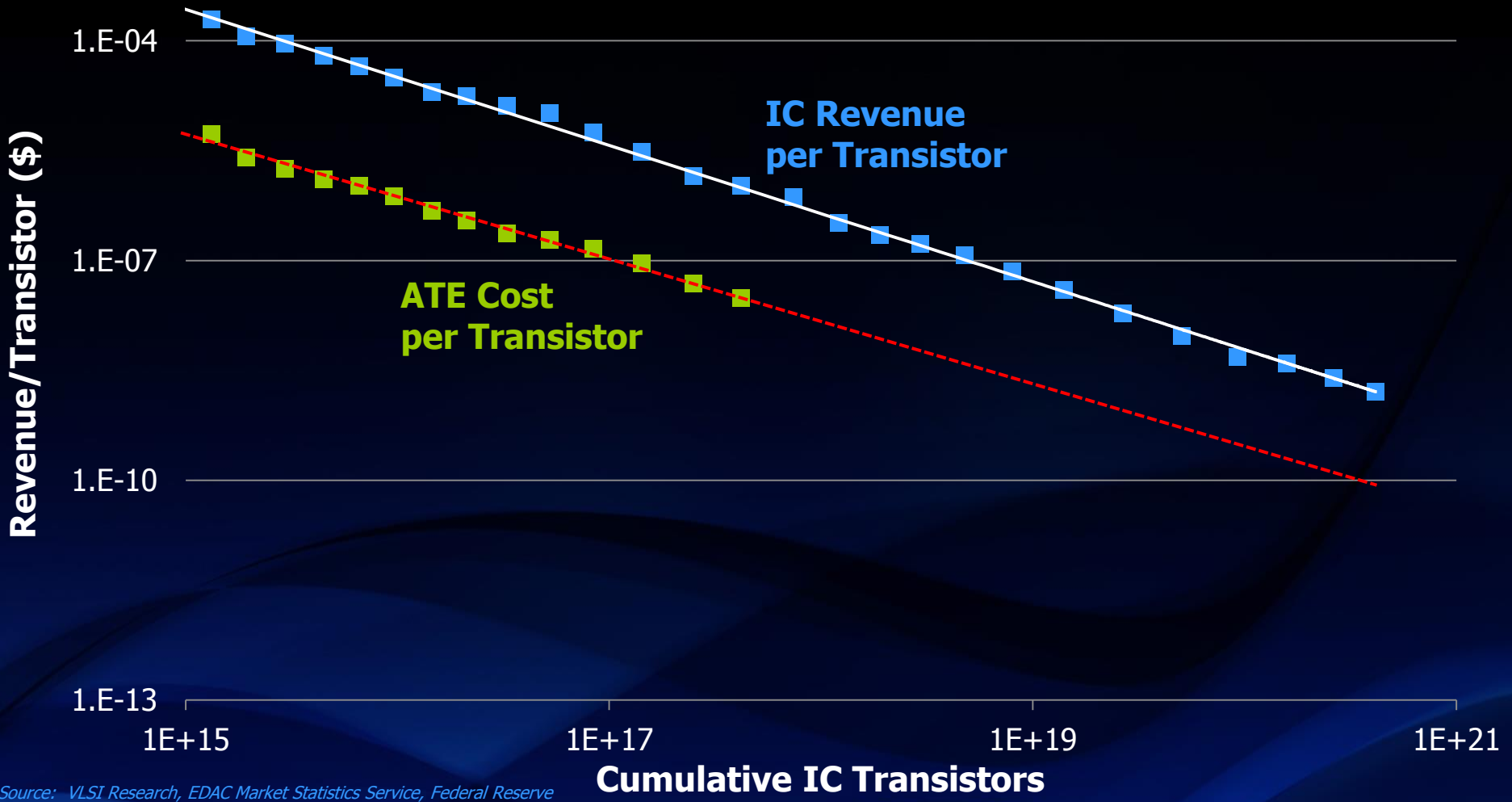
Ten Years Ago, ATE Cost per Transistor Was Not Keeping Up with the IC Learning Curve

"It may cost more to test a transistor than it costs to manufacture the transistor."

1999 ITC Keynote: Pat Gelsinger, Intel CTO

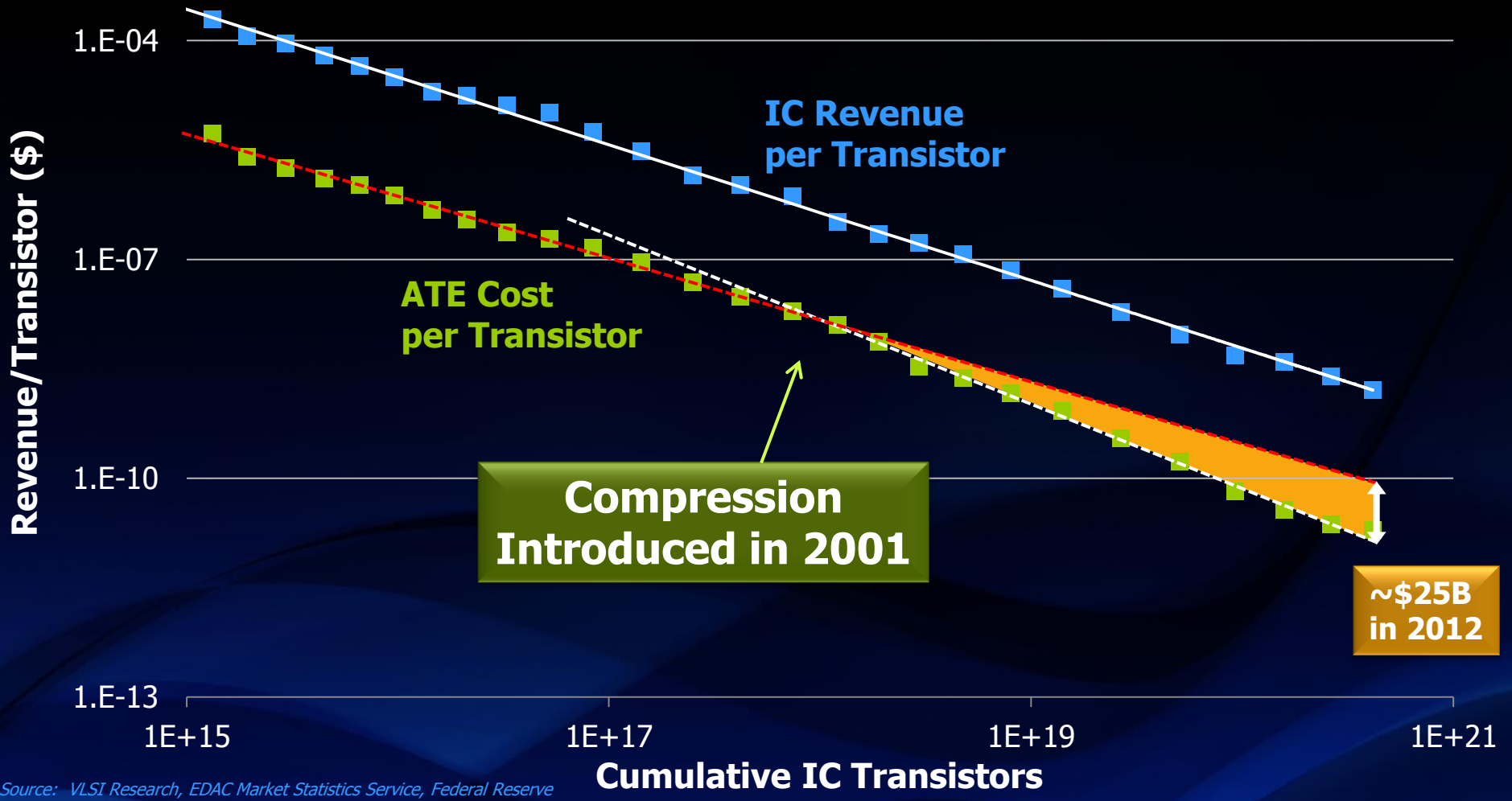
IC Economics – 2003 Edition,
Chapter 9 page 97
ICKnowledge.com

...Providing a Warning of a Need for Major Innovation



Source: VLSI Research, EDAC Market Statistics Service, Federal Reserve
Note: Revenue adjusted for Inflation... 1985-2012

Compression Realigns ATE Costs



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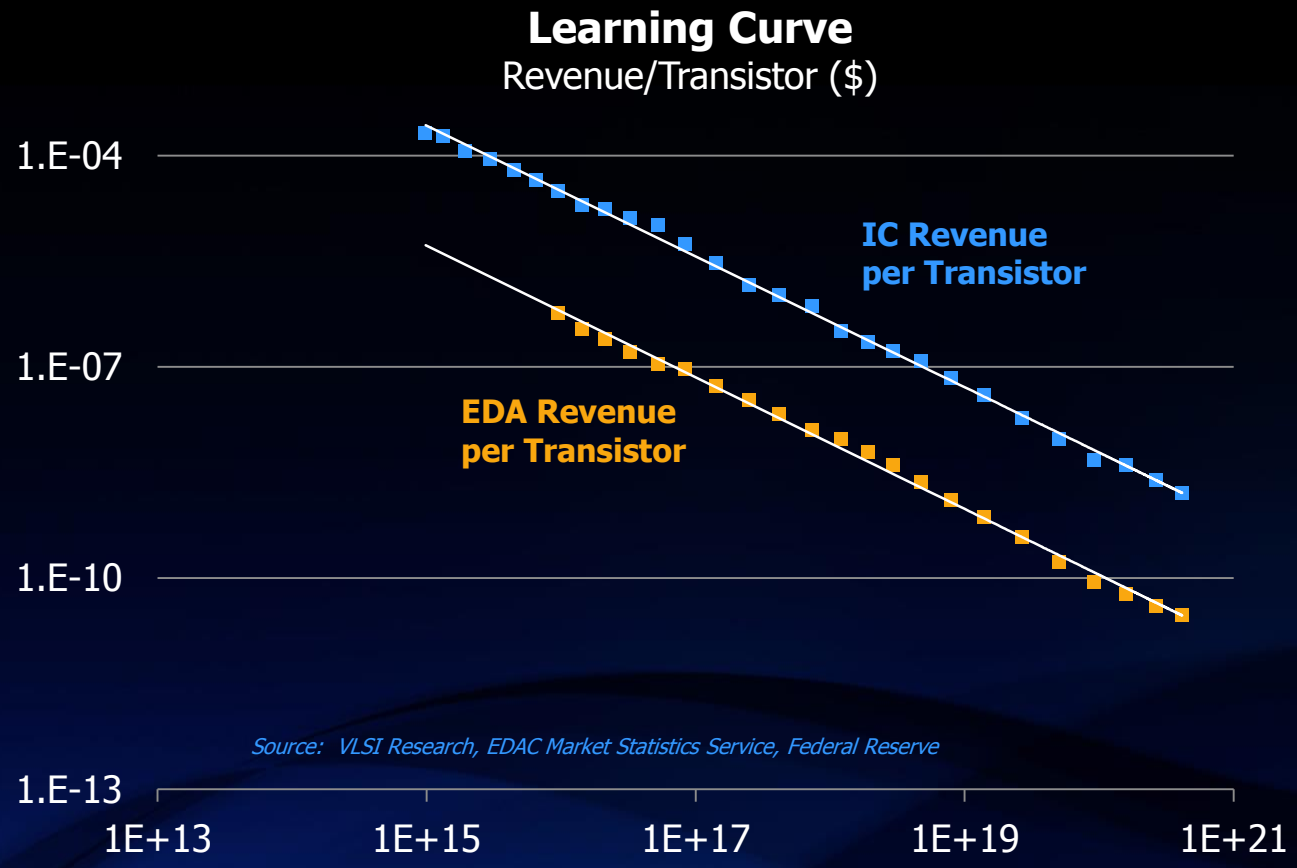
What about the EDA Tools Cost?



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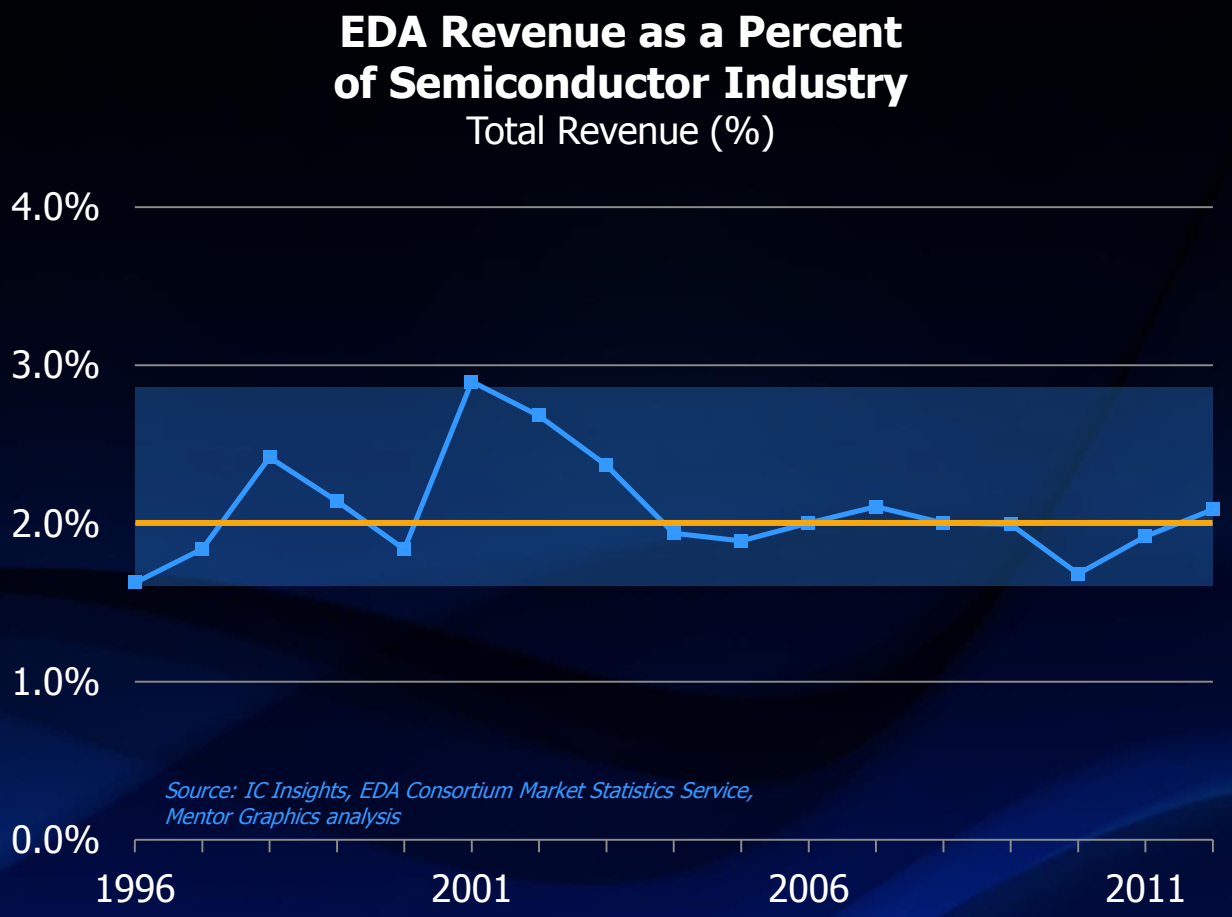

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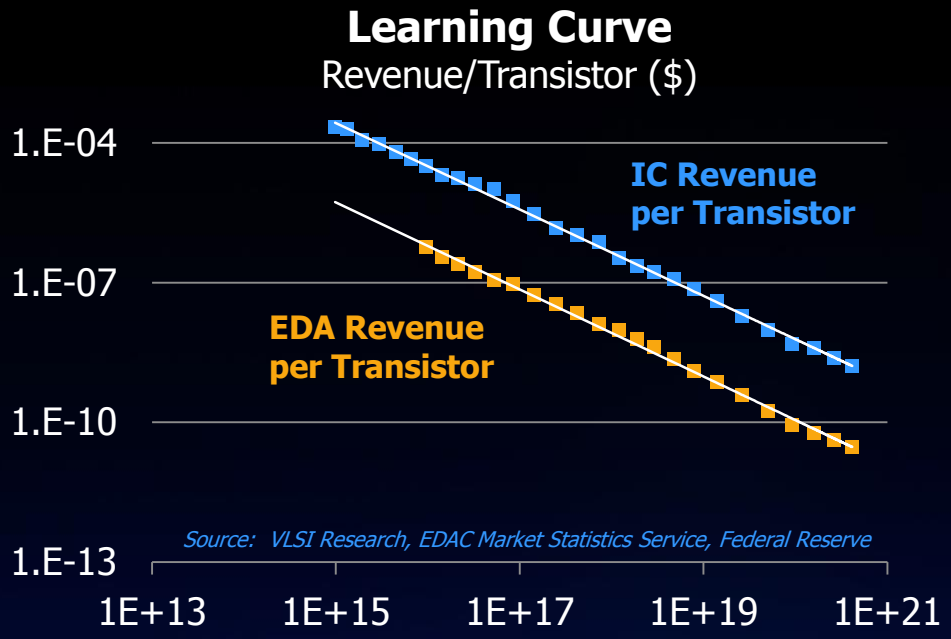
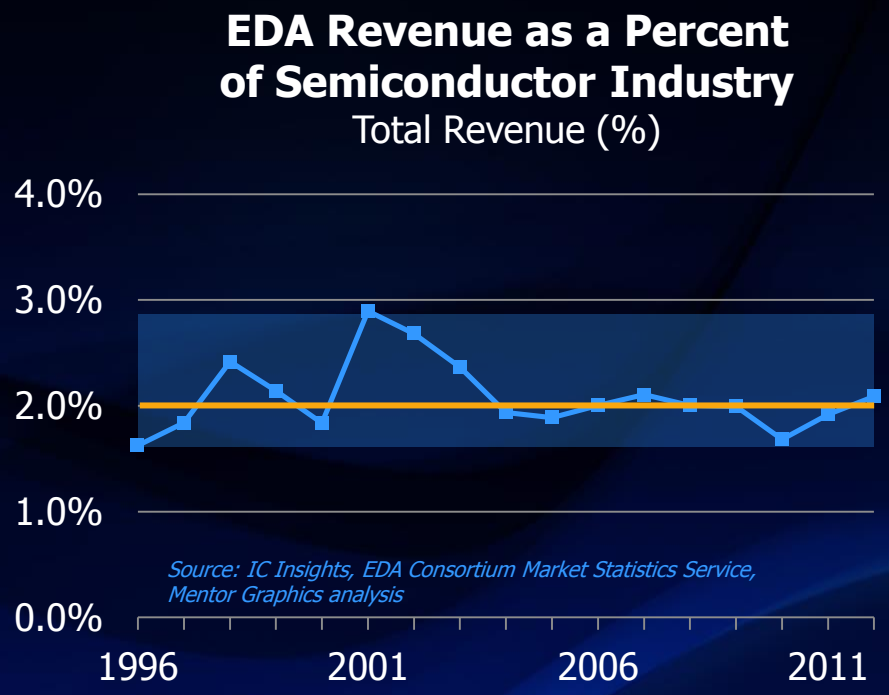
What about the EDA Tools Cost?





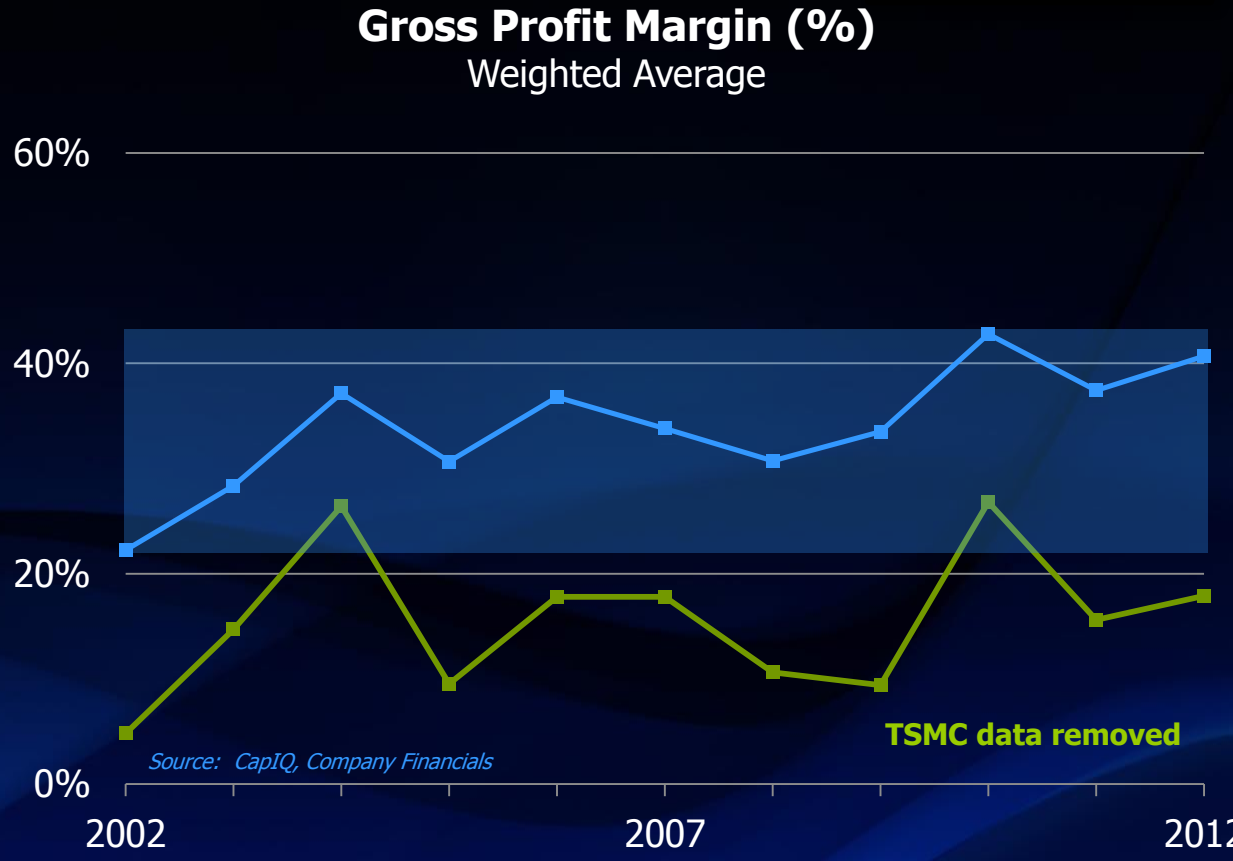
Note (Learning Curve): Revenue adjusted for Inflation… 1985-2012

- "Food chain" suppliers (other than foundries)?
- **Silicon Foundries?**
- Semiconductor companies?
- End users and system companies?

Foundry

Note (Gross Profit Margin): Includes TSMC, SMIC, Chartered, UMC

Foundry



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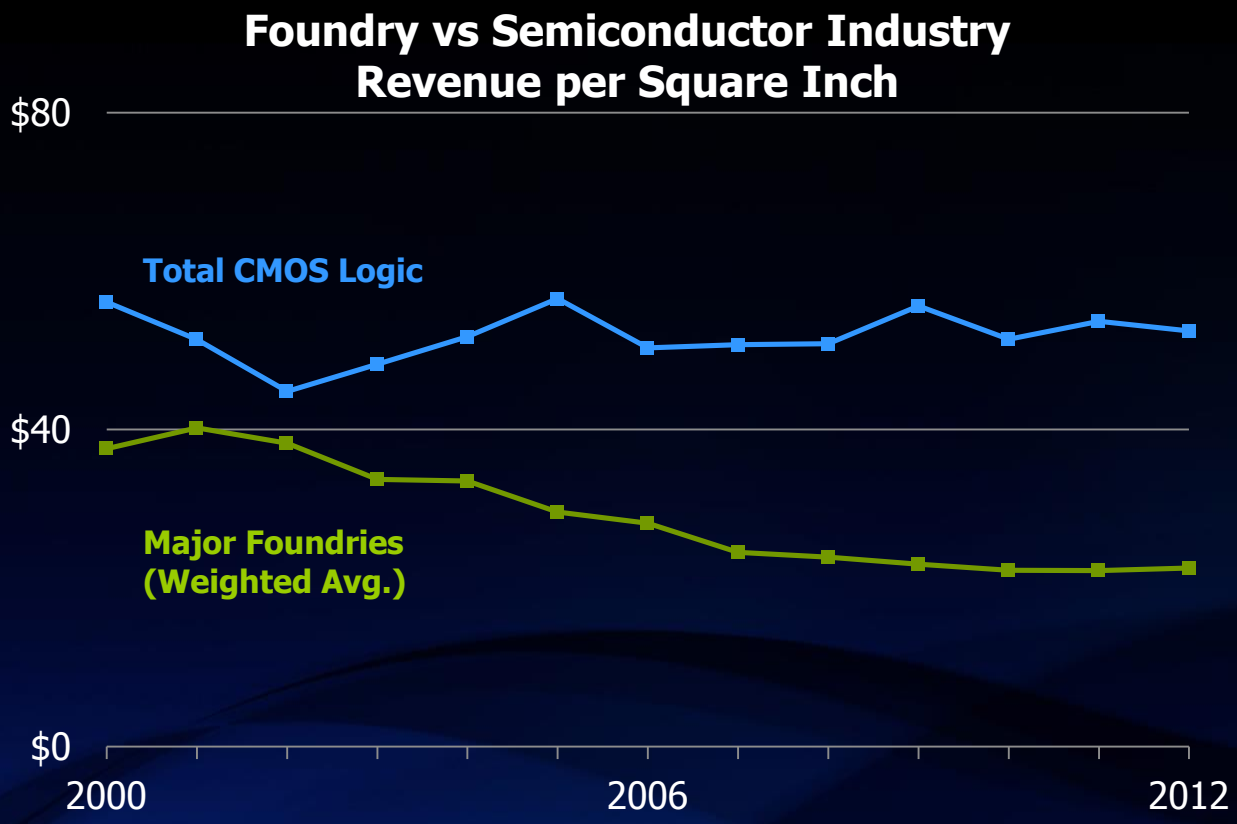
Foundry



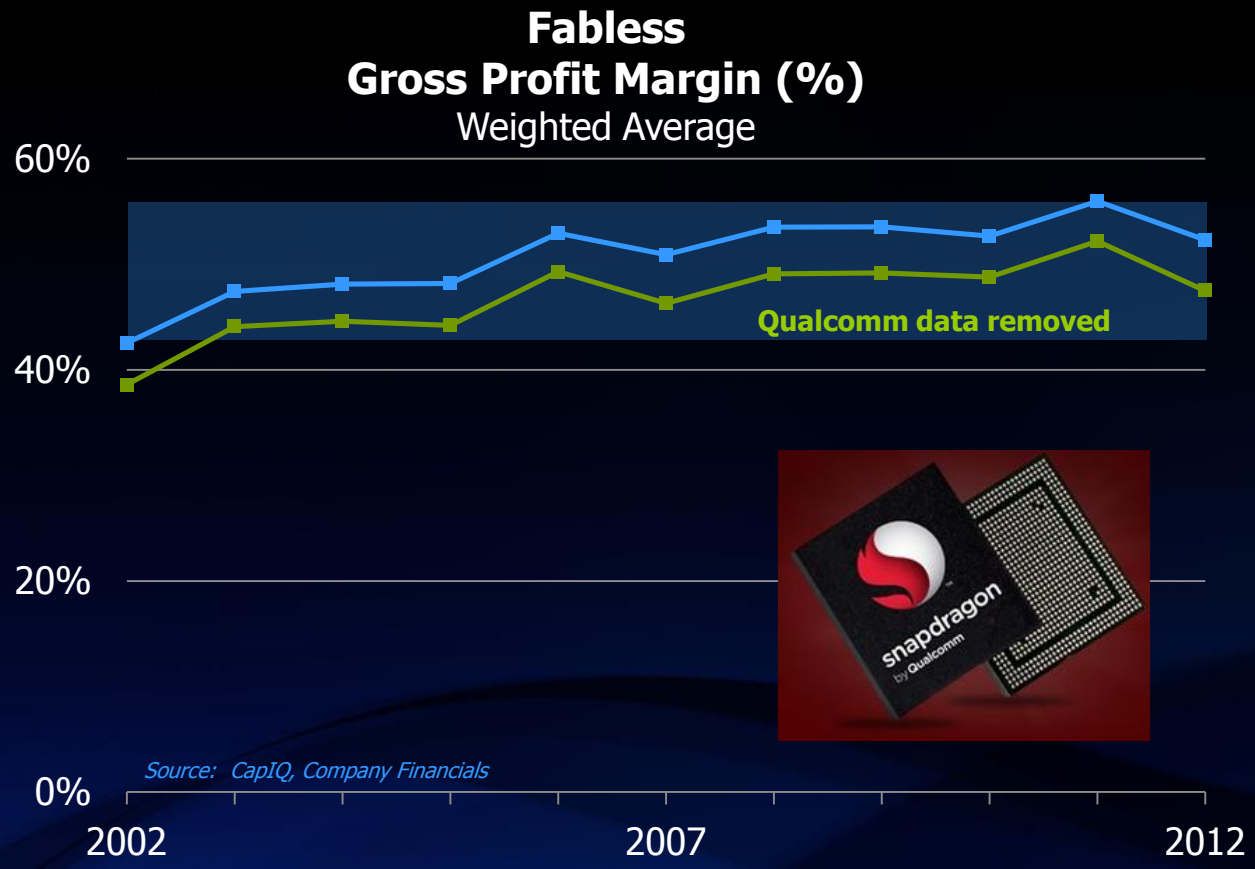
Note (Gross Profit Margin): Includes TSMC, SMIC, Chartered, UMC

- "Food chain" suppliers (other than foundries)?
- Silicon foundries?
- **Semiconductor Companies?**
- End users and system companies?

Fabless and IDM

Note (Fabless Gross Profit Margin): Includes 31 fabless semiconductor companies
Note (IDM Gross Profit Margin): Includes 16 IDM semiconductor companies

Fabless and IDM



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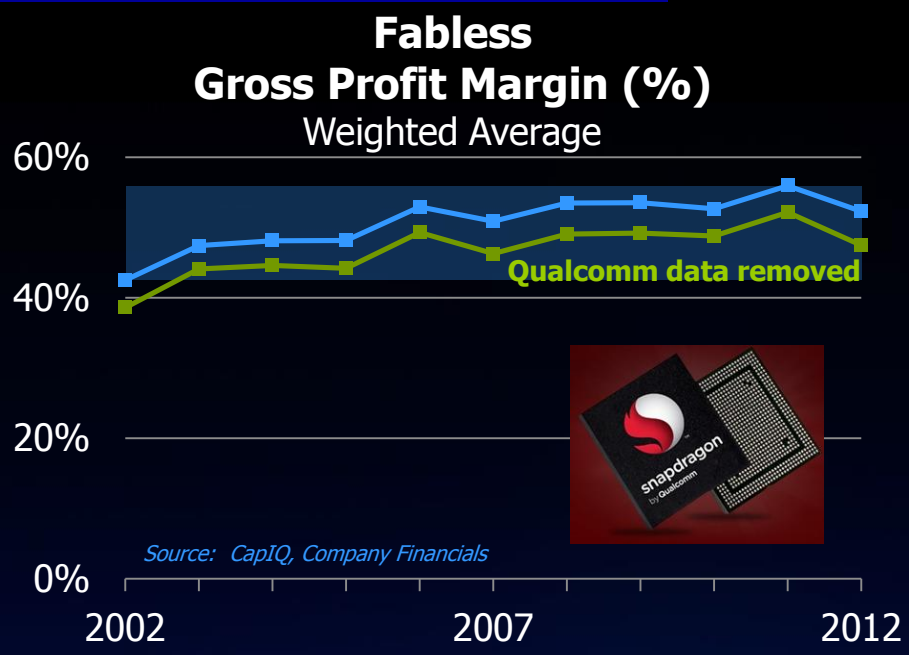
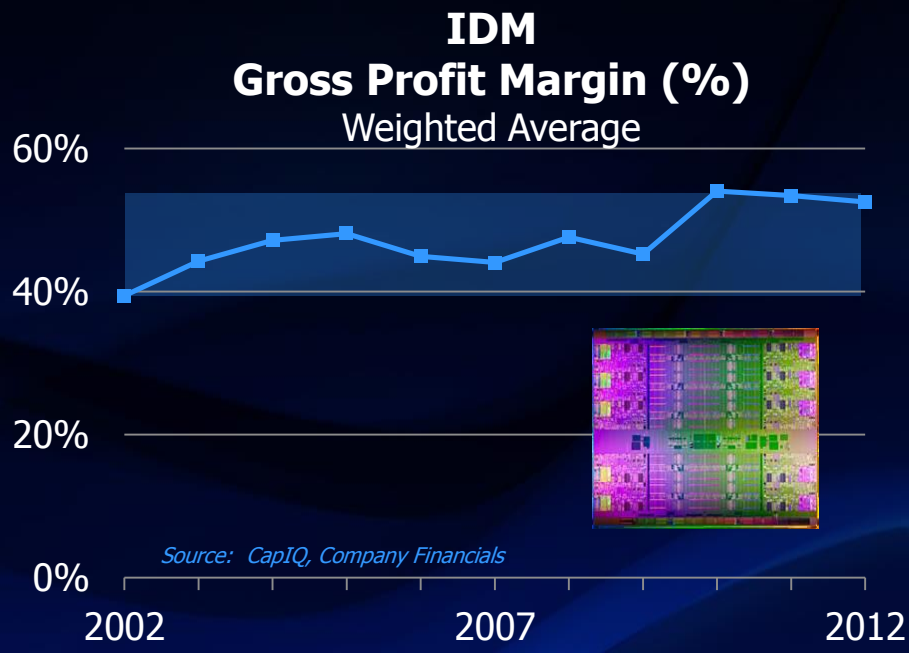
Note (IDM Gross Profit Margin): Includes 16 IDM semiconductor companies

Fabless and IDM

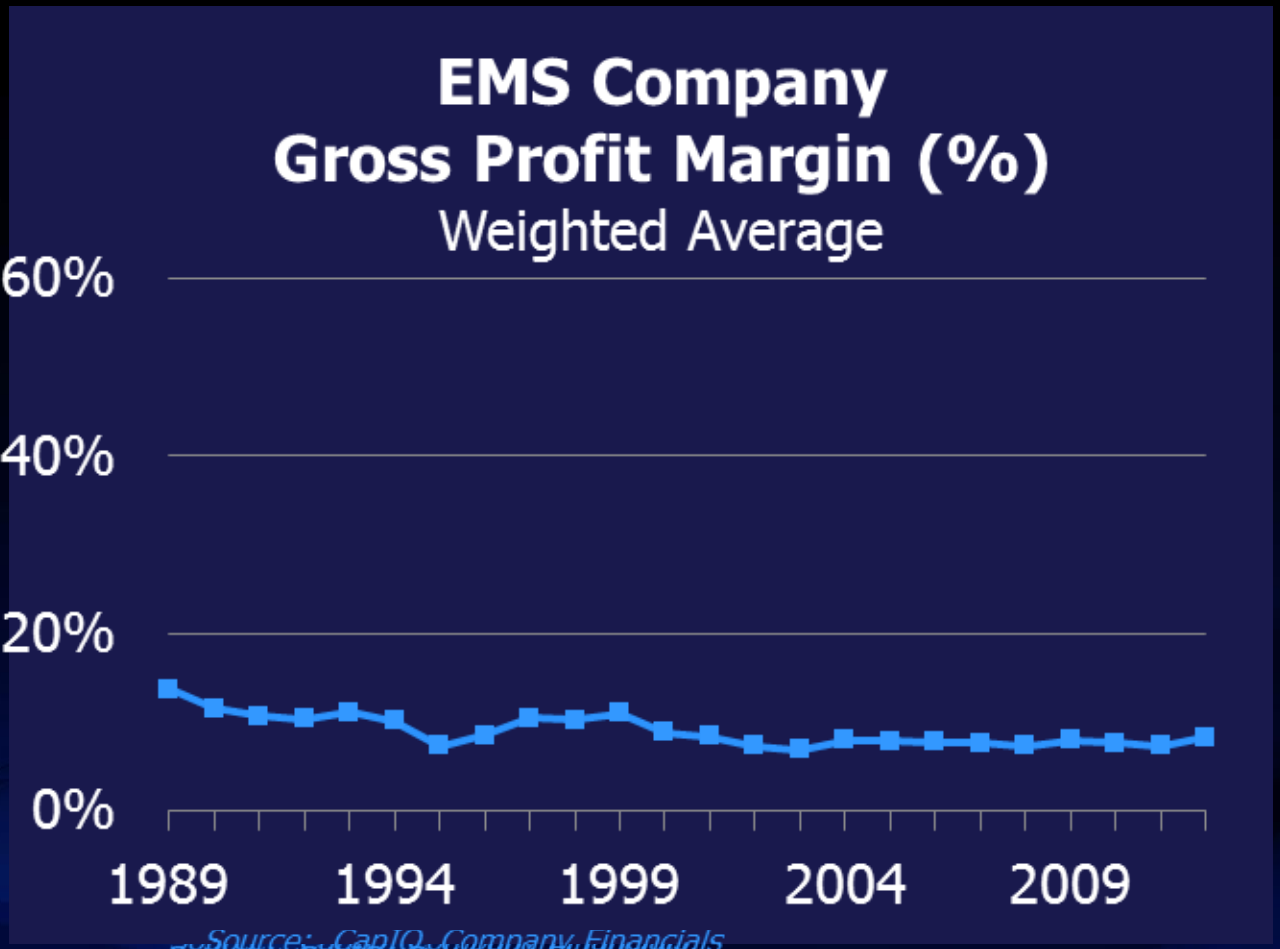




Note (Fabless Gross Profit Margin): Includes 31 fabless semiconductor companies
Note (IDM Gross Profit Margin): Includes 16 IDM semiconductor companies

- "Food chain" suppliers (other than foundries)?
- Silicon foundries?
- Semiconductor companies?
- **End Users and System Companies?**
  - Mobile Phones
  - Computers
  - Electronics Manufacturing Suppliers (EMS)

End User



Source: CapIQ, Company Financials
Note: Includes Hon Hai, Jabil Circuits, Plextronics, Sanmina, Celestica, Cal-Comp, Benchmark, Plexus, Venture

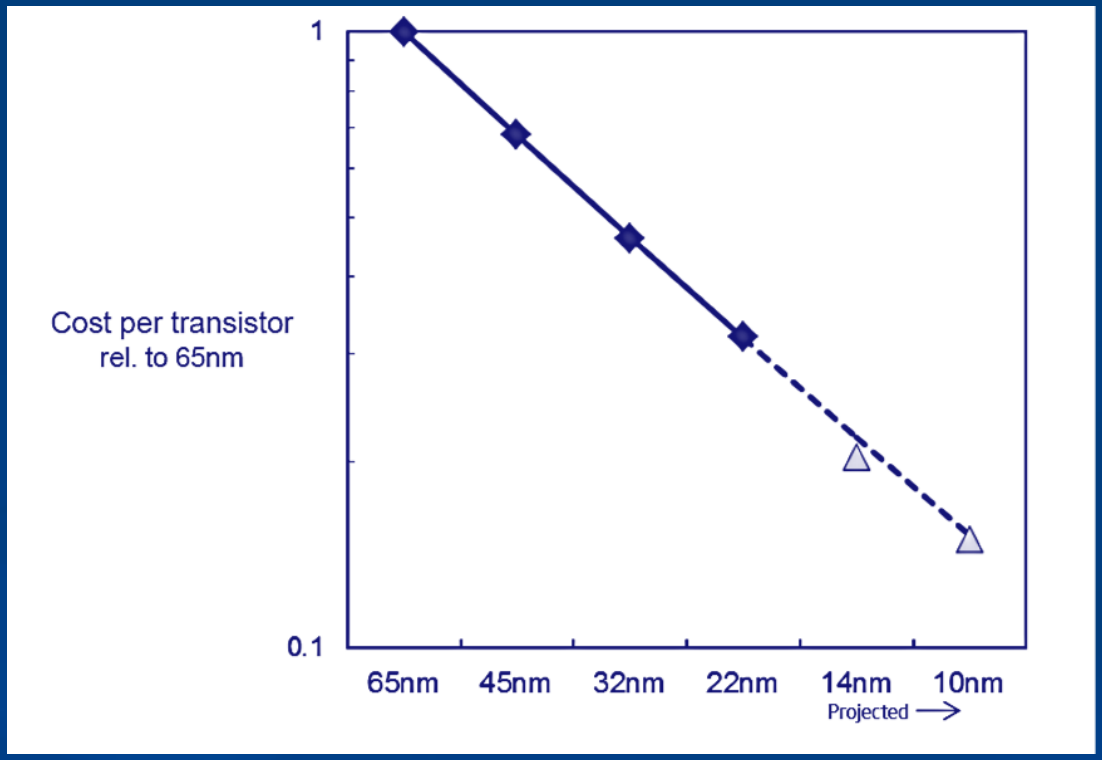
CAN WE GET THERE WITHOUT SQUEEZING MARGINS?

Other Possibilities

- **Silicon Foundry Innovations?**
- Slow down the learning curve?
- New innovations

Intel Predicts Wafer Fabrication Cost Solution

Density Scaling Enables Continued Cost Improvement

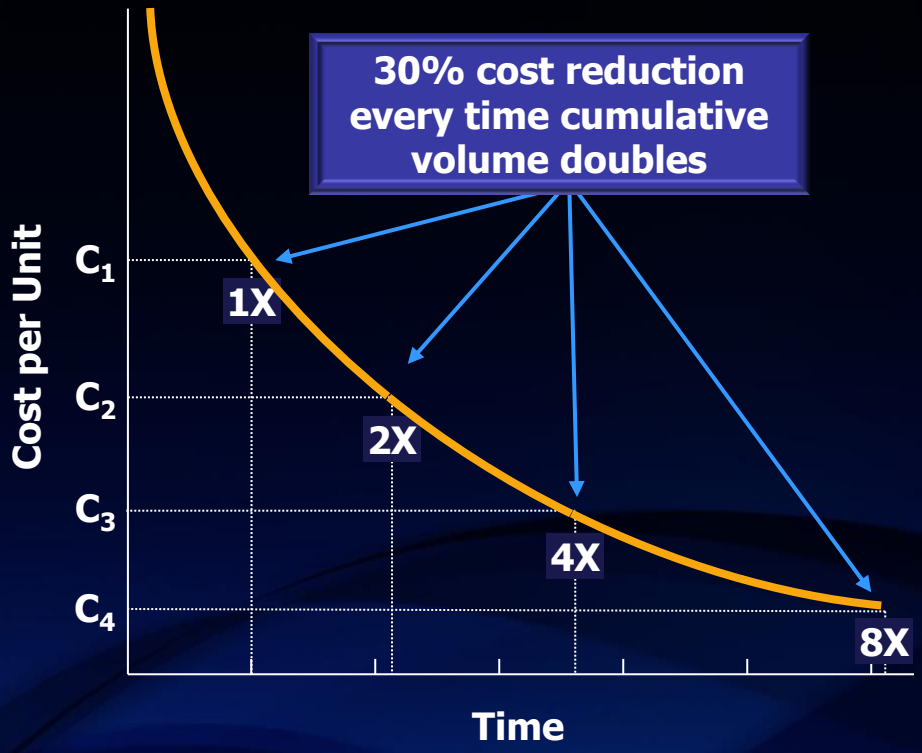


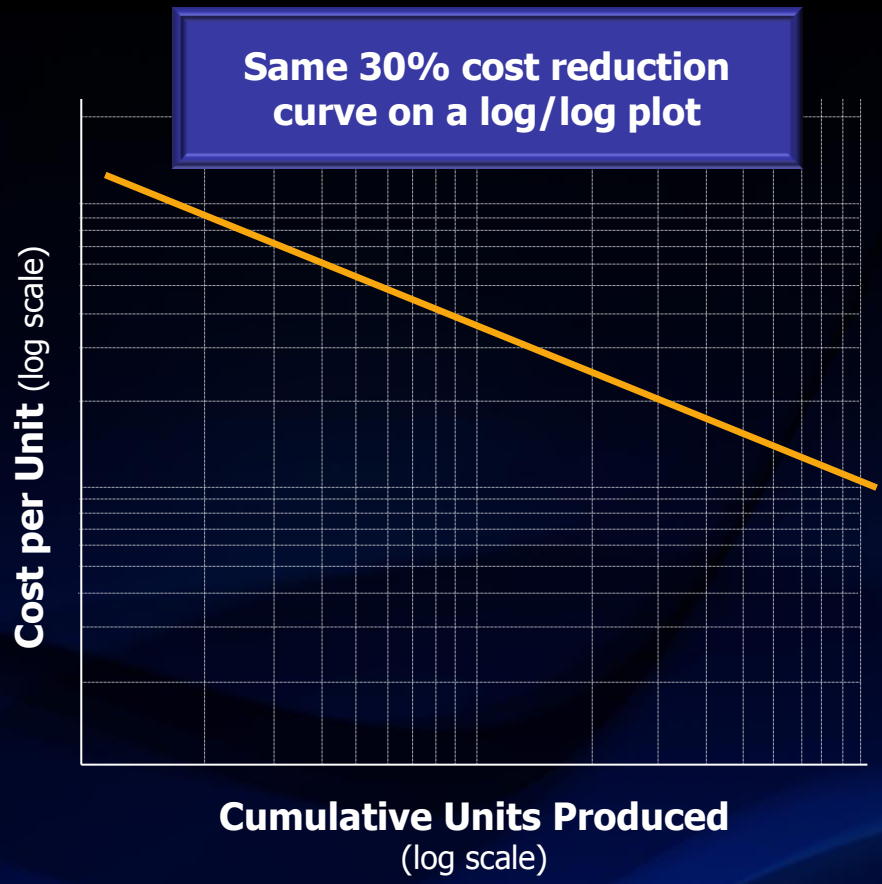
Source: William Holt, Intel Inc. May 7, 2013

Other Possibilities

- Silicon foundry innovations?
- **Slow Down the Learning Curve?**
- New innovations

Unit Cost Is a Function of Cumulative Unit Volume





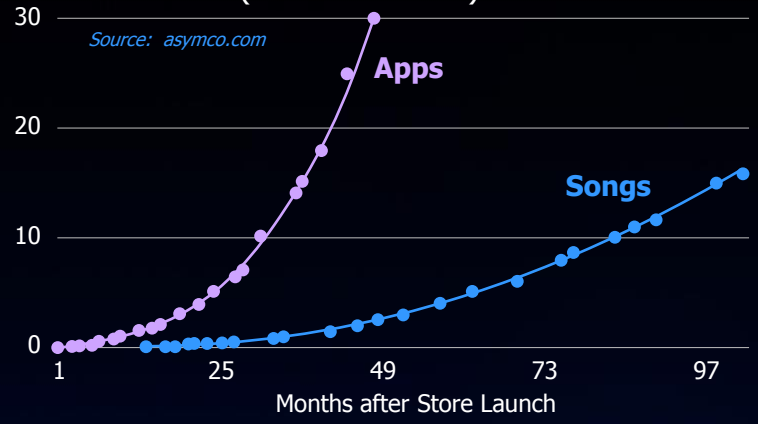
Semiconductors

Growth in Unit Volume Distinguishes Semiconductors from Other Industries Because of Insatiable Appetite for Information

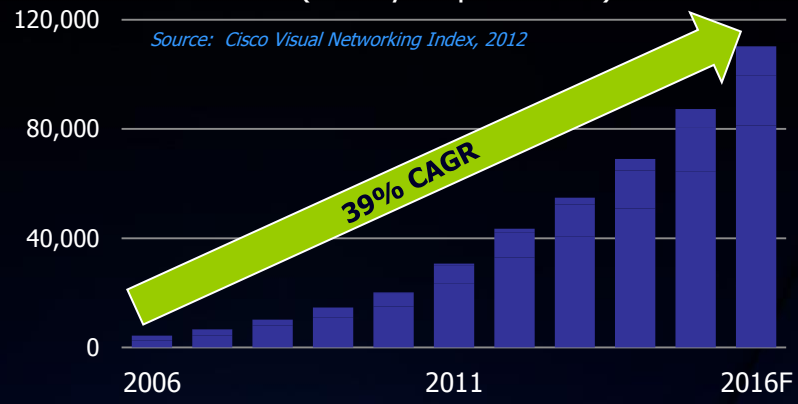
	Industry	10-Year CAGR
1	Crude Oil	1.1%
2	Aluminum	2.2%
3	Cotton	2.4%
4	Automotive	3.6%
5	Steel	5.8%
6	Computer	11.5%
7	Semiconductors	72% (Transistors)

Explosive Growth of Information

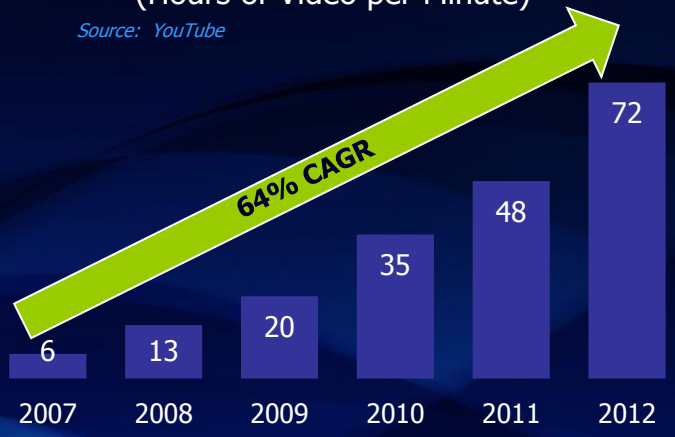
iTunes Downloads Totals
(Billions of Units)



Global IP Traffic
(Petabytes per Month)



Video Uploads to YouTube
(Hours of Video per Minute)



Tech. Capacity to Store Digital Data
Optimally Compressed Data (exabytes)

Source: Martin Hilbert and Priscila López, "The World's Technological Capacity to Store, Communicate, and Compute Information", Science,

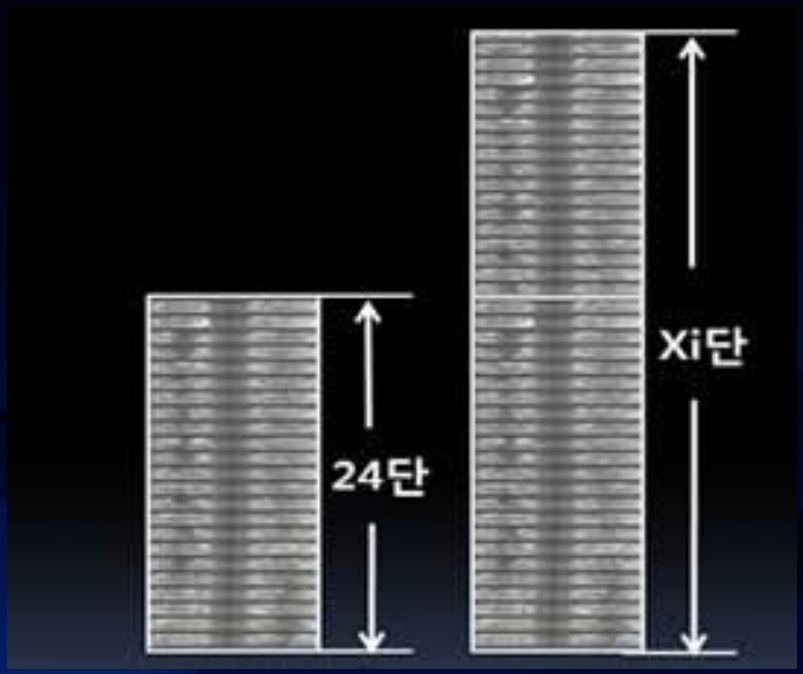
Other Possibilities

- Silicon foundry innovations?
- Slow down the learning curve?
- **New Innovations**

STAYING ON THE LEARNING CURVE DOESN'T REQUIRE MOORE'S "LAW" SCALING

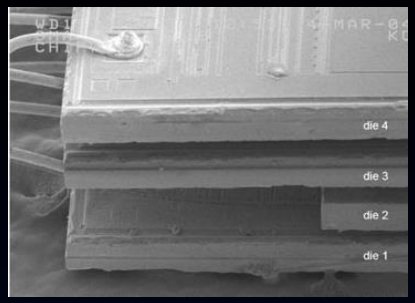
Growing Integrated Circuits Vertically

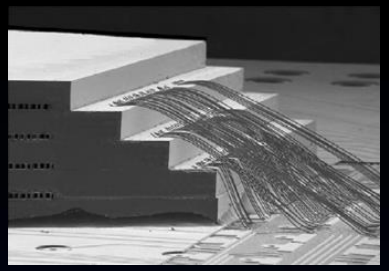
- Increasing chip density & functionality without scaling

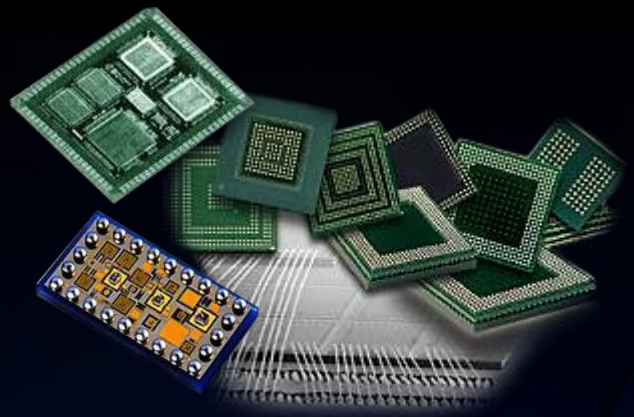


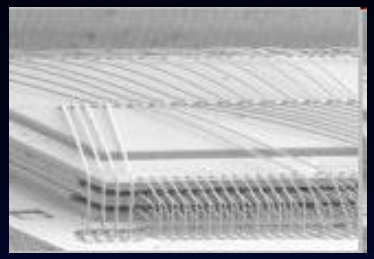
Source: Samsung 3D vertical NAND flash memory

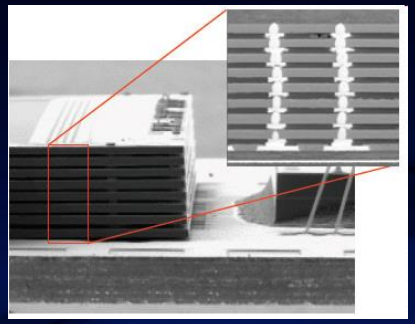
Or Stack Die in 2.5D or 3D

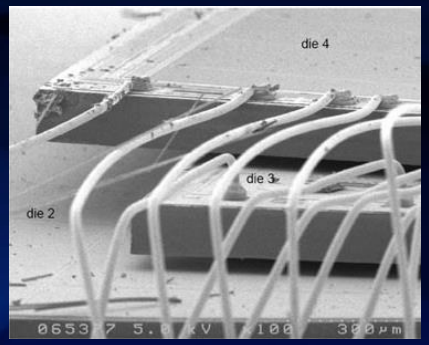


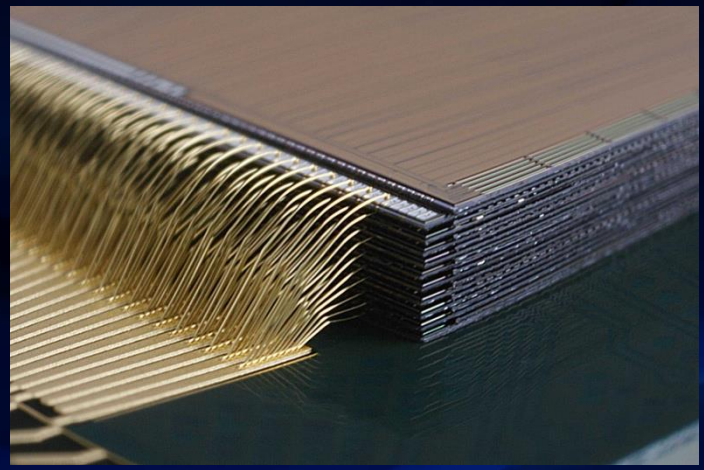










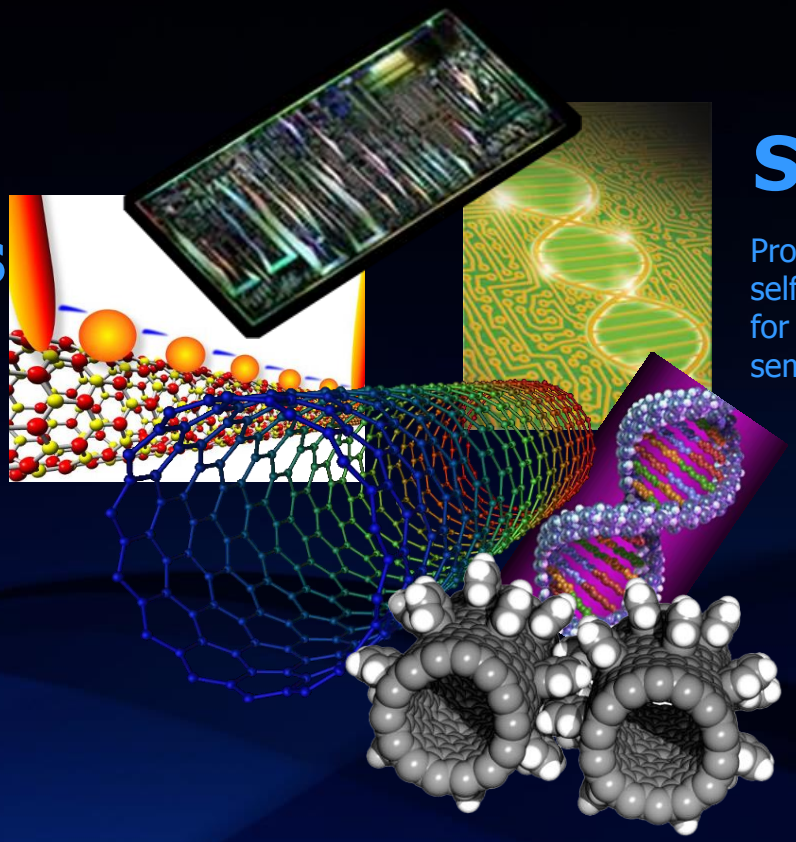


Source: IBM, Samsung, Sharp, Fujitsu, Intel, Renesas

New Technologies Drive Greater Functionality at Reduced Cost

Silicon Photonics

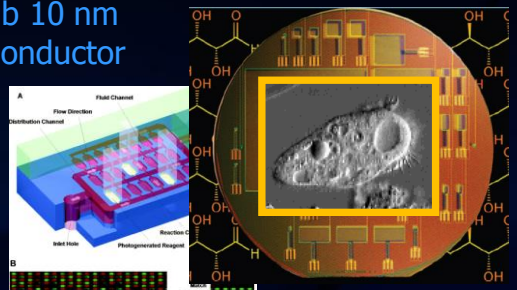
Spintronics



SemiSynBio

Programmable self assembly for sub 10 nm semiconductor

On-chip microbial energy generation

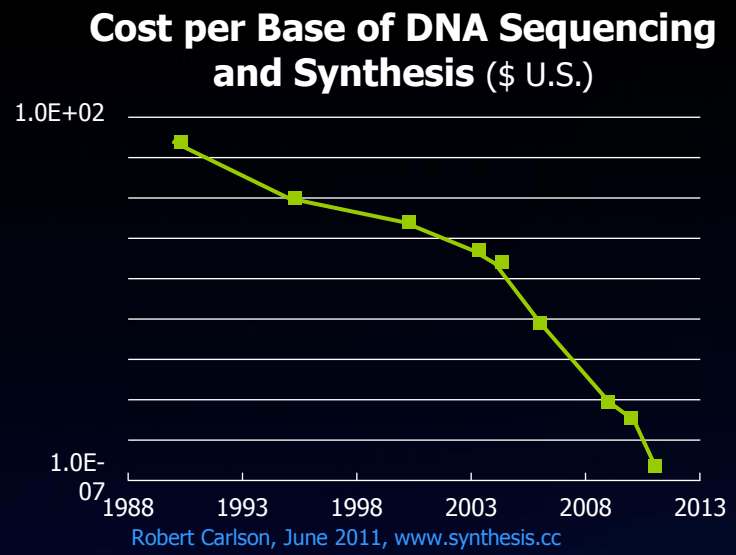


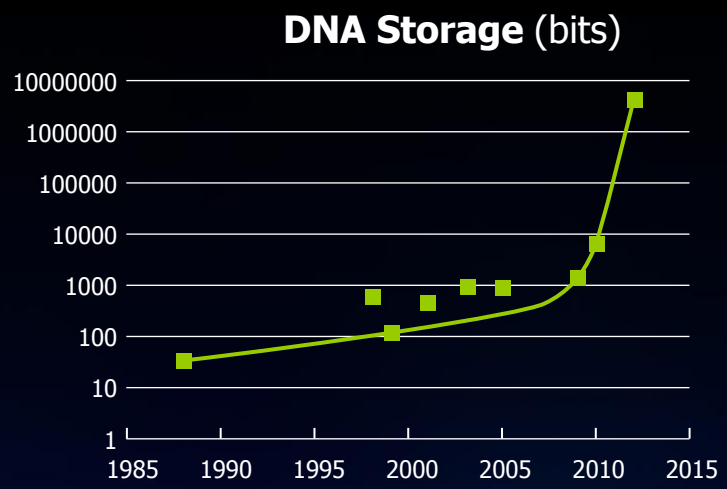
Chip-based DNA synthesis

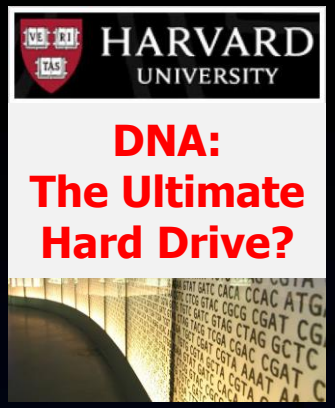
New Materials

Source: "Beyond Silicon: Transistors without Semiconductors", *Michigan Tech News 6/2013*

Beyond Silicon







	NAND Flash	DNA in Cell
ON Power (W/GB)	10^{-2}	**$<10^{-11}$ (9 orders of magnitude)**
Density	10^{16} bit/cm^3	**10^{19} bit/cm^3 (3 orders of magnitude)**

Source: SRC 11/12/2012

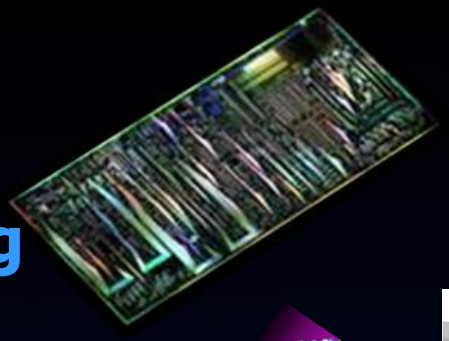
Summary: The Choices

Need to offset cost of double/triple patterning plus FinFET to continue 70% CAGR unit growth and learning curve cost

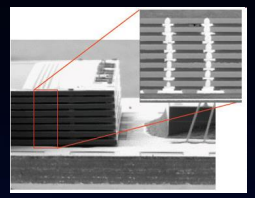
- Price pressure on the foundries?
- Margin pressure on the semiconductor companies?
- Force the supply chain to reduce cost faster than the long term learning curve?
- Slow down the rate of unit growth, and consequently innovation and new applications, of semiconductor electronics?

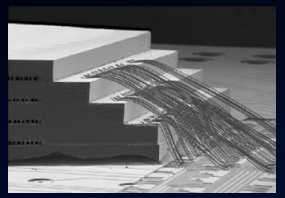
Or…

Innovate to Maintain Unit Volume Growth and Cost Reduction

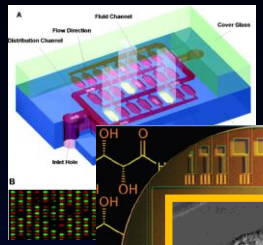


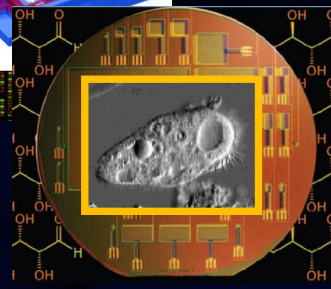
3D Stacking

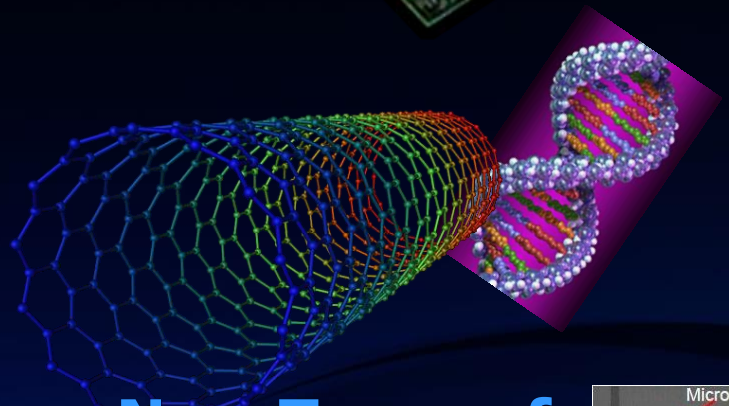




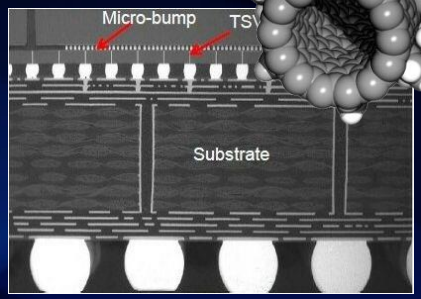
Increase Vertical IC Layers

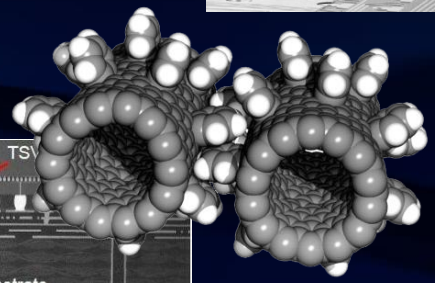






New Types of Transistor "Switches"





Carbon Nanotubes

www.mentor.com