FD-SOI

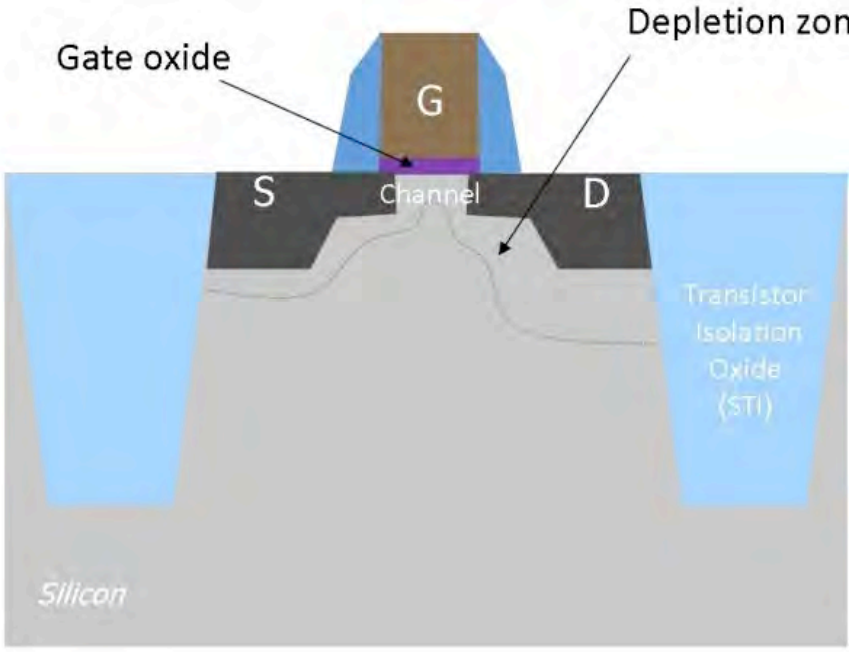
Paul McLellan, SemiWiki.com

EDPS 2014

FD-SOI

- Being driven by STMicroelectronics
- GlobalFoundries announced support for FD-SOI early last year but have de-emphasized it
- TSMC and Samsung are pure FinFET at 16nm

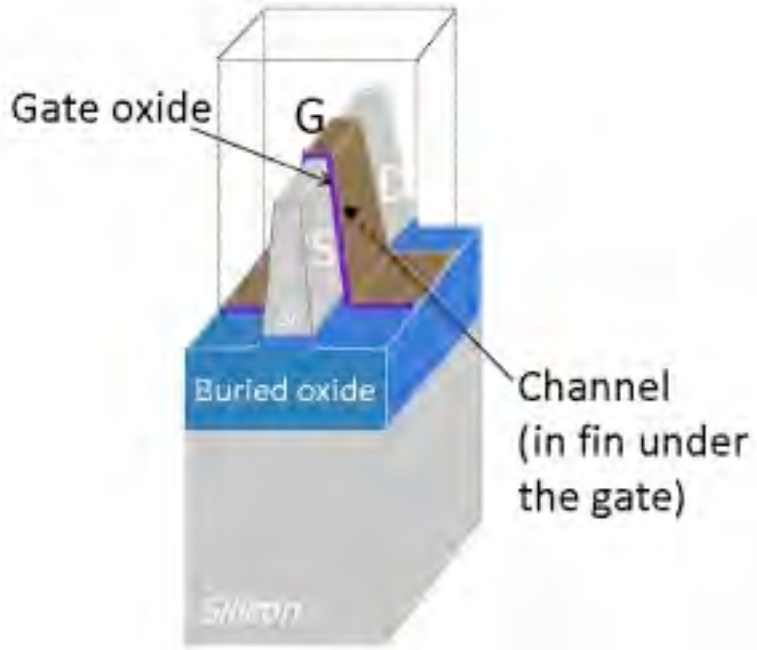
The Problem: 20nm Limit



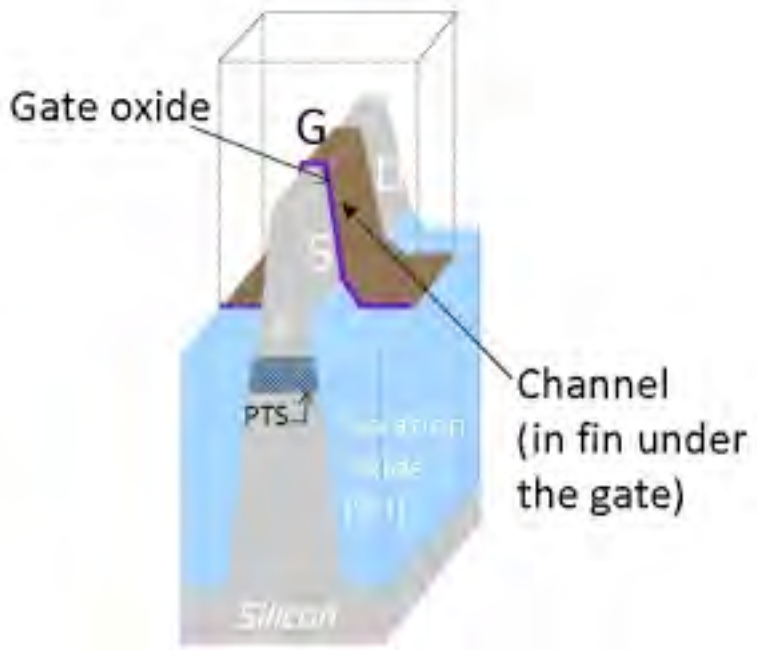
Planar bulk transistor

Gate does not control the channel well—very high leakage power. Channel must be made thinner

Solution 1: Go Vertical

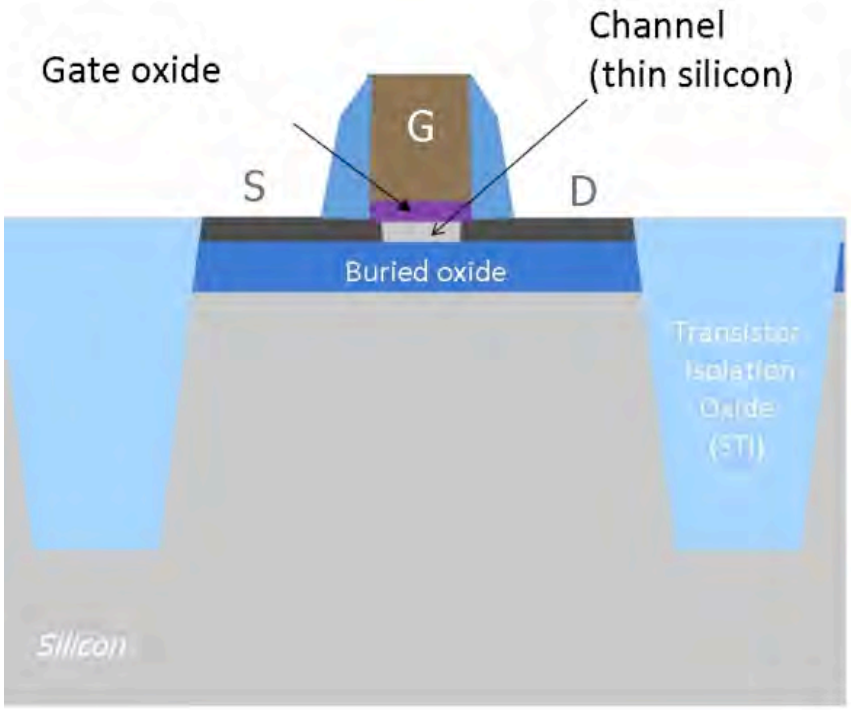


FinFET, silicon-on-insulator based



FinFET, bulk silicon based

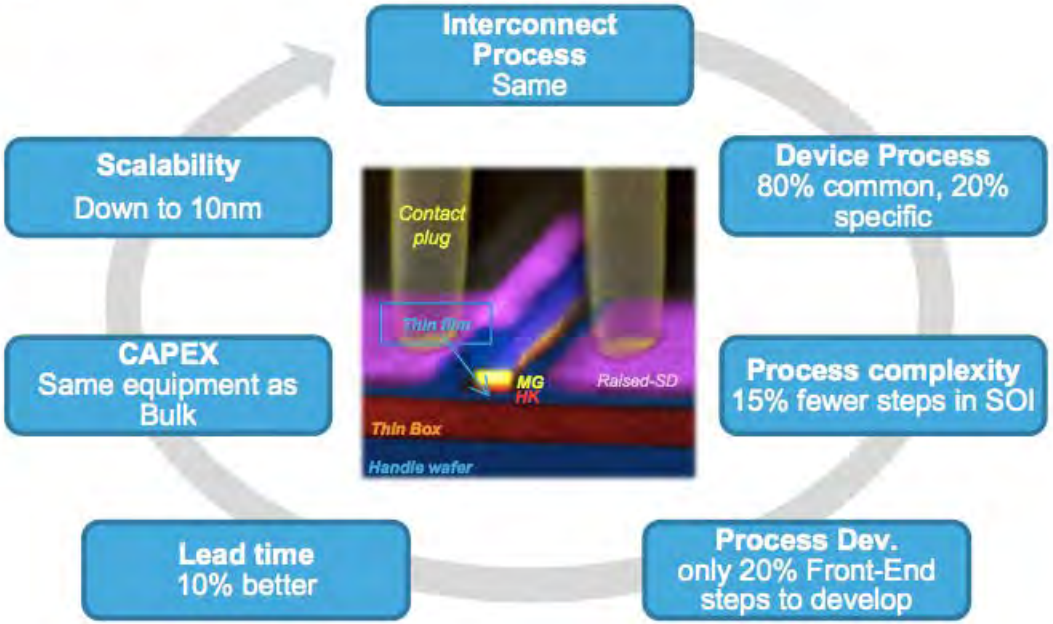
Solution 2: Back the Channel with Insulator



Planar FD-SOI transistor

FD-SOI is Simpler Than FinFET

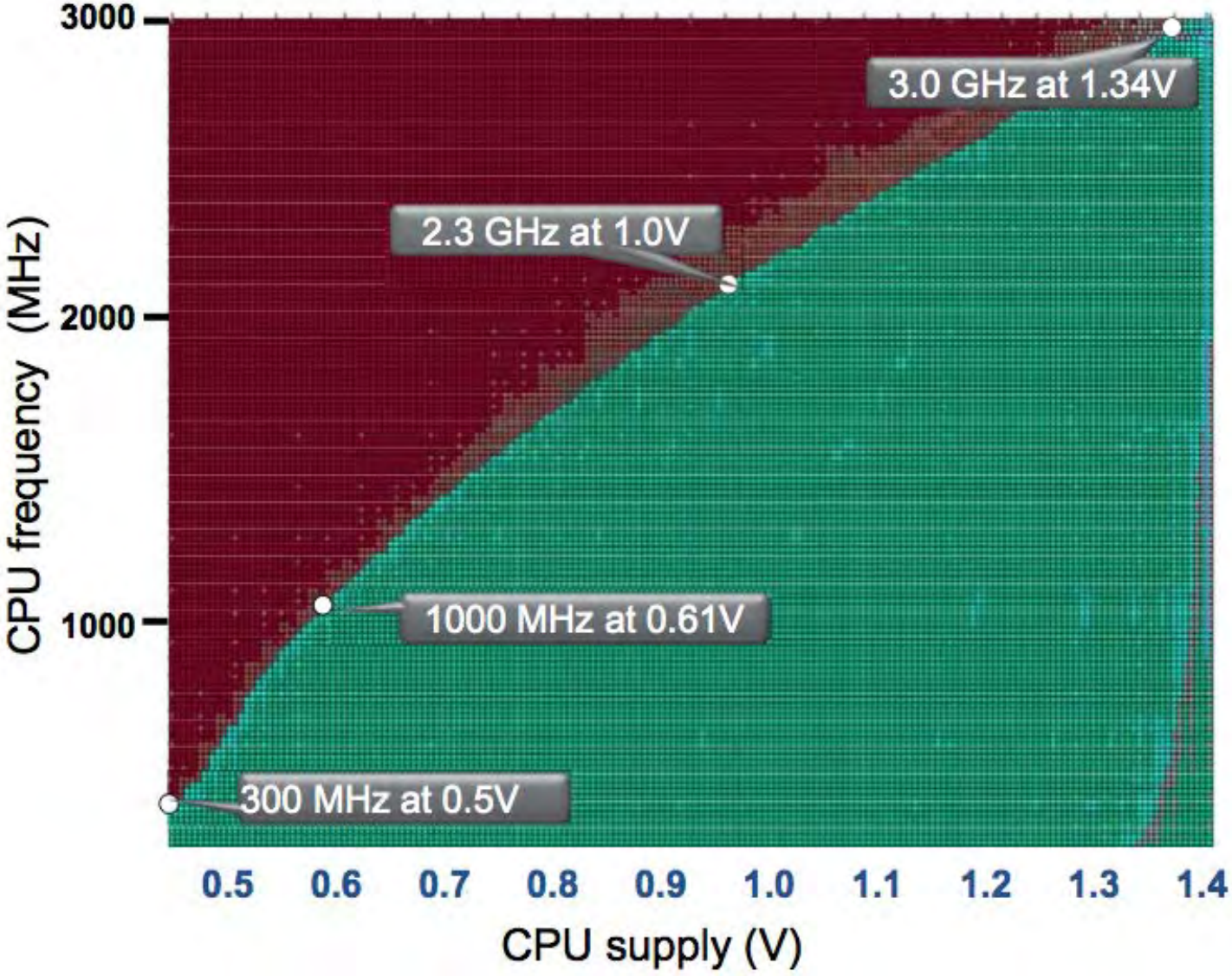
- Uses simpler process technology
  - 90% process-step reuse from 28nm bulk to 28nm FD-SOI
- Simple incremental porting from 28nm bulk low-power process
  - Same manufacturing tools
- Several process steps and masking levels are removed from 28nm bulk technology fully compensating for the extra cost of initial FD-SOI substrate wafer.



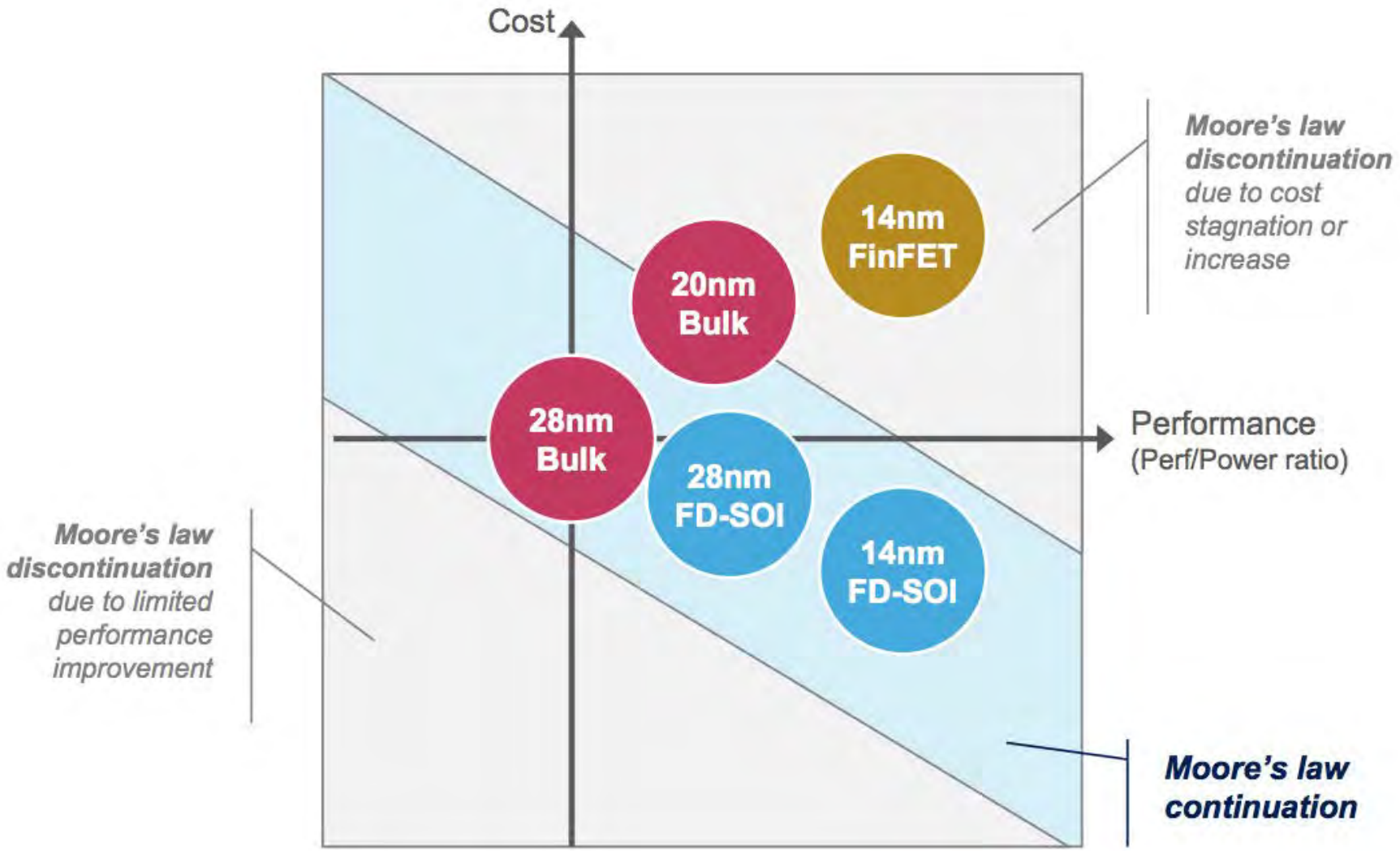
Other Features

- Cost of wafer blank is about $500
- 20nm film, thin oxide layer
  - Better back biasing for dynamic power and performance control
- FD-SOI can fully deplete the channel giving an excellent on-off ratio

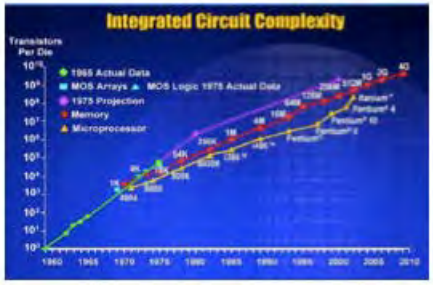
DVFS Range 0.5-1.3V



The Technology to Continue Moore's Law



The Driver of Semiconductors



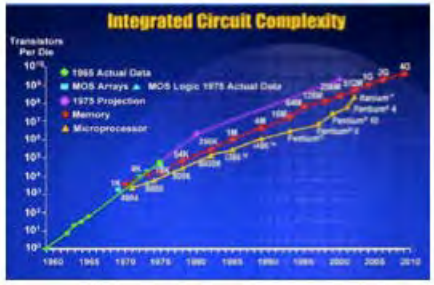
TRANSISTOR SIZE REDUCTION

BETTER COST/PERFORMANCE

MARKET GROWTH

INVESTMENTS

The Driver of Semiconductors



TRANSISTOR SIZE REDUCTION

BETTER COST/PERFORMANCE

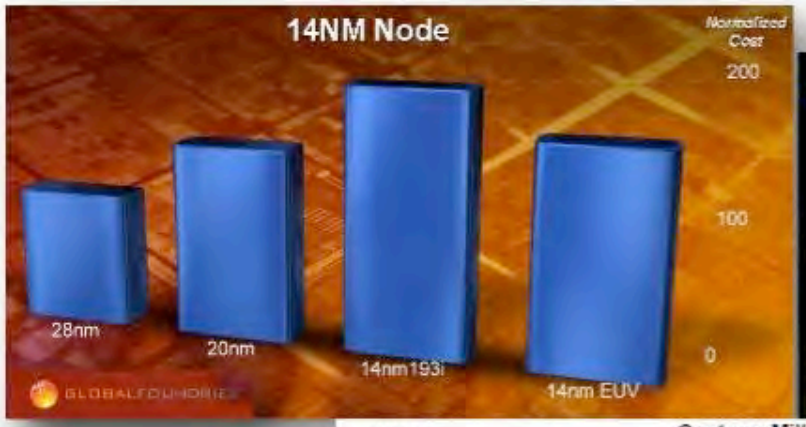
MARKET GROWTH

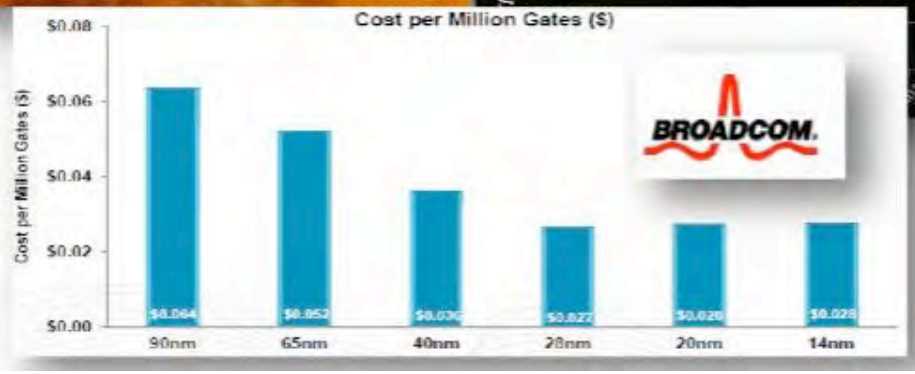
INVESTMENTS

EUV not happening

450mm not happening

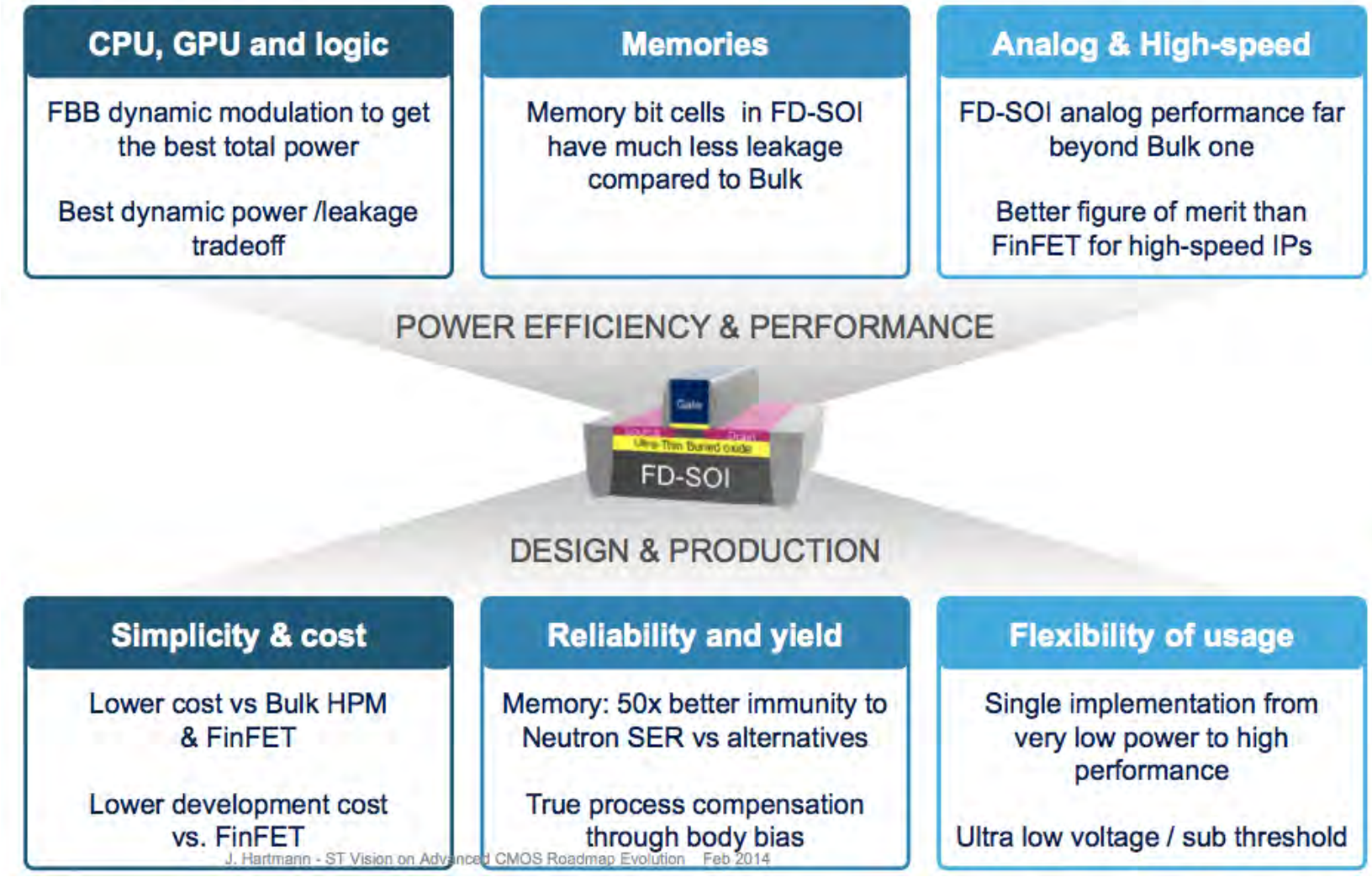
Virtuous Cycle Broken at 20nm





Sources: nVidea, ITPC, nov, 2011
Broadcom, IMEC, may 2012

FD-SOI Efficient for All Types of Design



ST Believes FD-SOI Superior to FinFET

Faster

Puts more powerful devices in the hands of the end user

Transistors at max frequencies are up to 30% faster than bulk CMOS, enabling faster processors

Cooler

End-user devices run cooler and last longer

Transistors are significantly more power efficient than bulk CMOS devices with lower leakage and much wider range of operation points down to lower voltages

Simpler

Much simpler manufacturing process

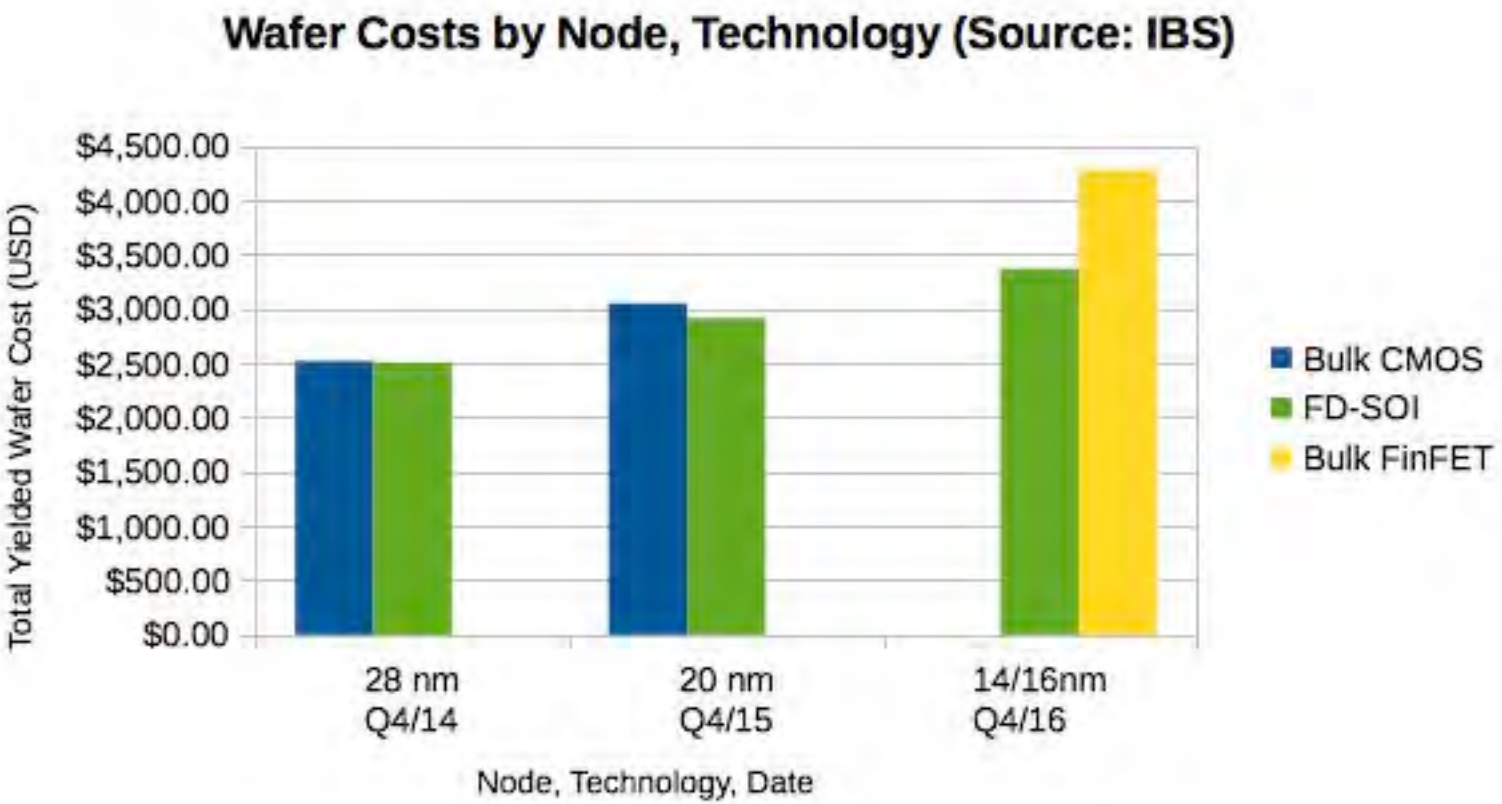
Extensive use of existing fab infrastructure
Design porting from bulk is simple and fast

Available today at 28nm - Roadmap in execution down to 10nm

Handel Jones (IBS) Believes it Too

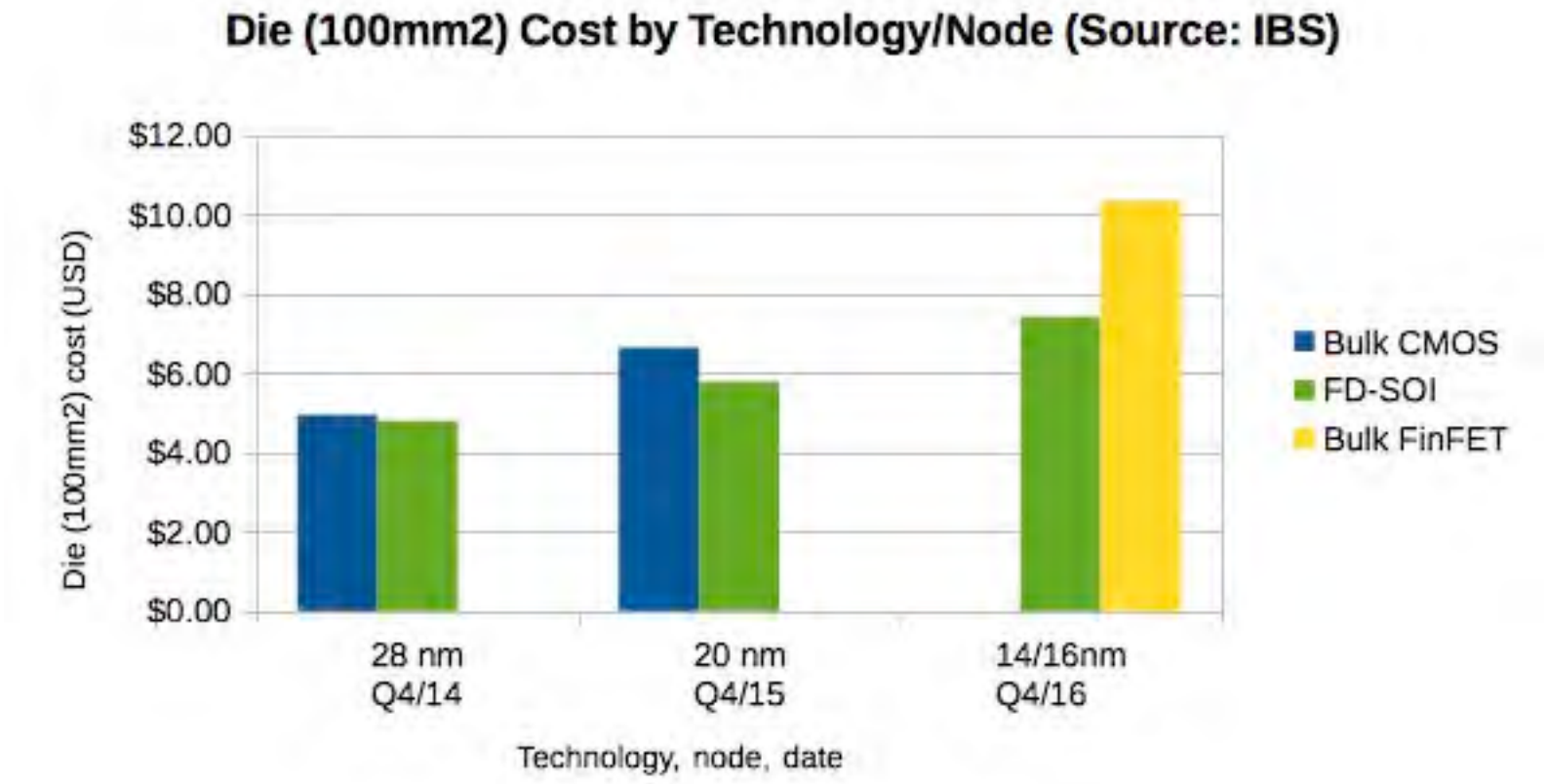
- ***Why Migration to 20nm Bulk CMOS and 16/14nm FinFETs Is Not the Best Approach for the Semiconductor Industry***
- at 28nm and 20nm, the lower power consumption and higher performance of FD-SOI compared to planar bulk CMOS gives major competitive advantages to FD-SOI in high volume portable applications.
- the lower cost of FD-SOI die compared to 16nm FinFET die provides an overwhelming advantage to utilizing FD-SOI for high volume applications at this technology node
- The use of body biasing provides significant performance and power consumption advantages for FD-SOI. Also, FinFET has very high gate capacitance, a problem in high fanout designs

Wafer Costs by Technology



The wafer cost for 14nm FD-SOI is 18.4% lower than 16nm FinFET

Die Costs by Process Node (100mm2)



At 14nm/16nm, the FD-SOI die cost for a 100mm^2 die is 28.2% lower than the bulk FinFET die cost and has higher yield.

But…An FD-SOI Ecosystem Needed

- ST cannot be the only company driving the whole industry
- The supply chain for FD-SOI starting wafers is in place (by Soitec, SunEdison, and SEH) and can be expanded rapidly to provide the required wafer capacity if a demand environment is established.
- The use of body biasing provides significant performance and power consumption advantages for FD-SOI

Design Considerations

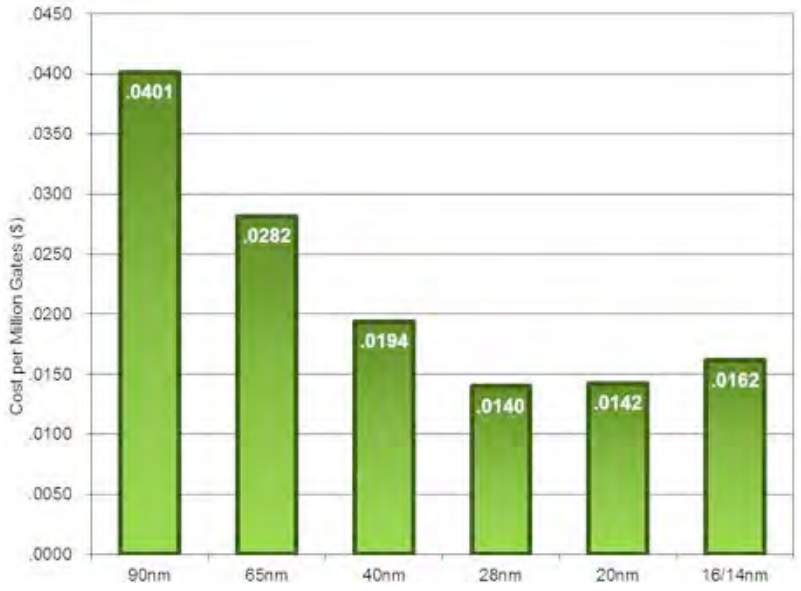
- Design flows for FD-SOI are effectively identical to those for bulk CMOS
- Libraries and basic IP developed for bulk CMOS can be easily modified for FD-SOI.
  - The cost of modification between bulk CMOS and FD-SOI is approximately 10% of that required to migrate to a new technology node for bulk CMOS at 20nm.

Capabilities by Market Segment

Technology segment	Challenges	FD-SOI Benefits
Infrastructures Networking Servers	Energy-efficient multicores	High performance at low voltage & low performance degradation when lowering supply {~800MHz @ 0.6V} on ARM big cores.
	Energy used proportional to workload	FBB to adjust the "Dynamic power / leakage / maximum frequency" vs load.
	Large Embedded memories	FD-SOI offers excellent SER performance thus reducing the total RAM area or increasing the system reliability
Internet of Things Medical/Wearable	Ultra-low-power SOC	Ultra-low-voltage operations with high performance. e.g. a 247 MHz DSP @ 0.39V using ULV cells
Consumer	Energy-Efficient SOC in different thermal environment & maximum temperature conditions	FBB dynamic modulation can be used to get the best total power (dynamic power / leakage tradeoff) reusing the same SOC for different markets

Call to Arms

- Foundry vendors will not invest unless they see customer demand
- Customers need to provide leadership
  - The current FinFET roadmap is too high cost for high-volume designs
  - Costs per transistor are increasing
  - Moore's Law is broken economically



ST's Roadmap

- ST is committed on FD-SOI technology
  - 28nm FD-SOI open for risk production
  - Full 28nm Design Platform offer available and silicon qualified
  - Compelling silicon results obtained (mobile multi core A9 running at 3GHz)
  - All ST next-gen consumer products in FD-SOI
- FD-SOI technology for high energy efficiency: faster & cooler
  - Dynamic Process Scaling (thanks to extended body bias), the new design leverage
    - Allowing dynamic switching between high-speed and static-power optimization
  - Low gate capacitance (lower than bulk) and high-speed devices: low dynamic power
  - Allowing full reuse of low-power bulk planar design techniques
- FD-SOI technology: simpler & cheaper
  - High-K/Metal-Gate gate-first technology, no complex "G" stressors
  - Less variability, less layout effects
  - Simplified process flow, same equipment as for bulk planar
- FD-SOI technology: scalable
  - Roadmap already defined down to 10nm
  - 14nm node in development

Summary

- The world is going FinFET in a big way

BUT

- costs are out of line
  - EUV is not going to bring them down soon
  - 450mm is not going to bring them down soon
- Users should consider seriously whether FD-SOI is actually a better solution for their needs