

2.5D/3D-IC Update

Electronic Design Process Symposium
Monterey, CA, April 17, 2014

Herb@eda2asic.com

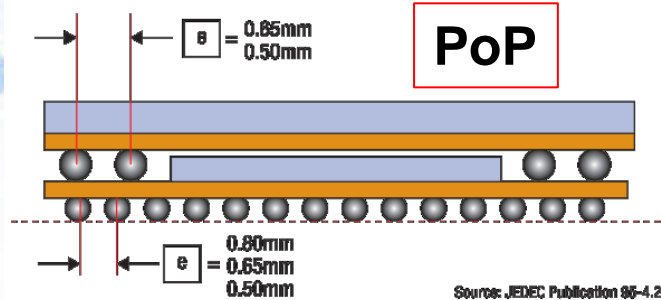
- **Introduction**
- **Why do we need 2.5D/3D Technology ?**
 - Business reasons
 - Technical considerations
- **2.5D/3D key benefits and challenges**
 - Application-specific benefits
 - Challenges
- **2.5D/3D EDA vendor updates**
 - Si2 Open 3D TAB
 - Basic 2.5D/3D Design Flow
 - Updates from: Ansys, Atrenta, Cadence, Docea, eSystem, Mentor, MicroMagic, Synopsys
- **Summary, Q & A**

~1980s

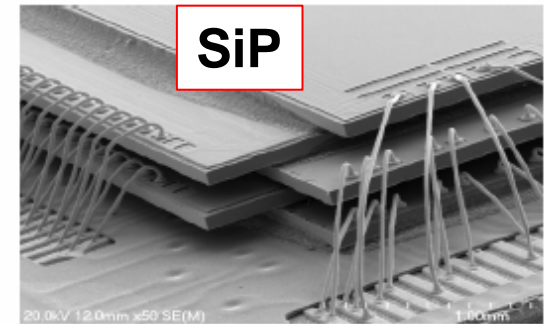


2,500 μm contact spacing

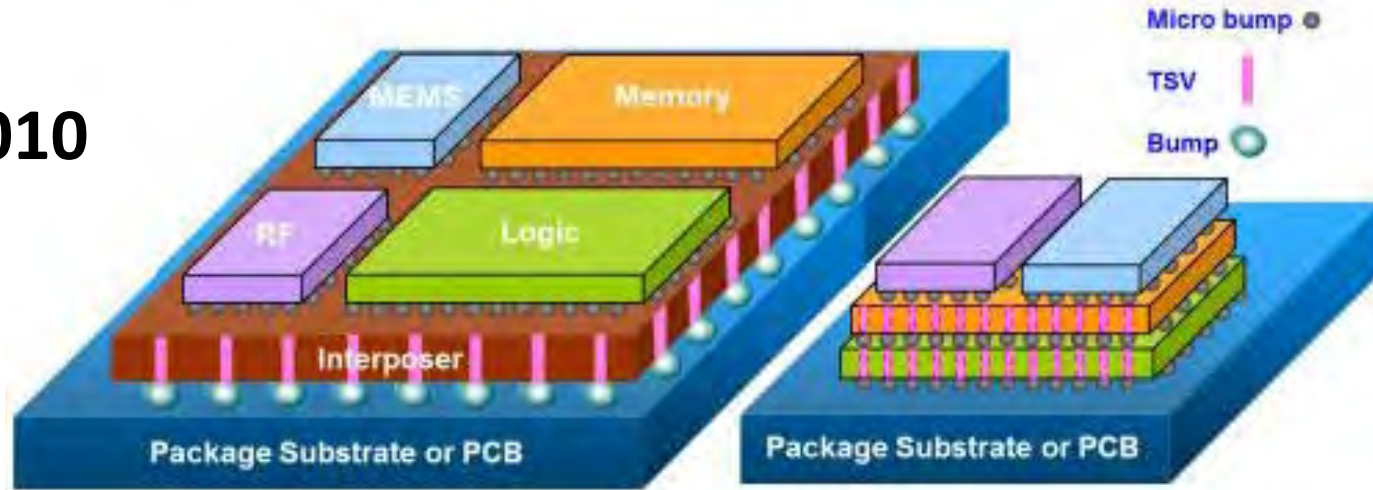
~1990s



~2000s



~2010



*: OSAT =
Outsourced
Semiconductor
Assembly and
Test company

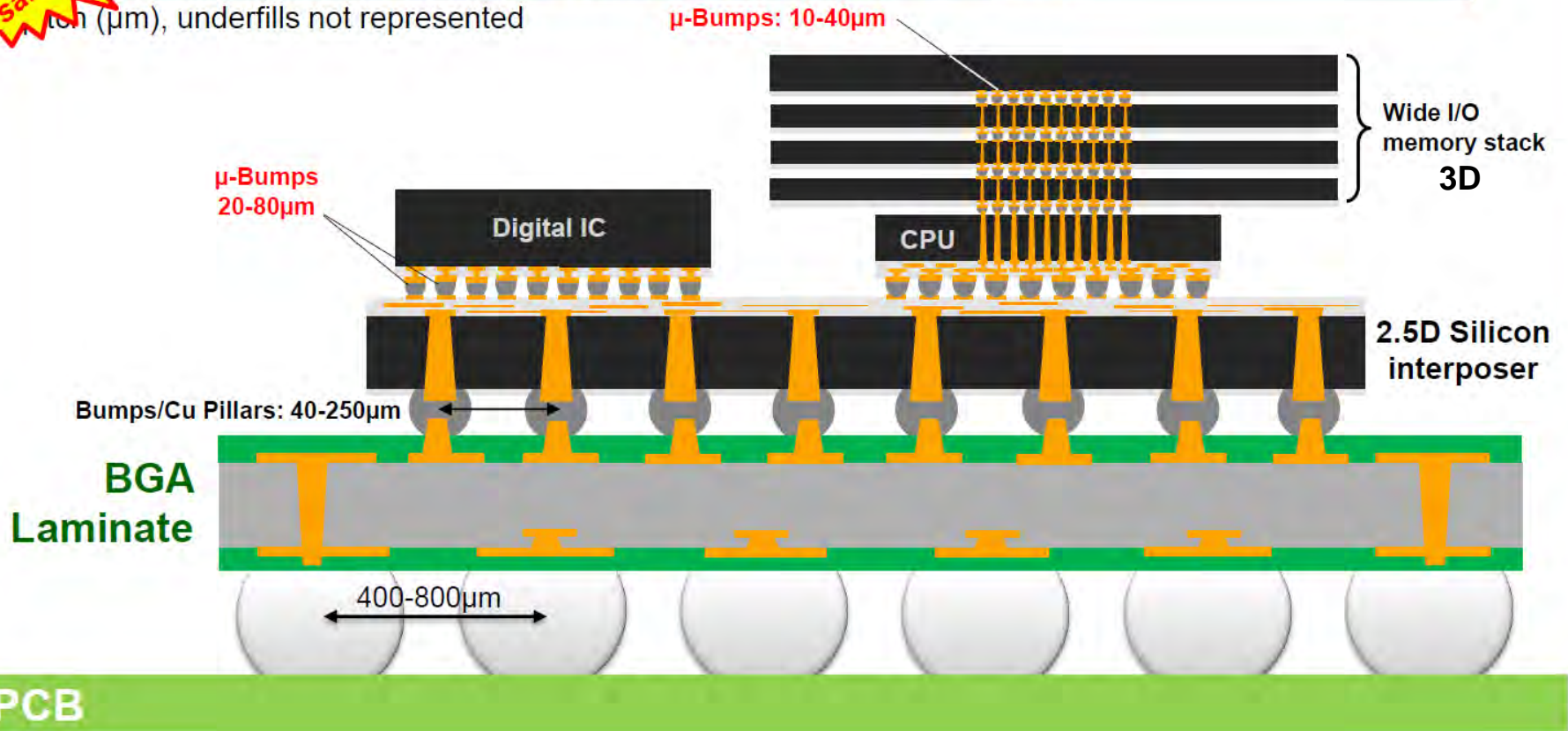
Side-by-side dice on an Interposer,
also called “2.5D-IC”

Vertically stacked dice,
called “3D-IC”

~ 25 μm contact spacing

Bumping Hierarchy* in Flip Chip
& related 3D Packaging Solutions as of 2013

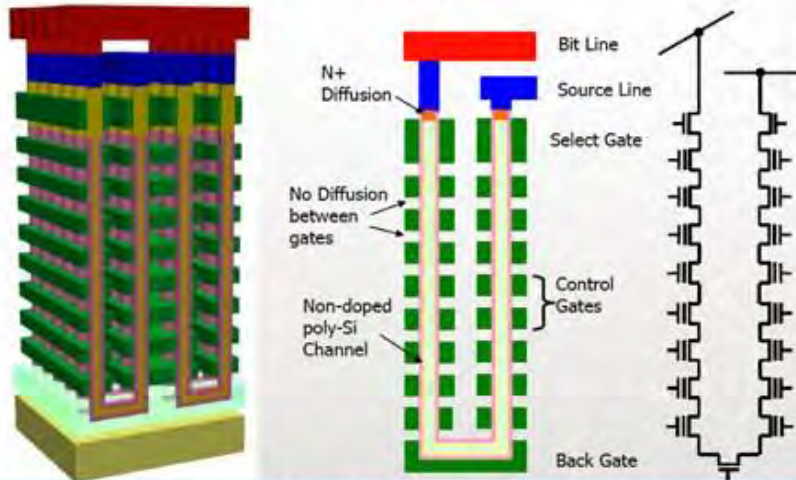
Report sample



* : SOURCE: YOLE Developpement, France

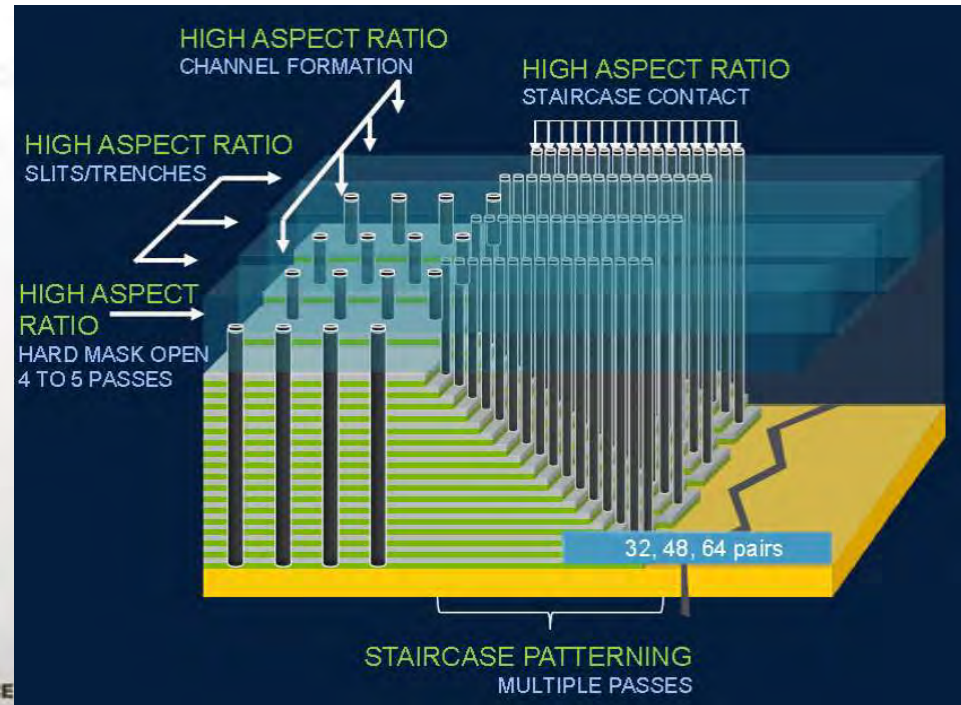
eda2asic Monolithic Memory Integration in Fab

P-BiCS Flash



P-BiCS has "U" shaped NAND string with back gate to reduce parasitic resistance of bottom portion. There is no diffusion between CGs. Select gate has asymmetric source and drain structure to reduce off current.

MEMORY CONFERENCE

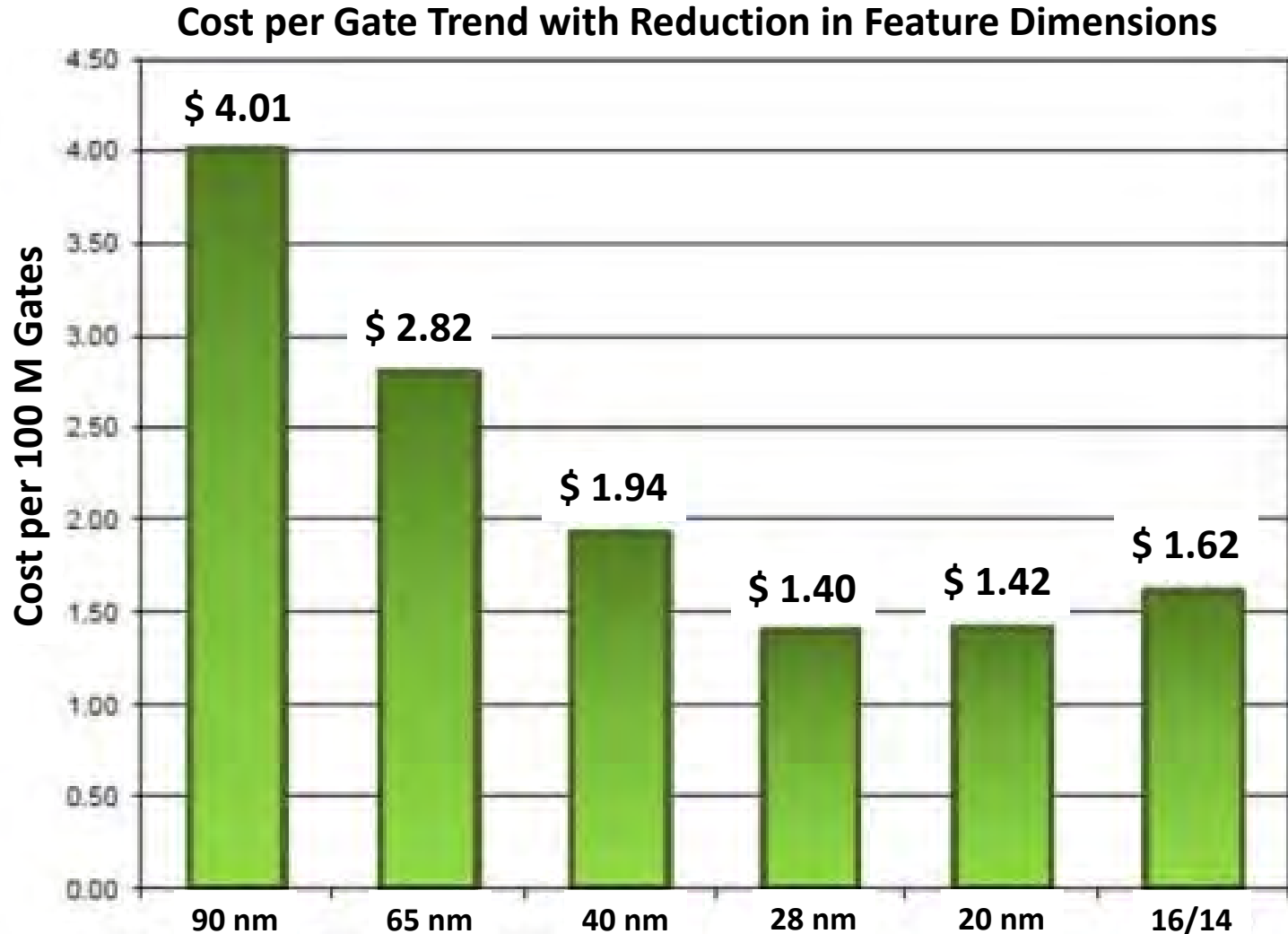


http://www.theregister.co.uk/2013/04/22/sandisk_q1_2013/

<http://semimd.com/blog/2014/01/29/3d-nand-to-10-nm-and-beyond/>

Monolithic vertical memories are in development as building block for 2.5D/3D-ICs
Monolithically integrated logic requires additional EDA capabilities to succeed
Monolithic integration of heterogeneous functions --- TBD ?

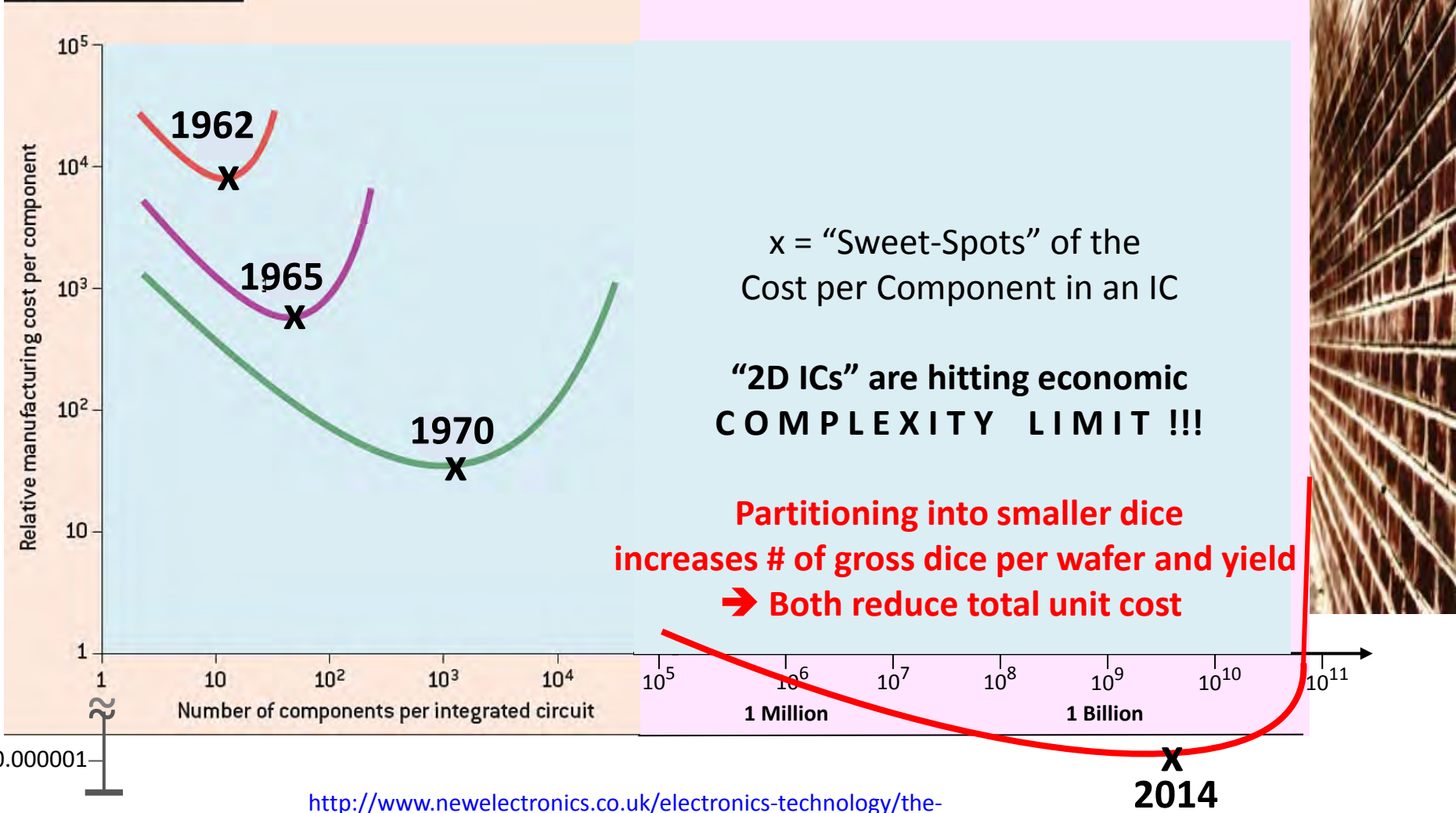
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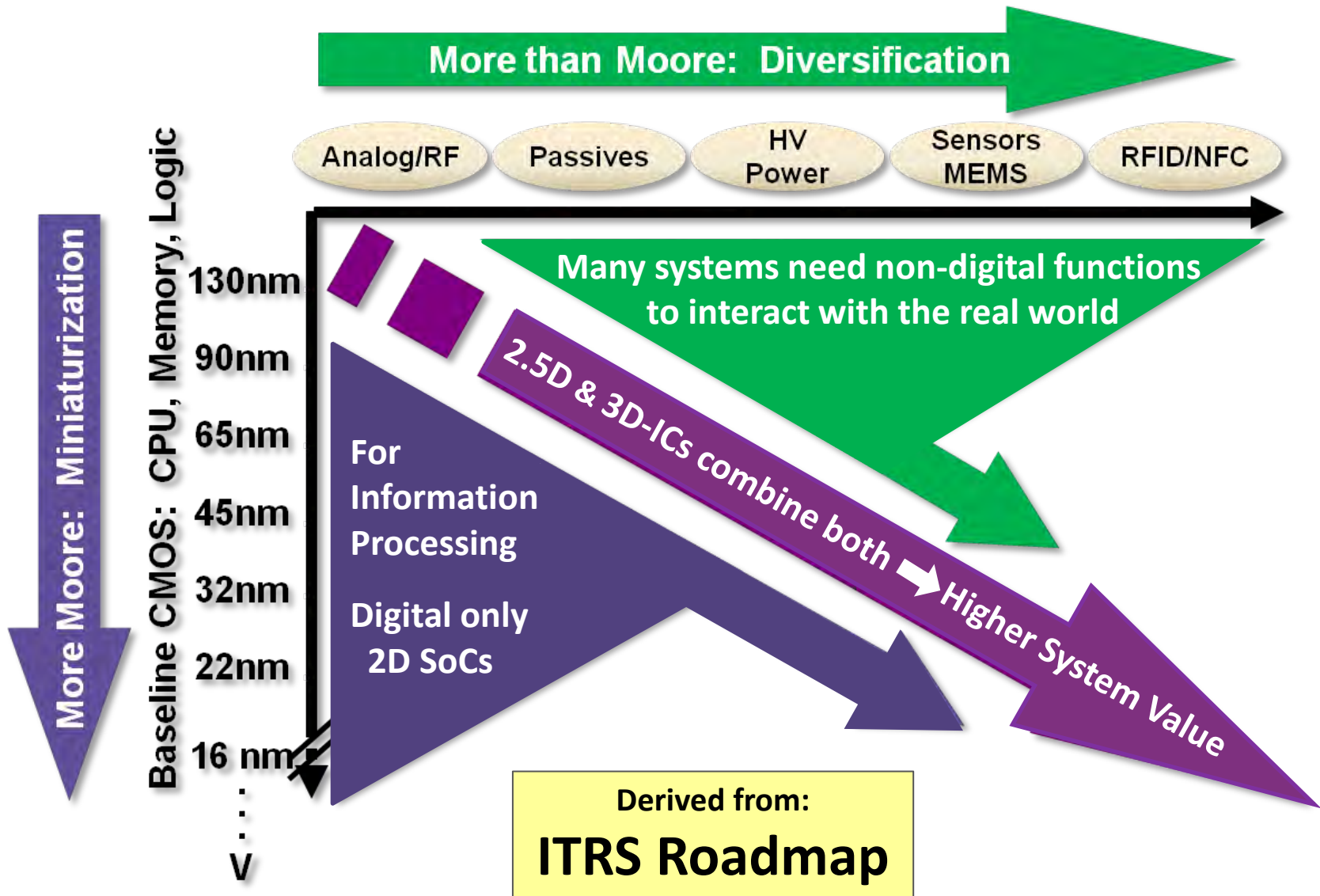
Source:
International
Business
Strategies, Inc.

http://www.eetimes.com/author.asp?section_id=36&doc_id=1321674&image_number=1

Fig 1: Moore's curves



<http://www.newelectronics.co.uk/electronics-technology/the-economics-of-chip-manufacture-on-advanced-technologies/35562/>



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Benefit Market	Low Power Dissipation	High Bandwidth CPU <-> DRAM	Low Latency IC <-> IC	Heterogeneous Integration	Form- factor
Cellphones and esp. Smartphones	★ ★ ★	★ ★	★	★ ★	★ ★ ★
Compute Servers, Network Routers	★ ★	★ ★ ★	★ ★ ★	★ ★	★
Tablets and other Mobile Devices	★ ★	★ ★	★	★ ★	★
Standard PCs and Workstations	★ ★	★ ★	★	★	★
Automotive Applications	★	★ ★	★ ★	★ ★	★

Additional decision factors: Unit Cost, System Cost Savings, NRE, Time-to-profit, Risk,...

2014-04-11 ★ ★ ★ Extremely Valuable

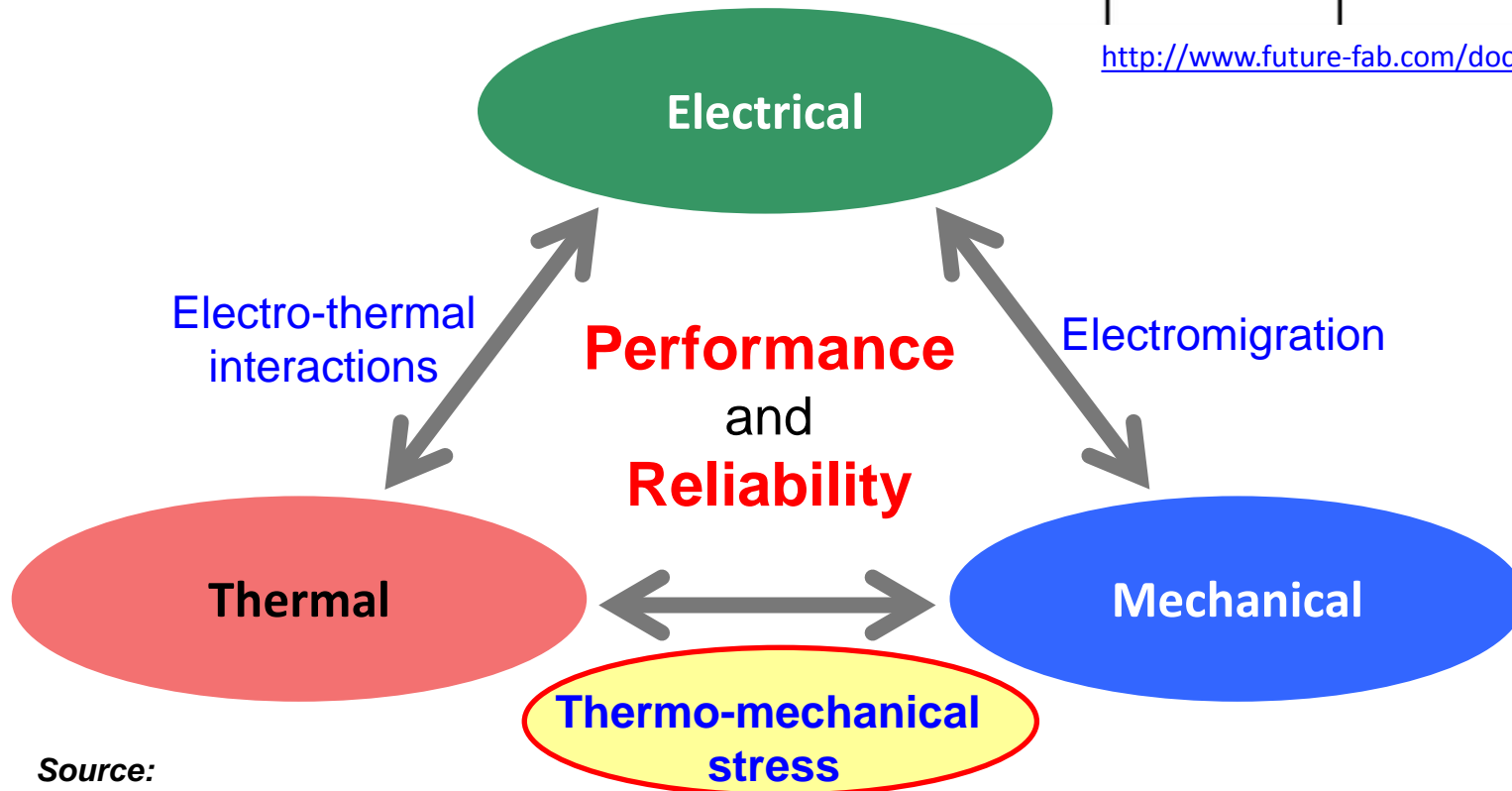
★ ★ Very Valuable

★ Valuable

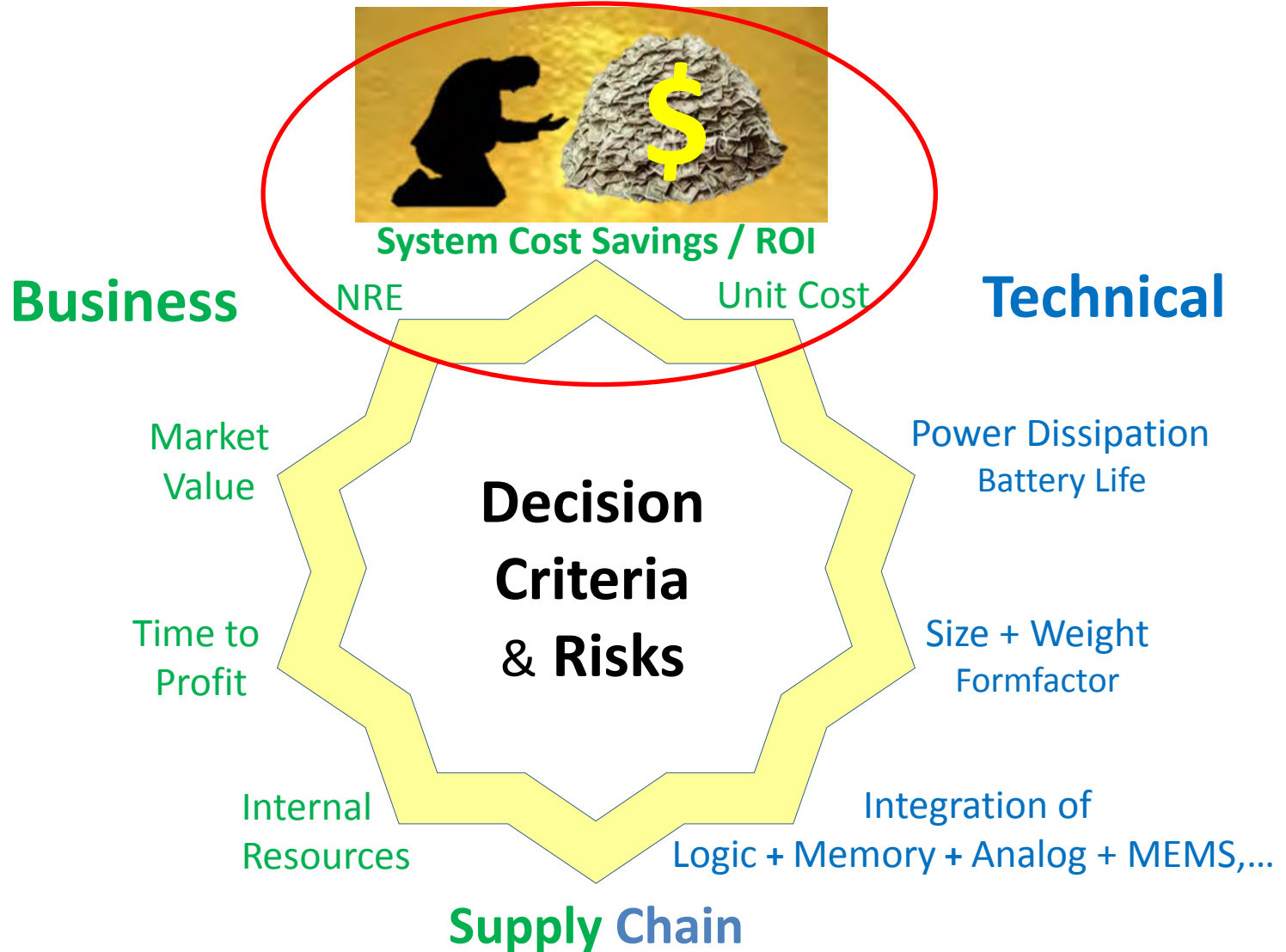
eda2asic Multi-Physics Design Challenges

Materials	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio
Silicon	2.8	131	0.28
Copper	17.0	117	0.35

http://www.future-fab.com/documents.asp?d_ID=4988



Source:
A. Wilde, P. Schneider, P. Ramm, DTC 2010



Electronic System Vendors

> \$ 3,000 B

Design Companies

Semiconductor Vendors

\$ 300 B

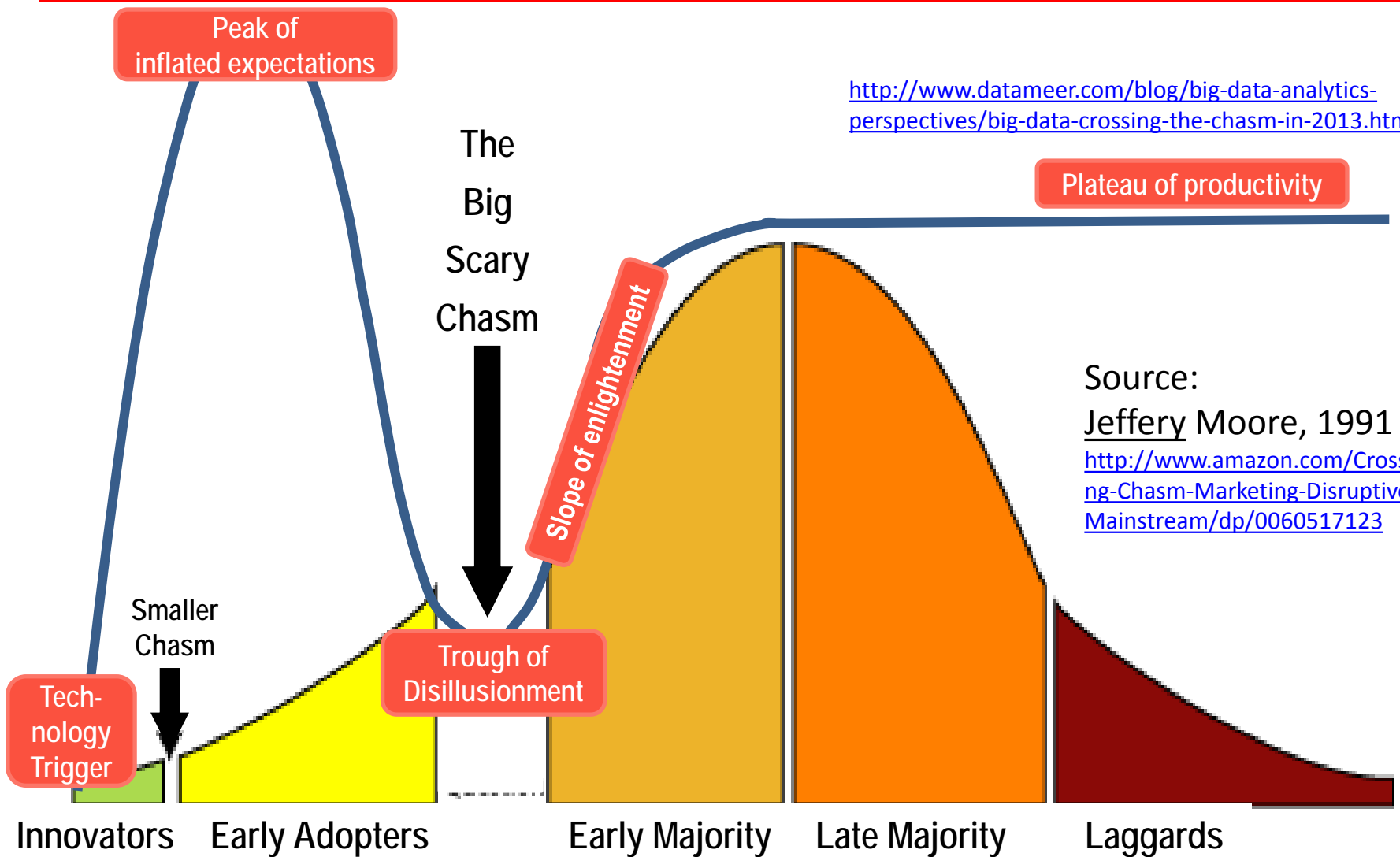
EDA & IP \$ 7 B

OSATs \$ 10 B

Wafer Fabs \$ 40 B

Equipment & Materials \$ 40 B

Manufacturing Companies



<http://www.datameer.com/blog/big-data-analytics-perspectives/big-data-crossing-the-chasm-in-2013.html>

Plateau of productivity

Source:
Jeffery Moore, 1991
<http://www.amazon.com/Crossing-Chasm-Marketing-Disruptive-Mainstream/dp/0060517123>

Where is 2.5D and 3D ?

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Open3D TAB

The Open3D Technical Advisory Board (TAB) was chartered to develop standards to support the design of 2.5D interposer-based packages and full 3-D stacked-die assemblies. Open3D TAB is scoped to define open standard interfaces and formats to enable interoperable 2.5D and 3D design flows, providing common interfaces, but not infringing upon any proprietary algorithms, products, or methodologies based on Si2's member-approved and well-accepted IP Policy. The Open3D Technical Advisory Board (TAB) participation draws from a wide range of the supply chain, including fabless leaders, packaging / OSAT, foundries, and system / OEMs. Open3D will also be engaging a number of experts across the research and academic community for their domain knowledge.



Major Accomplishments - 2013

- **Si2 3D-IC Design Exchange Format Standard for Power Distribution Network (PDN)**

PDN describes a unified interface protocol for both Power/Ground and signal ports for die-2-die, die-2-package and package-2-PCB interfaces. This also allows the creation of compact SPICE-level descriptions to aid in the design, analysis and optimization of the resulting networks that define these interfaces to ensure they meet the requirements for power and signal integrity.

- **Si2 3D Thermal Constraints Standard**

The purpose of the Thermal Design Exchange Format is to facilitate thermal analysis to predict the time-varying average temperature and temperature variation of various locations within the stack, depending on a set of heat-loads.

https://www.si2.org/open3d_index.php

Plans for 2014

- ***Pathfinding***

An architectural planning standard for Through Silicon Via (TSV) models for interacting electrical, thermal and mechanical stress. The 3D TAB plans to release the pathfinding standard in the first half of 2014.

- ***Signal integrity and physical verification***

In 2.5D and 3D ICs, signal integrity becomes very important, particularly when one has to account for the effects of a dense array of through silicon vias (TSV). Physical verification, likewise, is also challenged by the increased densities of “More than Moore” and by the challenges of TSV’s. It is expected that this last effort will be a joint effort between the Open3D TAB and the DFM Coalition. If initiated, the goal of this effort will be to advance the existing OpenDFM standard to accommodate the needs of 2.5D and 3D technologies.

Open3D TAB Members

Advanced Micro Devices

Altera

ANSYS

Atrenta

Cadence Design Systems

Fraunhofer Institute

GLOBALFOUNDRIES

Helic

IBM

Intel

Invarian

Mentor Graphics

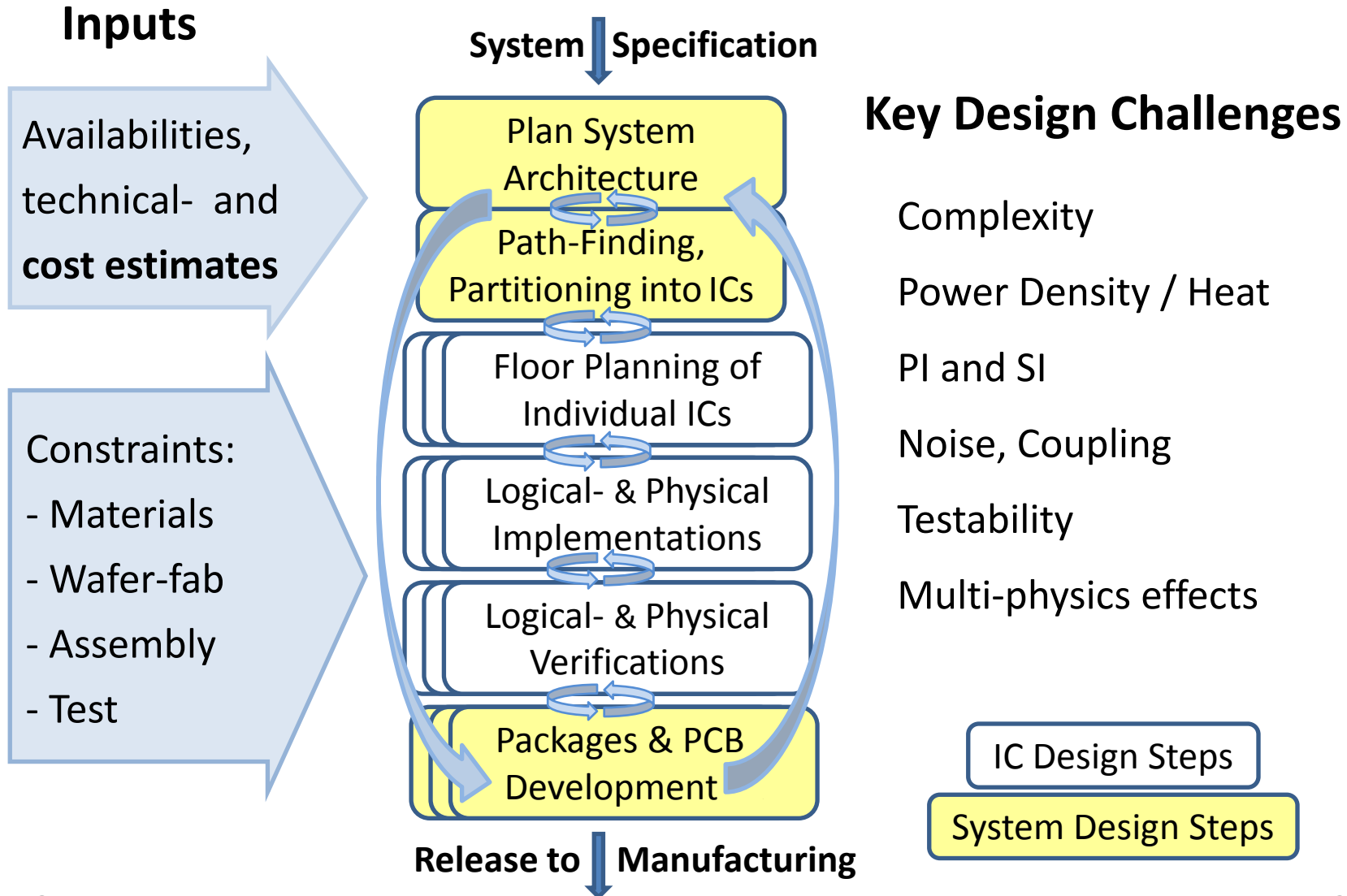
Qualcomm

R3 Logic

SEMATECH

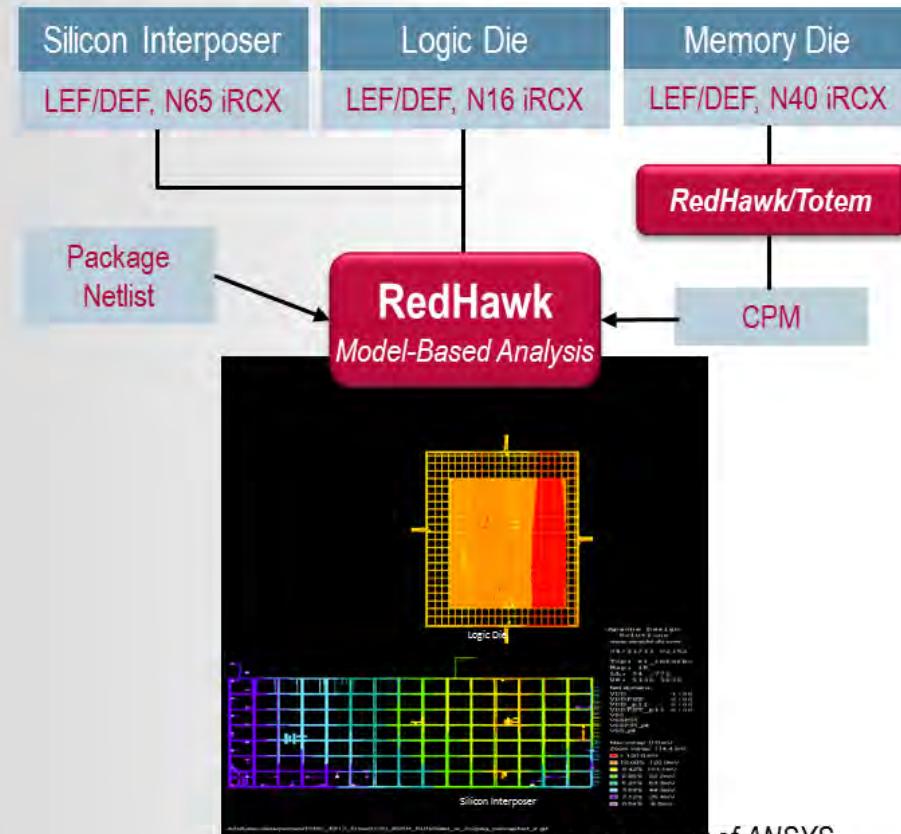
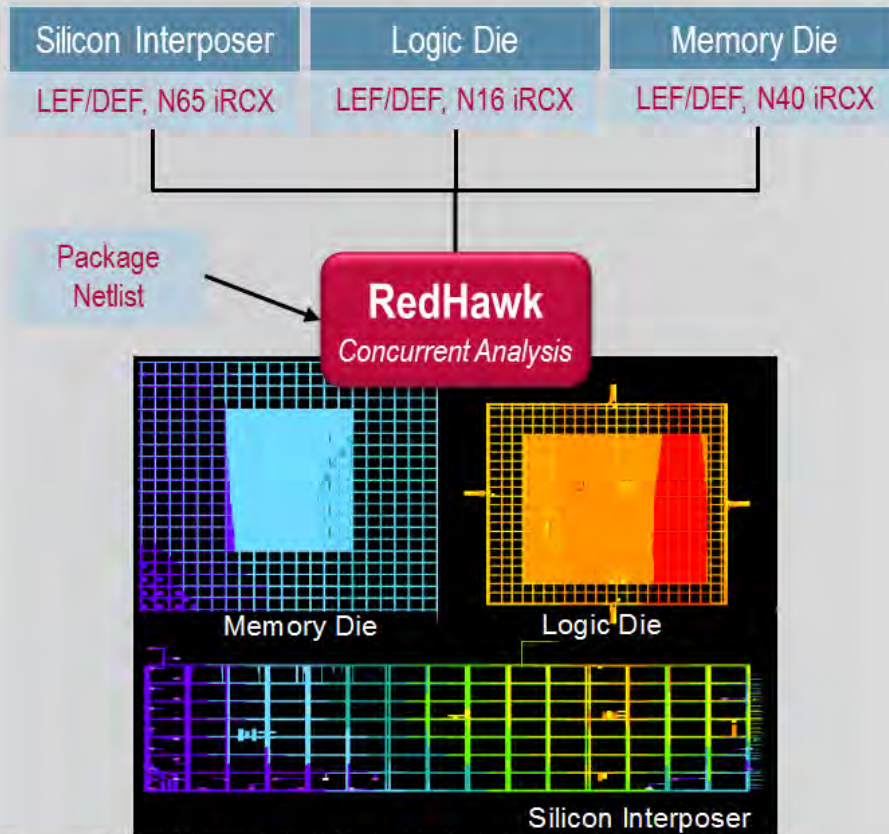
STMicroelectronics

Texas Instruments

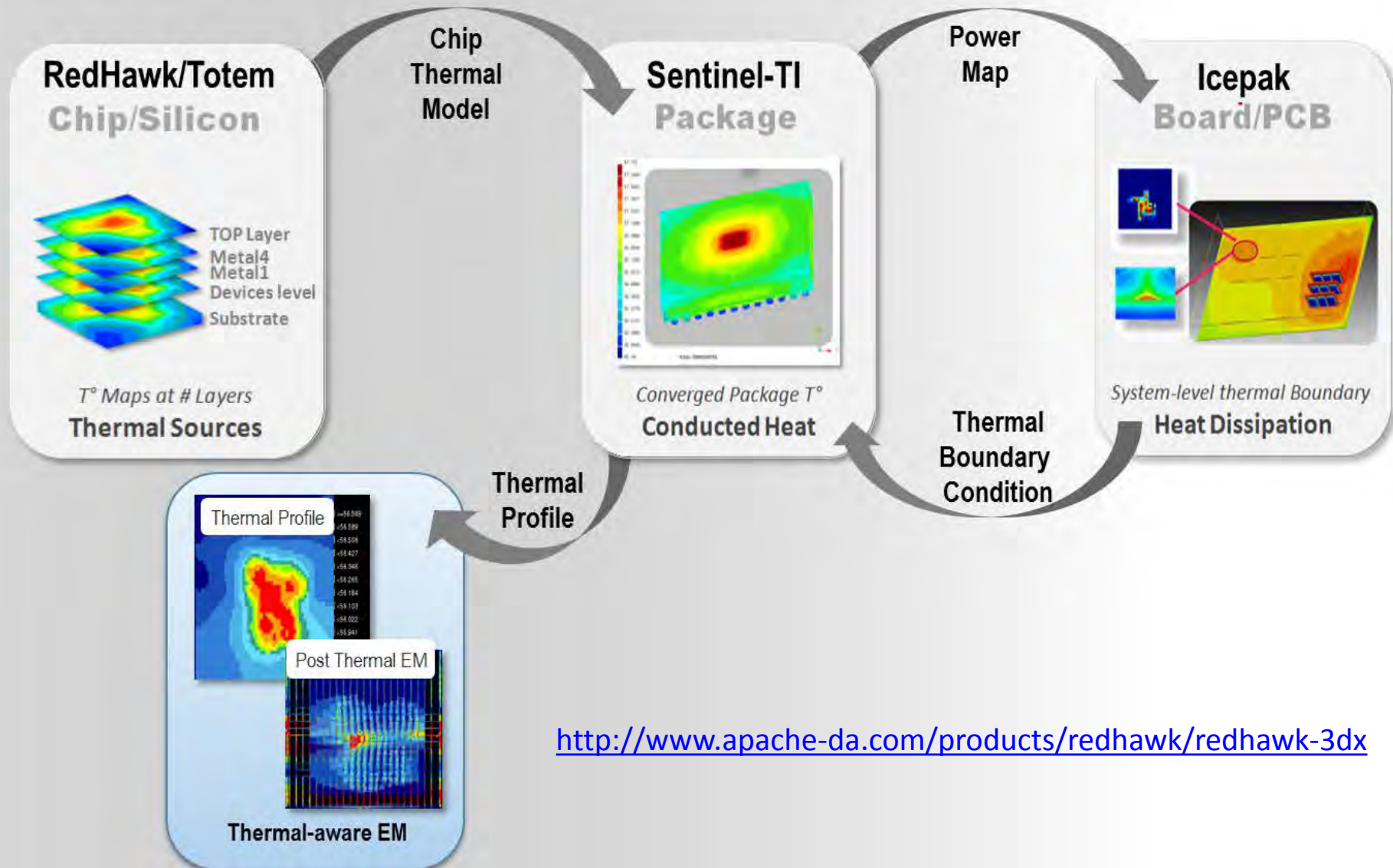


RedHawk-3DX: Concurrent and CPM-based 2.5D / 3D IR and Dynamic Voltage Drop Analysis

- Supports multi-die design with corresponding process data, including heterogeneous technologies
- Analyze impact of shared P/G nets and decap in interposer on memory and logic die
- Utilizes Chip Power Model (CPM™) - a die model with RLC network and current profile, generated by RedHawk™ or Totem™
- Enables simple hand-off and fast turn-around-time

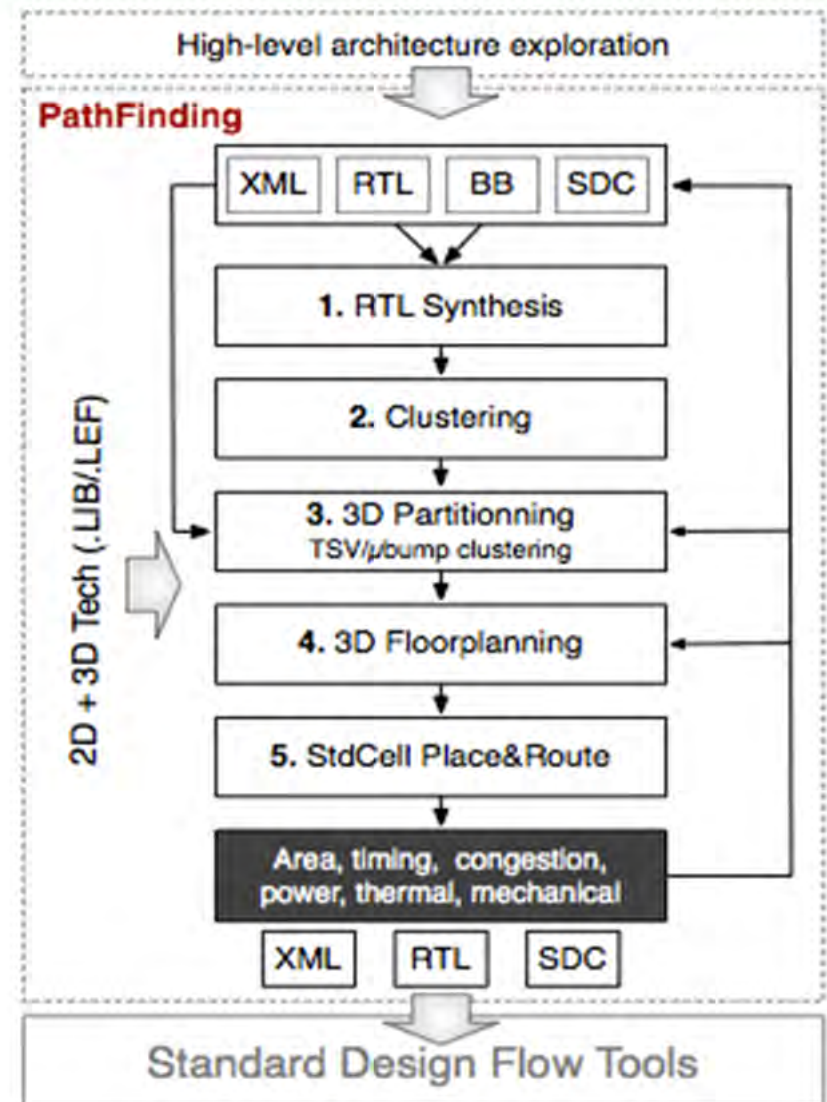


2.5D / 3D-IC Thermal Integrity Methodology



<http://www.apache-da.com/products/redhawk/redhawk-3dx>

- Early exploration flow
- Inputs: incomplete design spec, initial 3D configuration, system constraints and technology
- Performs standard (synthesis, P&R) plus 3D-IC specific tasks (partitioning, TSV/ μ bump planning, 3D floorplanning, P&R)
- Design characterization
- Outputs: stack configuration, design constraints, floorplan



- **System, technology, and implementation exploration**
 - Face-up vs. face-down orientation of the dies
 - Use of passive/active interposers
 - Use of RDL layers
 - Explore different number of layers to achieve design closure (timing and congestion)
 - Multiple technology nodes
 - Different size and pitch for TSVs

- **Floor-planning system in the 3D stack**
 - Constraints between blocks
 - Different TSV placement strategies

- **Customizable cost models to evaluate the quality of results (QoR)**
 - Power estimates, area reports, wiring congestion, timing, thermal and stress reports

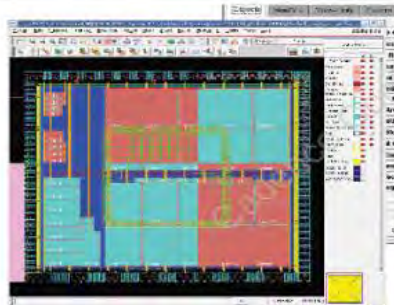
<http://www.atrenta.com/>

What's needed in 3DIC Design Methodology

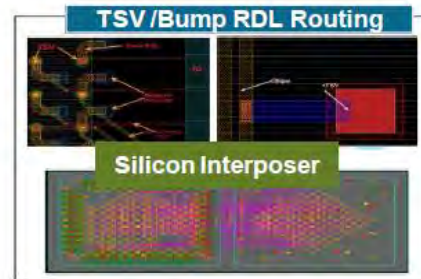
System Level Exploration



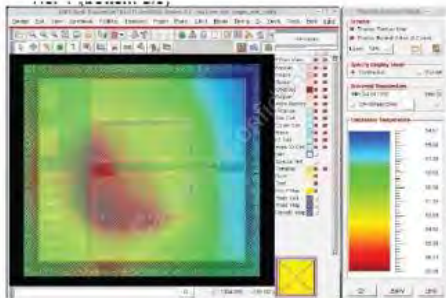
3D Aware Die Floorplan Optimize power & TSV/Bump locations



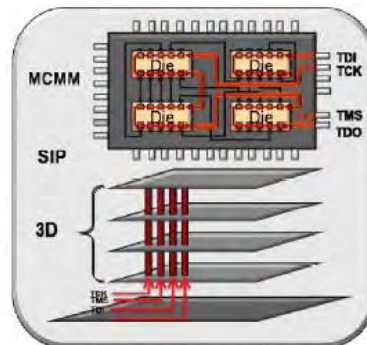
Die Implementation Placement, Optimization and Routing



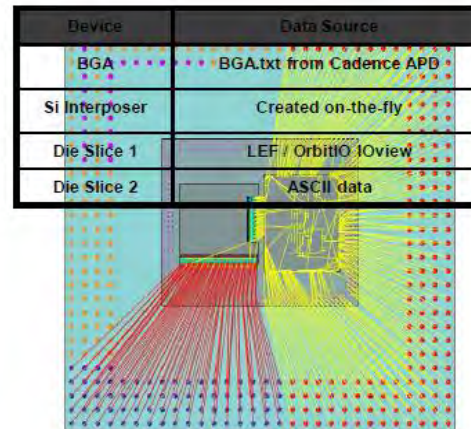
Multi Die Extraction & Analysis Manage Power, Thermal and SI



DFT for 3DIC Stack & Diagnostics



Silicon Package Co-Design

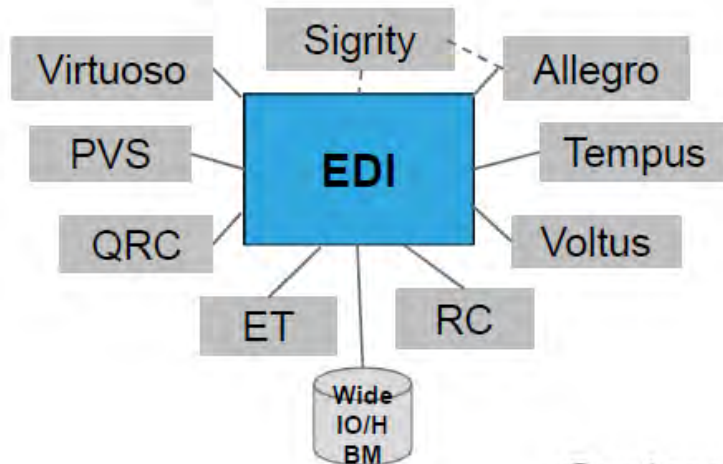


Multi-Fabric
Planning View

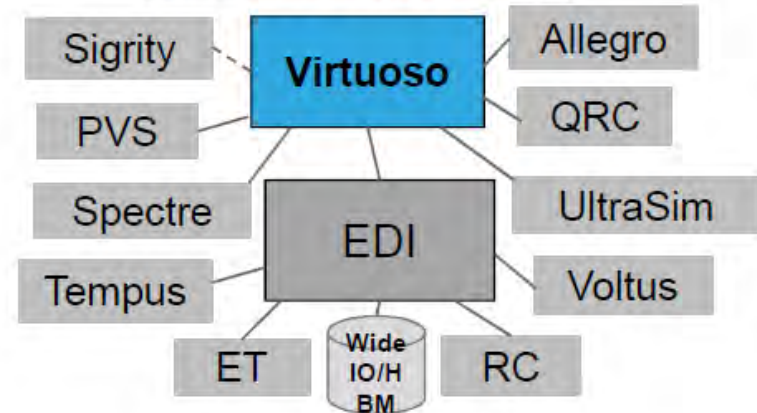
cadence®

Cadence 3D/2.5D Solutions with flexible Implementation Cockpits

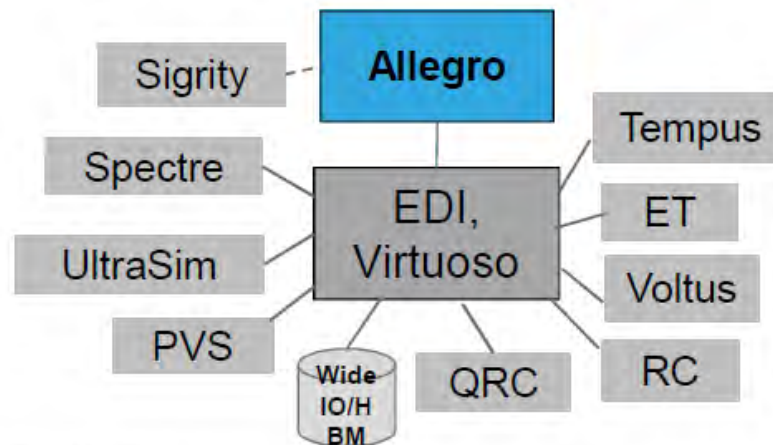
SOC entry point



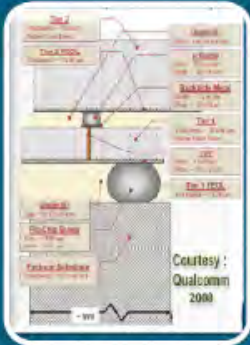
Virtuoso entry point



System entry point

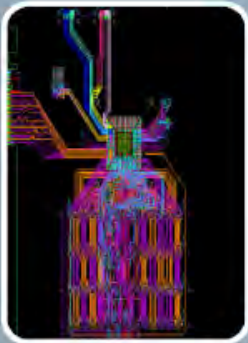


Cadence 3D-IC Integrated Solution



Complete Implementation Platforms for flexible Entry Point and Seamless Co-design

Using OpenAccess, EDI, Virtuoso™ each has dedicated 3DIC functions that work together, plus co-design with Cadence SiP tools for complete End to End implementation including early stage system exploration and feasibility
3D-IC Planning using OrbitIO



Full Spectrum Analysis Capability

RC/ET DFT and ATPG for 3DIC

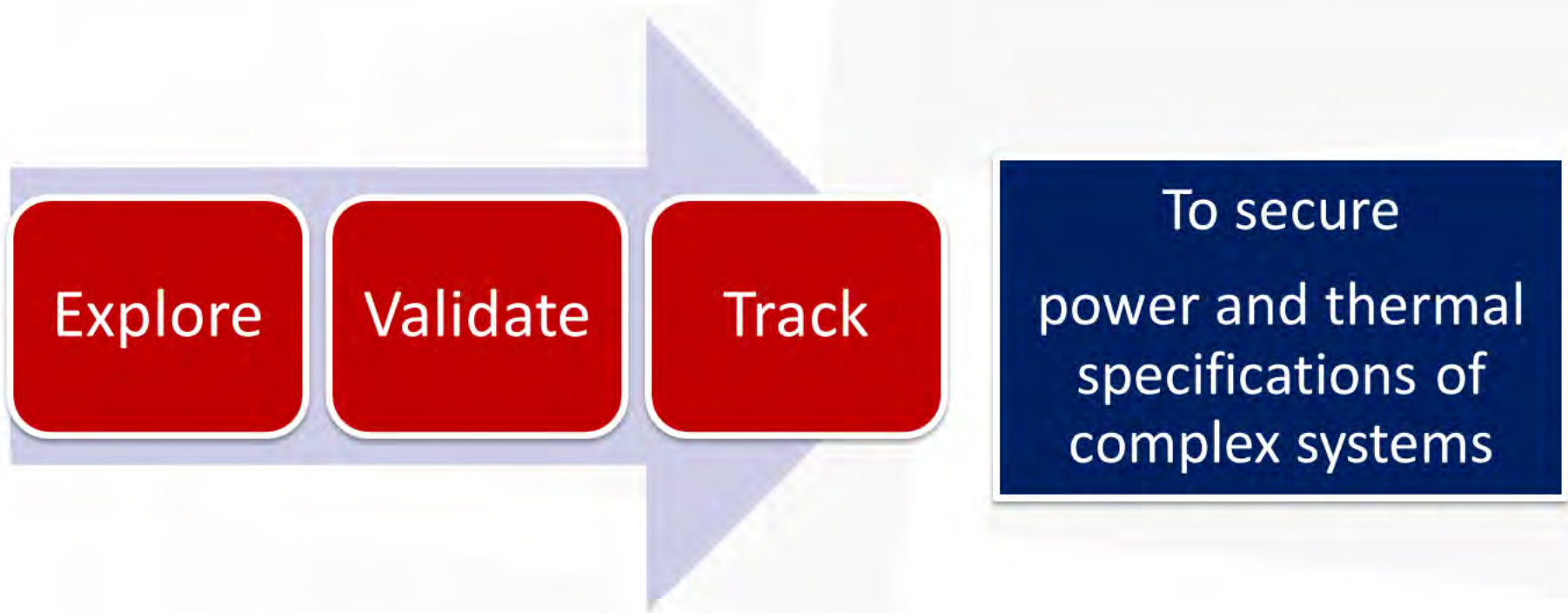
Voltus/Tempus/QRC Digital Analysis Tool

Virtuoso™ Based Full Spice Simulation in multiple processes concurrently

SiP/Sigrity™ based Extraction, SI, and PI System/Package Analysis

PowerDC Thermal Analysis

Docea solutions



Docea Power: Modeling and Analysis Flow

Functional

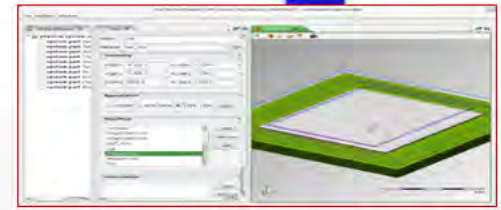
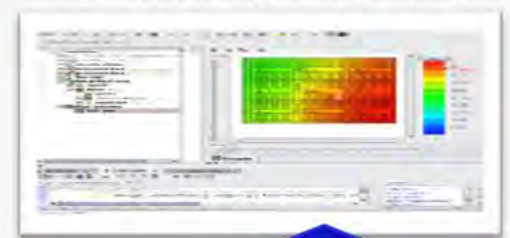


AceTLMConnect™

(API/Library for functional, power, thermal parameter monitoring & co-simulation link)

Power Aceplorer™

Power modeling and coupled Power/Thermal simulation

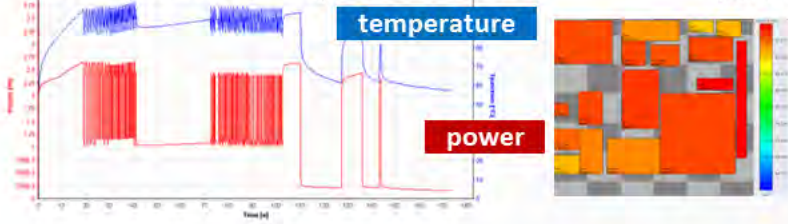


AceThermalModeler™

Dynamic Compact Thermal Model Generation

Thermal

Temporal and Spatial Effects



Increasing thermal issues

- Technology scaling => higher power density
- 3D stacking with TSV => greater thermal issues

MPSoC architectures

- Dynamic applications, variable execution time
- Power management solutions (DVFS), can even worsen thermal properties!

➔ **Thermal mitigation schemes must be proposed at design time**

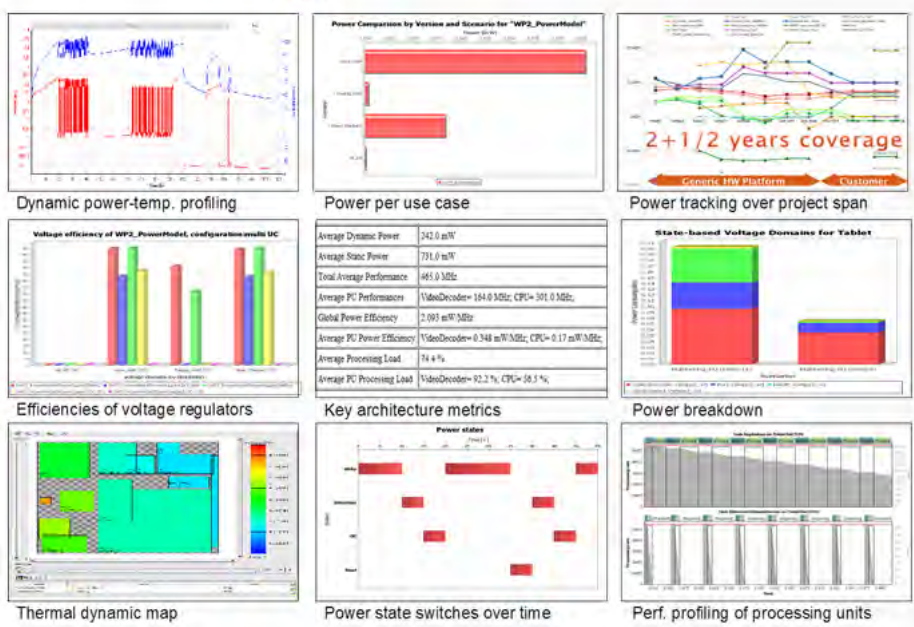
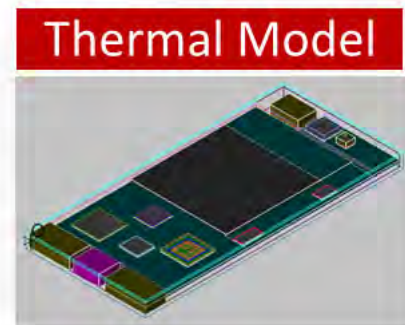
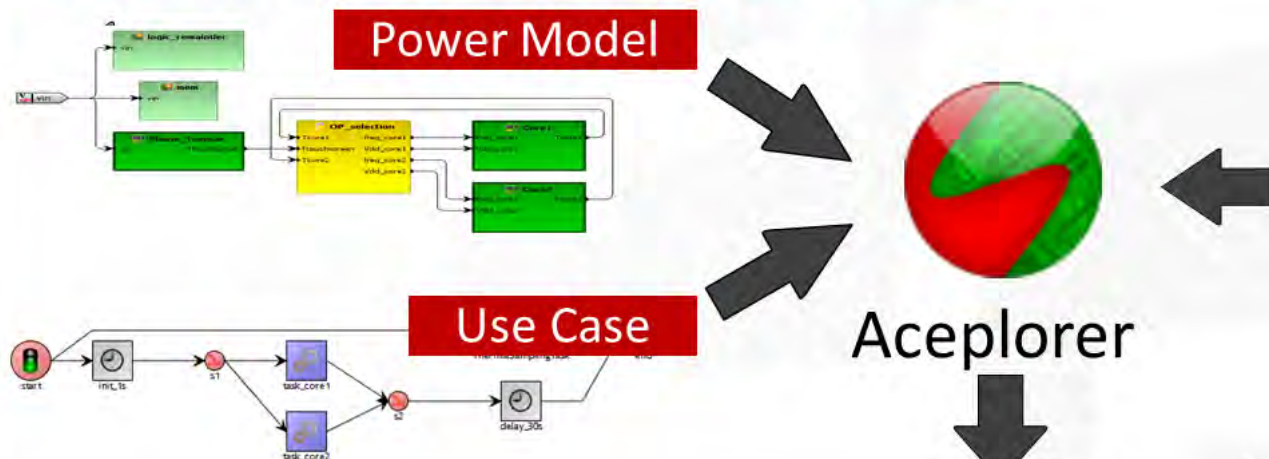


Temperature impacts

- Power consumption
- Peak performance
- Ageing
- Package costs

Architecture Exploration: Power/Thermal/Performance Trade-off

- Converge on design targets earlier and optimize performance



- ✓ Voltage/Clock Domain Analysis
- ✓ Power/Thermal Management Policies
- ✓ Performance vs. Power trade-off
- ✓ HW/SW partitioning
- ✓ Power Tracking per Use case
- ✓ VR, Power Delivery Efficiency
- ✓ Leakage Power-Temp Coupling
- ✓ Floor plan and Sensor Placement
- ✓ Task Scheduling and OS/Application Interaction
- ✓ ID Hot Spots and Design tradeoffs

Path Finding YOUR solution

- **How do you choose the **right technology** to meet performance goals?**
 - 3D Vs 2.5D Vs 2D
 - Flip chip Vs Wire Bond
 - Microbumps Vs Solder Bumps
 - Silicon Vs Glass Interposer
 - **For a technology: how do you decide the **optimum structure**?**
 - Via Array topology
 - RDL topology
 - Signal/PDN Assignments
 - **For a technology and structure: how **do you account for**?**
 - Process variations
 - Interactions
 - **Requires 1000s of tests early in the design cycle**
 - **Using existing tools are:**
 - Expensive and time consuming
 - Requires expert staff, many licenses and machines
 - Restricts exploration
- **Try “3DPF”, specifically created for Path Finding requirements!**

“Best technical simulation GUI I’ve ever used. It is quick, responsive, logically organized, and intuitive.....I do really like it.” (*From a large IC Foundry*)

“Experiments are much easier to set up than with competing tools, dramatically reducing setup time costs.” (*From a large IC Foundry & large IC Company*)

“Similar to other commercial tool responses but with less CPU time”
(*From a large IC Company*)

For an easy test drive, contact us at:

info@e-systemdesign.com

Definitive book on 2.5/3D Design and Modeling:

<http://www.e-systemdesign.com/pdfs/SwamiNew3DBookFlyer.pdf>

V2.0 Datasheet (V3.0 in Beta testing):

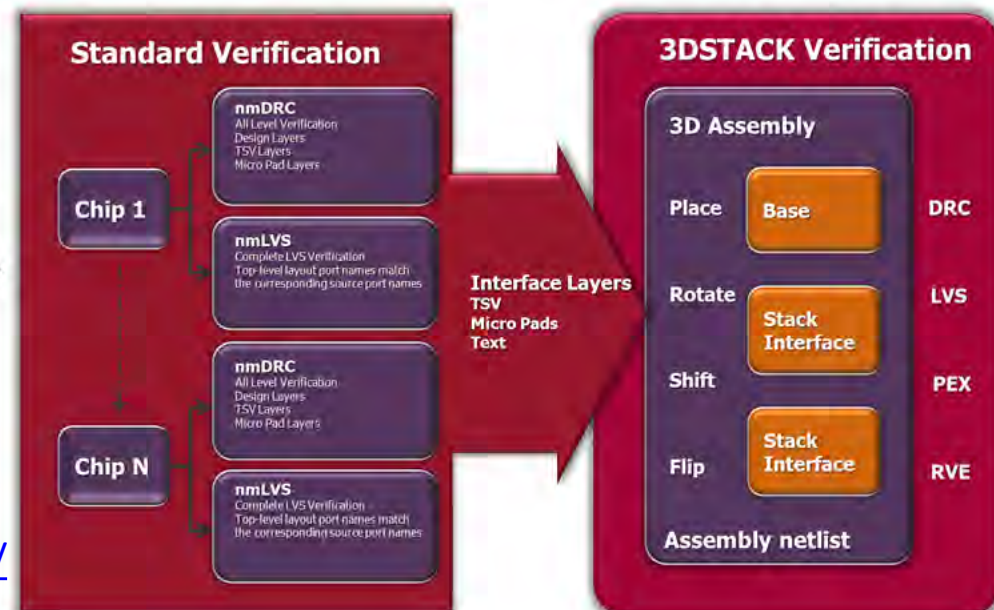
http://www.e-systemdesign.com/pdfs/Sphinx3DPFV2_2013.pdf

Other 2.5/3D white papers and videos:

<http://www.e-systemdesign.com/Collateral.html>

Calibre 3DSTACK Summary

- Maintains standard DRC, LVS, PEX verification processes to verify independent die
- Performs 3D interface verification
 - Verify physical: offset, rotation, scaling, etc...
 - Trace connectivity of interposer or die-to-die
- Benefits
 - Minimal disruption to existing verification flows
 - Superior performance and memory vs. "mega-merge"
 - Simple debugging
 - Maximum flexibility



<http://www.mentor.com/solutions/3d-ic-design/>

3DIC Flows and Models for Analog and Digital

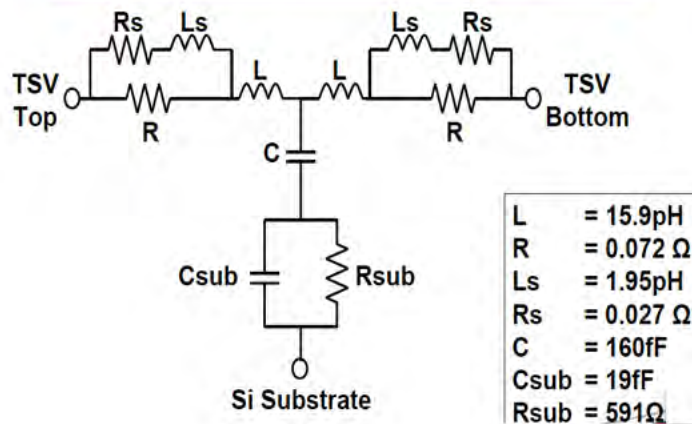
Analog flow

Accurate TSV model

Treat TSV as a LVS device

LVS device = Spice subcircuit

Spice simulation



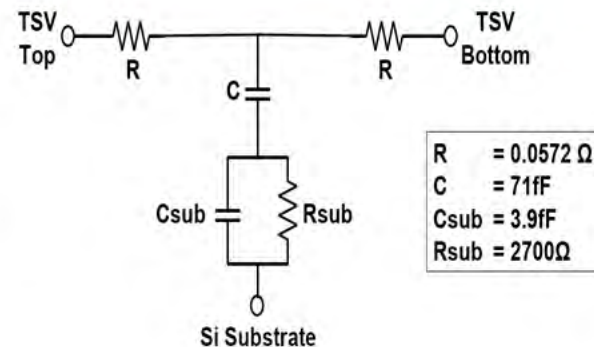
Digital flow

Lower accuracy requirements

Treat TSV as a via

Extraction tool \rightarrow R(C) model

Static timing analysis



3D IC Test Challenges and Mentor Approaches

- Known good die prior to 3D packaging
 - Thorough tests and contactless IO tests
- Package level test generation
 - Retarget BIST and scan patterns from die level
- Die to die interconnect test
 - Simple boundary scan structure at IO
- External RAM test
 - Test through PHY on logic die
- Partial stack test?
 - Possible with pattern retargeting, contactless IO test, and interconnect test



Tessent® 3D Test Solutions

- Based on plug-and-play principles
 - Pattern retargeting, common TAP structure in each die
- TAP as the common interface
 - Same patterns and TAP interface for wafer, individually packaged die, partial stack, and 3D package
- JTAG enables flexibility for changing requirements
- Minimize DFT work at the 3D package level
 - Common die level test structures
 - All scan ATPG and BIST performed at the die level and retargeted

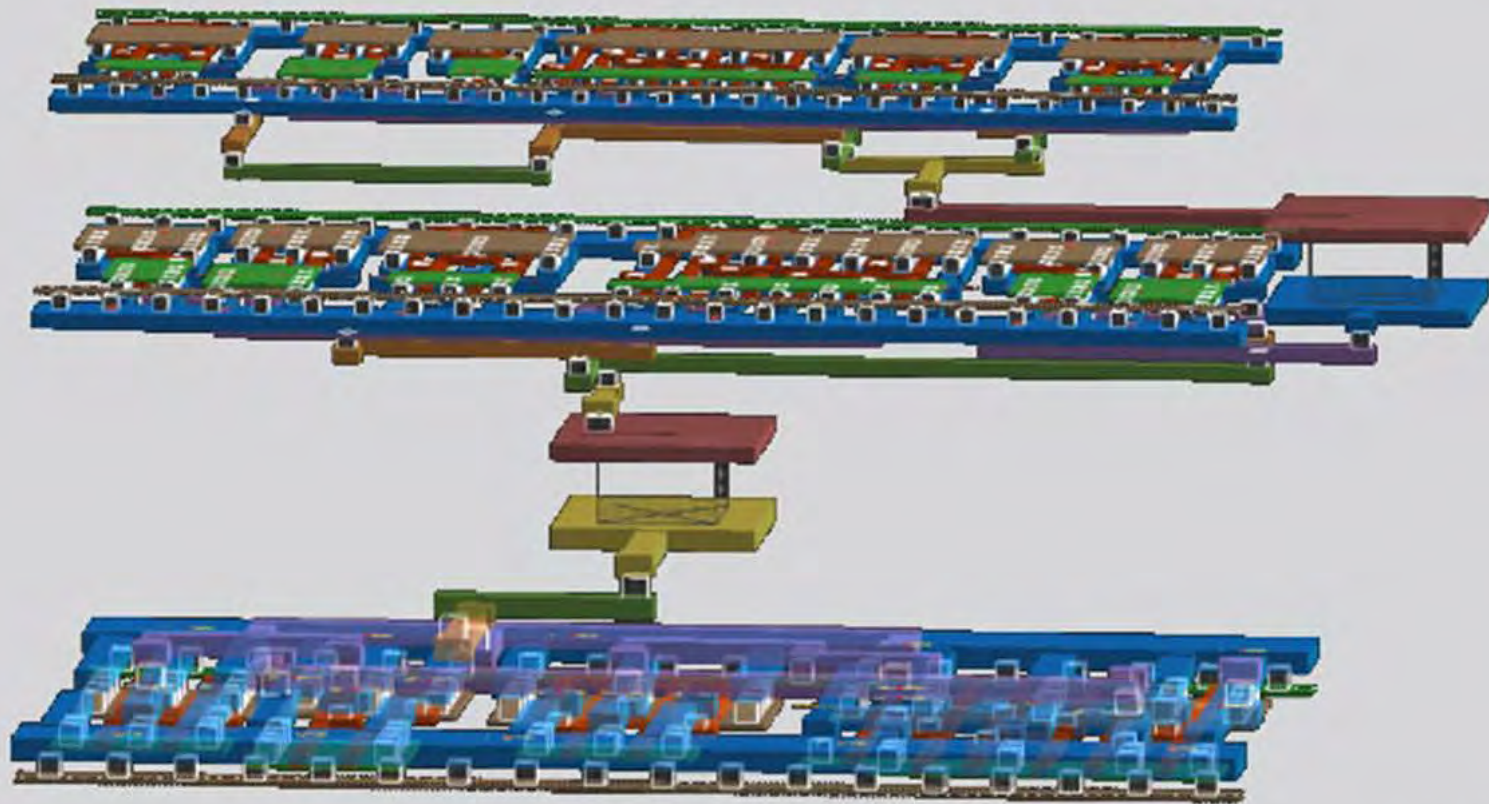
White paper available at: www.mentor.com/products/silicon-yield/techpubs/download/?id=82511



MAX-3D Design Suite

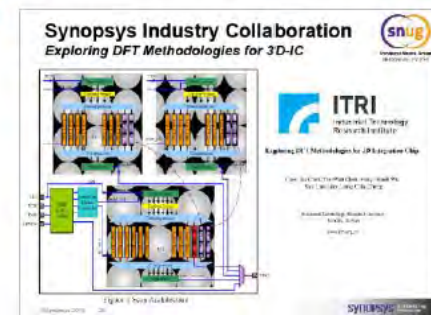
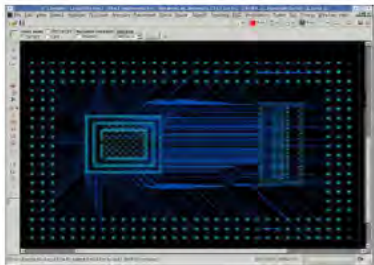
- **MAX-3D** for true 3-dimensional layout, supporting multiple distinct technology files for Through-Silicon Via 3D wafer-stack and interposer design.
- **MAX-3D TSV Placer** for automatically locating, optimizing and placing TSVs.
- **MAX-3D Path Finder** to explore viability of interposer or stacked-die implementations.

MAX-3D Viewed in 3D Mode

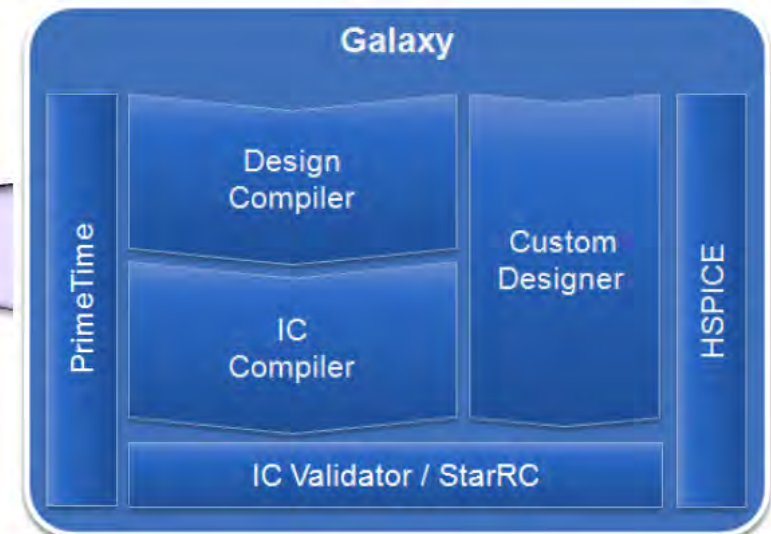
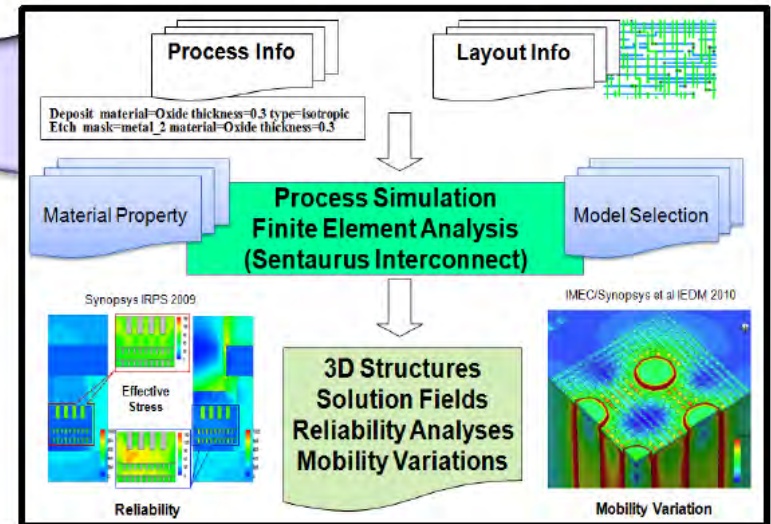
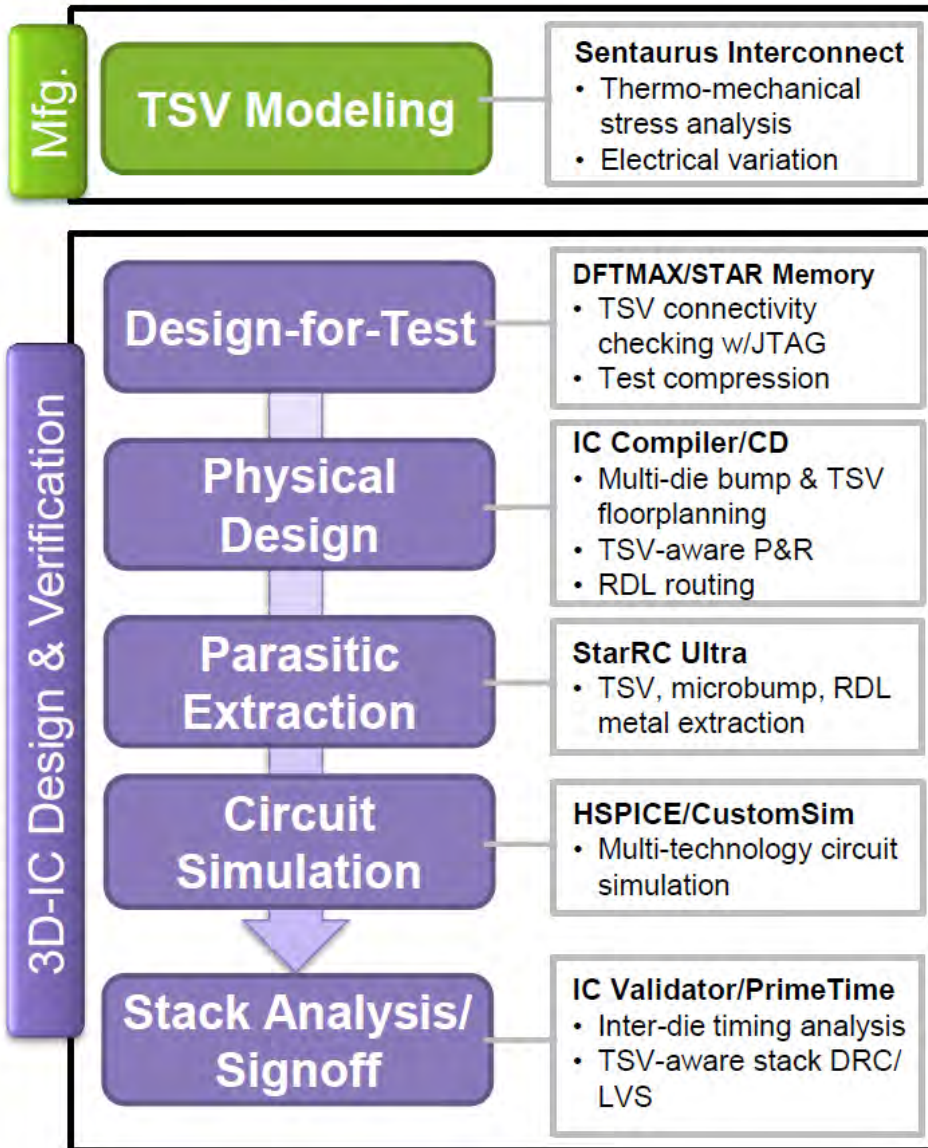


3D-IC Status At Synopsys

- ✓ Committed to supporting 3D-IC EDA tools, technologies, and flows for implementation, test, and verification
 - ✓ 3D support integrated throughout our Galaxy tool set
- ✓ Both silicon interposer (2.5D) and stacked-die (3D) designs supported
- ✓ Driving the IEEE P1838 **Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits** (Synopsys Co-Chair)
- ✓ <http://www.synopsys.com/Solutions/EndSolutions/3D-IC-Solutions/Pages/default.aspx>



Synopsys 2.5D/3D-IC Solution Today



Foundry-Certified 3D-IC Support

- Achieved Reference Flow foundry certification for TSMC (2.5D and 3D) and GlobalFoundries (2.5D)

News Release

Synopsys and TSMC Deliver 3D-IC Design Support

Design Tools Selected in TSMC's First Integrated, Validated Reference Flow and Design Kit Enabling Multi-Die Integration Using TSMC CoWoS Technology

MOUNTAIN VIEW, Calif., Oct. 11, 2012 /PRNewswire/ --

Highlights:

- Supports multi-die integration using TSMC CoWoS™ technology
- Includes enhanced versions of Synopsys' Galaxy™ Implementation Platform tools
- Increases productivity, accelerates time to market and speeds time to volume

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that it is delivering a comprehensive 3D-IC design solution that is included in TSMC's CoWoS™ (Chip on Wafer on Substrate) Reference Flow. The design flow is the result of the latest collaboration between the companies on 3D-IC integration technologies. It provides a smooth transition from a traditional "2D" integrated circuit (IC) to a multi-die stacking design flow. In support of the TSMC CoWoS reference flow, Synopsys has released enhanced versions of its Galaxy Implementation Platform tools for physical implementation, parasitic extraction, physical verification and timing analysis. With the new flow and tool enhancements, engineers can increase productivity, shorten time-to-market and speed time-to-volume when designing multi-die systems for TSMC CoWoS silicon.

<http://www.globalfoundries.com/newsroom/press-releases/2013/12/28/globalfoundries-introduces-certified-design-flows-for-multi-die-integration-using-2.5d-ic-technology>



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GLOBALFOUNDRIES Introduces Certified Design Flows for Multi-Die Integration Using 2.5D IC technology

Collaboration with leading EDA vendors supports complete range of steps required to create and verify advanced stacking implementations using TSV and interposer approaches

Milpitas, Calif. — May 30, 2013 — At next week's 50th Design Automation Conference (DAC) in Austin, Texas, GLOBALFOUNDRIES will unveil a comprehensive set of certified design flows to support 2.5D IC product development with its most advanced manufacturing processes. The sign-off ready flows, jointly developed with the leading EDA providers, offer robust support for implementing designs using sophisticated multi-die packaging techniques, leveraging through-silicon vias (TSVs) in 2.5D silicon interposers and new bonding approaches.

Multi-vendor support is available, with full implementation flows from Synopsys and Cadence Design Systems. Physical verification with Mentor Graphics' suite of tools is included in the flow.

<http://news.synopsys.com/index.php?s=20295&item=123443>

- Introduction
- Why do we need 2.5D/3D Technology ?
 - Business reasons
 - Technical considerations
- 2.5D/3D key benefits and challenges
 - Application-specific benefits
 - Additional design challenges
- 2.5D/3D EDA vendor updates
 - Si2 Open 3D TAB
 - Ansys, Atrenta, Cadence, Docea, eSystem, Mentor, MicroMagic, Synopsys
- **Summary, Q & A**

- 2D to 2.5D/3D shift is happening now
- Cooperation & Standards will accelerate transition
- 2.5D/3D-ICs need 2D-ICs as building blocks
- EDA is small, but very important for the EcoSystem
 - It's the bridge from idea to product manufacturing
 - EDA reduces risk, TTM, IC cost and assures reliability
 - IP blocks for SoCs →→→ Die-level IP for 2.5D/3D-ICs
- Q & A

APPENDIX

- [Handbook of 3D Integration: Volume 3 – 3D Process Technology](#) by Phil Garrou, Mitsumasa Koyanagi and Peter Ramm (June 2014)
- [Design and Modeling for 3DICs and Interposers](#) by Madhavan Swaminathan and Ki Jin Han (Jan 2014)
- [Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs](#) by Brandon Noia and Krishnendu Chakrabarty (2013)
- [Advanced Flip Chip Packaging](#) by Ho-Ming Tong, Yi-Shao Lai and C.P. Wong (Apr 4, 2013)
- [Designing TSVs for 3D Integrated Circuits \(SpringerBriefs in Electrical and Computer Engineering\)](#) Nauman Khan, Soha Hassoun (2012)
- [Through-Silicon Vias for 3D Integration](#) by John Lau (Sep 20, 2012)
- [Chips 2020: A Guide to the Future of Nanoelectronics \(The Frontiers Collection\)](#) by Bernd Hoefflinger (2012)
- [Handbook of 3D Integration: Volumes 1 and 2 - Technology and Applications of 3D Integrated Circuits](#) Garrou, Bower and Ramm (2012)
- [Electrical Modeling and Design for 3D System Integration: 3D Integrated Circuits and Packaging, Signal Integrity...](#) by Er-Ping Li (2012)
- [Design for High Performance, Low Power, and Reliable 3D Integrated Circuits](#) by Lim, Sung Kyu (2012)
- [Design Technology for Heterogeneous Embedded Systems](#) by Nicolescu, Gabriela, O'Connor, Ian and Piguet, Christian (2012)
- [Semiconductor Packaging: Materials Interaction and Reliability](#) by Andrea and Chen (2012)
- [Handbook of Wafer Bonding](#) by Peter Ramm, James Jian-Qiang Lu and Maaiké M. V. Taklo (2012)
- [Handbook of 3D Integration: Volumes 1 and 2 - Technology and Applications of 3D Integrated Circuits](#) by Garrou, Bower, Ramm (2012)
- [Stress Management for 3D ICs Using Through Silicon Vias:: International Workshop on Stress Management for 3D ICs...](#) Ehrenfried Zschech, Riko Radojicic, Valeriy Sukharev and Larry Smith (2011)
- [3D IC Stacking Technology](#) by Banqiu Wu, Ajay Kumar and Sesh Ramaswami (2011)
- [3D Integration for NoC-based SoC Architectures \(Integrated Circuits and Systems\)](#) Abbas Sheibanyrad, Frédéric Pétrot, Axel Jantsch (2010)
- [Reliability of RoHS-Compliant 2D and 3D IC Interconnects \(Electronic Engineering\)](#) by Lau, John H. (2010)
- [More than Moore: Creating High Value Micro/Nanoelectronics Systems](#) by Zhang, Guo Qi and Roosmalen, Alfred (2010)
- [Wafer Level 3-D ICs Process Technology \(Integrated Circuits and Systems\)](#) by Tan, Chuan Seng, Gutmann, Ronald J. and Reif, L. Rafael (2010)
- [Three Dimensional System Integration: IC Stacking Process and Design](#) by Papanikolaou, Antonis, Soudris, Dimitrios, Radojicic, Riko (2010)
- [3D Integration for NoC-based SoC Architectures \(Integrated Circuits and Systems\)](#) by Abbas Sheibanyrad, Frédéric Pétrot and Axel Jantsch (2010)
- [Ultra-thin Chip Technology and Applications](#) by Burghartz, Joachim (2010)
- [3-Dimensional VLSI: A 2.5-Dimensional Integration Scheme](#) by Deng, Yangdong and Maly, Wojciech P. (2010)
- [Three-dimensional Integrated Circuit Design \(Systems on Silicon\)](#) by Pavlidis, Vasileios F. and Friedman, Eby G. (2010)

eda2asic Major Conferences with 2.5D/3D Content

[European 3D TSV Summit](#)

20-22 January 2014, Grenoble, France

[International Solid-State Circuits Conference \(ISSCC\)](#)

9-13 February 2014, San Francisco, CA

[International Symposium on Quality Electronic Design \(ISQED\)](#)

10-12 March 2014, Santa Clara, CA

[IMAPS Device Packaging Conference](#)

11-13 March 2014, Scottsdale/Fountain Hills, AZ

[Design, Automation, and Test in Europe \(DATE\)](#)

24-28 March 2014, Dresden, Germany

[Electronic Components and Technology Conference \(ECTC\)](#)

27-30 May 2014, Lake Buena Vista, FL

[Design Automation Conference \(DAC\)](#)

1-5 June 2014, Austin, TX

[SEMICON West](#)

8-10 July 2014, San Francisco, CA

[IEEE International System-on-Chip Conference](#)

3-5 September 2014, Las Vegas, NV

[SEMICON Europa and Advanced Packaging Conference](#)

9-11 October 2014, Dresden, Germany

[International Symposium on Microelectronics \(IMAPS\)](#)

13-16 October 2014, San Diego, CA

[International Wafer-Level Packaging \(IWLPC\)](#)

11-13 November 2014, San Jose CA

[3D Architectures for Semiconductor Integration and Packaging \(3D ASIP\)](#)

10-12 December 2014, Burlingame, CA