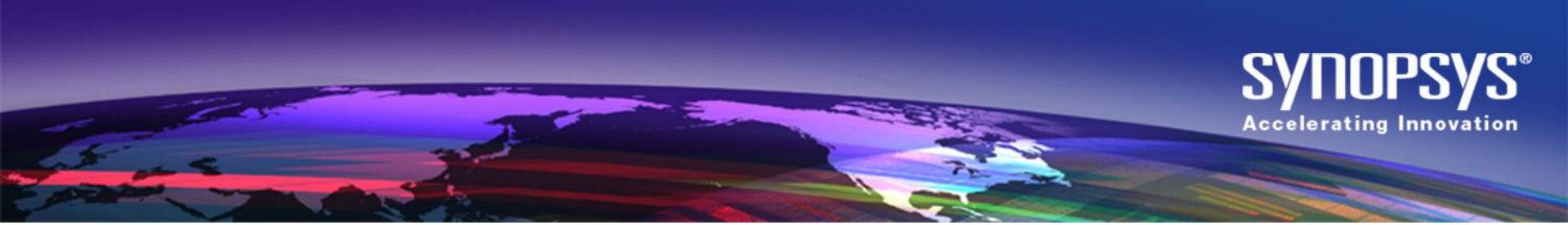


FinFETs
State of The Device

Jamil Kawa

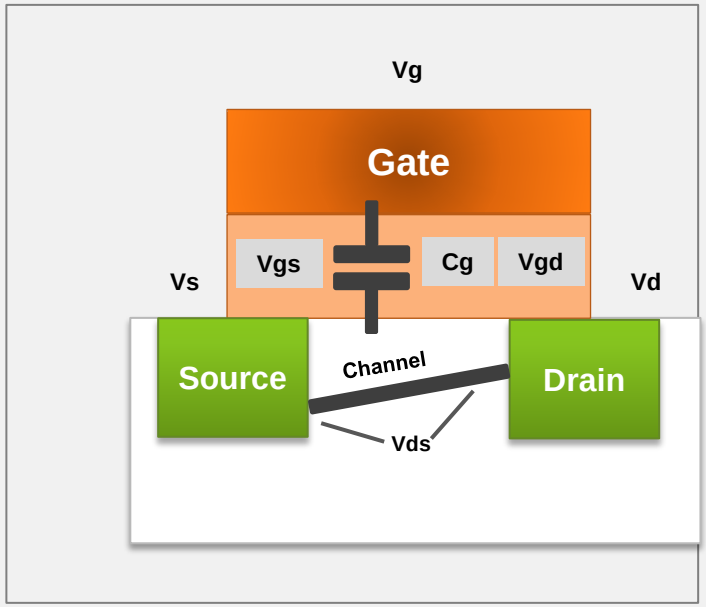
Synopsys Scientist

April 17, 2014

AGENDA

- From Planar to Multi-Gates (FinFET)
- FinFETs Today
- Device Technology – 10nm and Beyond
- Summary and Conclusions

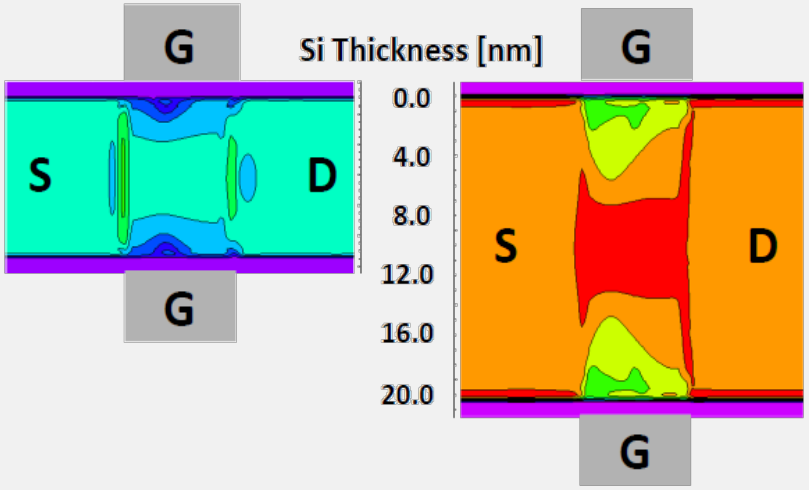
Progression from Planar to Multi-Gates



L_g = 25 nm; $T_{ox,eq}$ = 12Å

T_{Si} = 10 nm

T_{Si} = 20 nm



Leakage Current Density [A/cm²] @ V_{DS} = 0.7 V

- Gate coupling to substrate getting weaker with scaling
- Control does not exceed 5nm from surface

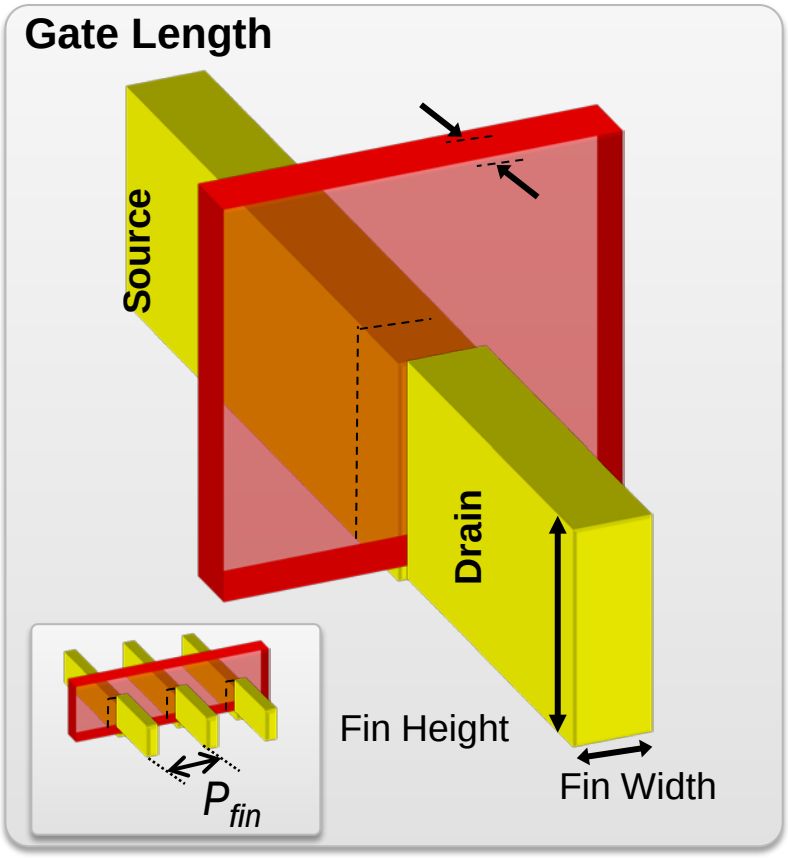
I_{off} = 2.1 nA/µm

I_{off} = 19 µA/µm

Tsi < ½ * L fog good channel control

FinFET Design Considerations

- **Fin Width**
  - Determines short channel effects
- **Fin Height**
  - Determines Current
  - Limited by etch technology
  - Also limited by mechanical stability
- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance vs. layout efficiency



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Status of FinFET technology today

- 22nm Trigate is in full production
- 16nm / 14 nm proven is silicon (testchips)
  - Production (yield) 1 to 2 years away
- 10nm: No major show-stoppers
  - Major Foundries working on it for over a year
  - Tools are in intermediate stages of development / partner interaction
  - The metrics of **accuracy**, **performance** and **run time** dominates
- The10 nm device is FinFET
  - Channel and Source/drain engineering is focus
  - Interconnect reaching the limits τ =80ns – significant bottleneck!!
    - Layout and design experience make a HUGE impact
    - IP architecture is critical

Status of FinFET technology today

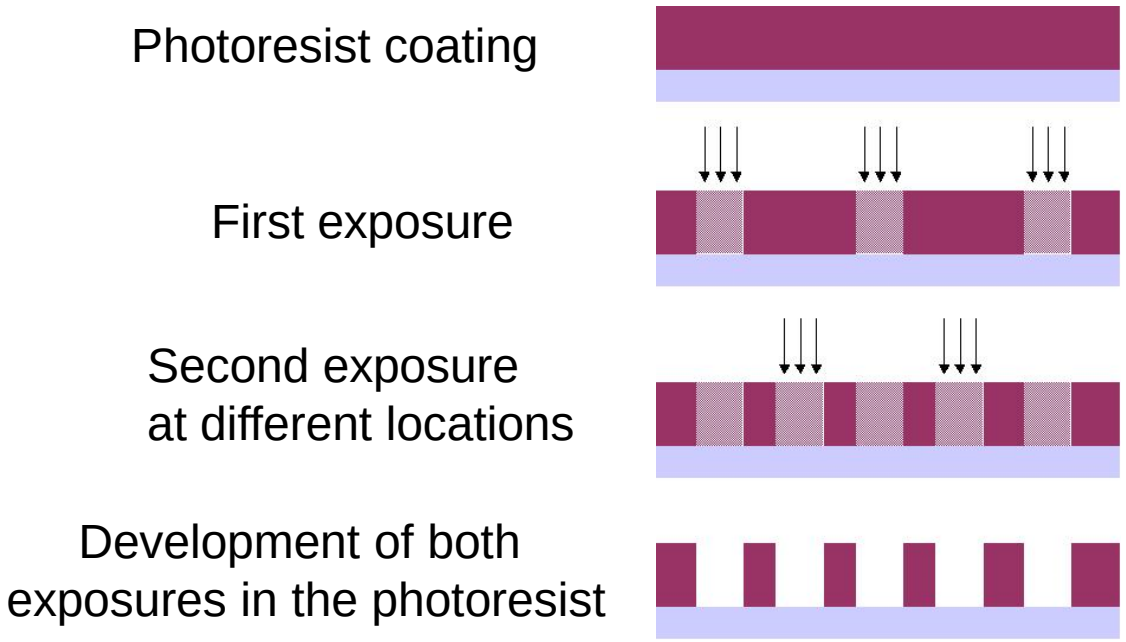
- Feasibility & Cost are two major factors in determining among Litho alternatives (LELE vs. SADP, etc..)
  - Has Layout Rules, Tools and IP implications)
- On the surface ….. Tools for 10nm are no different than for 14 nm /16nm given the device is more or less the same… but to maintain the triad of Accuracy, Performance, and Runtime,… tools are significantly impacted
- Largest impact on tools will be in
  - Simulation
  - Lithography
  - IP / Routing
  - Extraction
  - Verification (special constructs, fuzzy pattern matching), etc.

Some challenges for 10nm technology

- Simulation:
  - Netlist elements growing 3X-5X compared to 28nm
  - More complex BSIM-CMG model
  - Higher switching speeds -> smaller time-step -> simulation time without tools enhancements is 12X slower than planar.
    - Multi threading + other simulation enhancements brings it back to 2X-3X range
- Lithography: converging on solutions for 10nm
  - Spacer is Poly (SIP) for gate , LELELE (TPT) for M1 and contact, Spacer is Dielectric (SID) for Mx layers. QUAD patterning for 10nm lower interconnect?
  - TPT decomposition likely to be done by designers.
    - Subject of debate

Double Patterning Technology

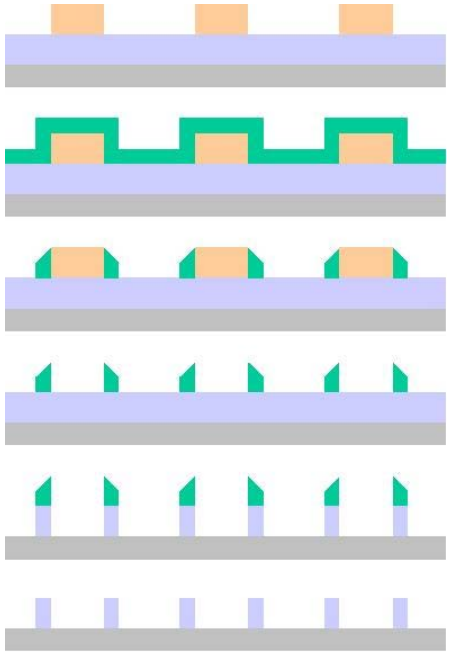
- Double exposure: a sequence of two separate exposures of the same photo-resist layer using two different photo-masks



Self-aligned Spacer: Basic Review

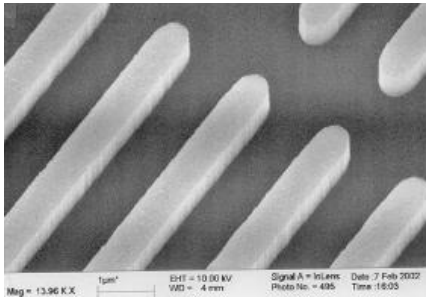
- A spacer is a film layer formed on the sidewall of a pre-patterned feature
- There are two spacers for every line, the line density has now double

1. First pattern
2. Deposition of mask material
3. Etching to from sidewall spacers
4. Removal of first pattern
5. Etching using remaining spacers as mask
6. Removal of spacer, leaving final pattern

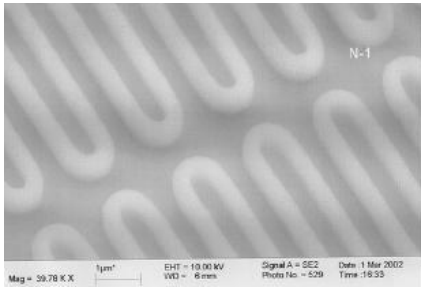


Spacer Lithography – Rinse and Repeat

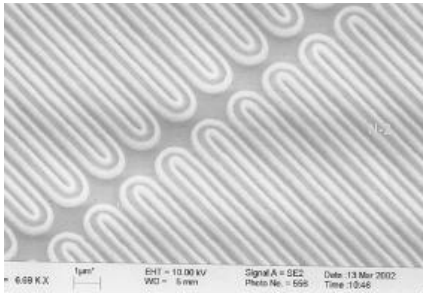
Photo-lithographically defined sacrificial structures



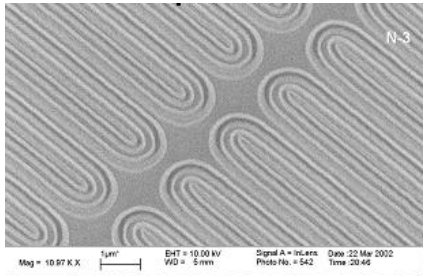
1st Spacers



2nd Spacers



3rd Spacers

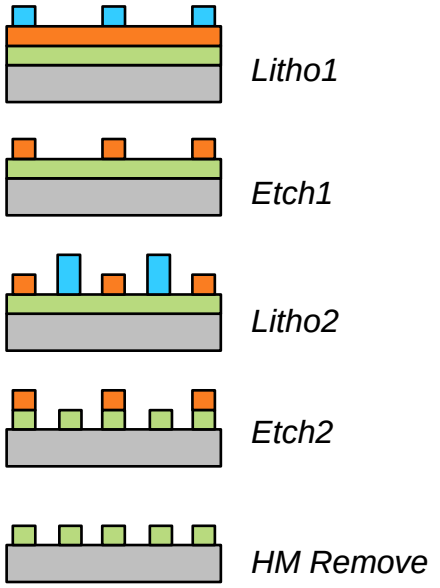


2^n lines after n iterations of spacer lithography!

- Many flavors of Spacer Lithography
  - SIP, SADP, SID, etc….
  - Flavor of Spacer has cost, tolerances, design rules, and verification implications

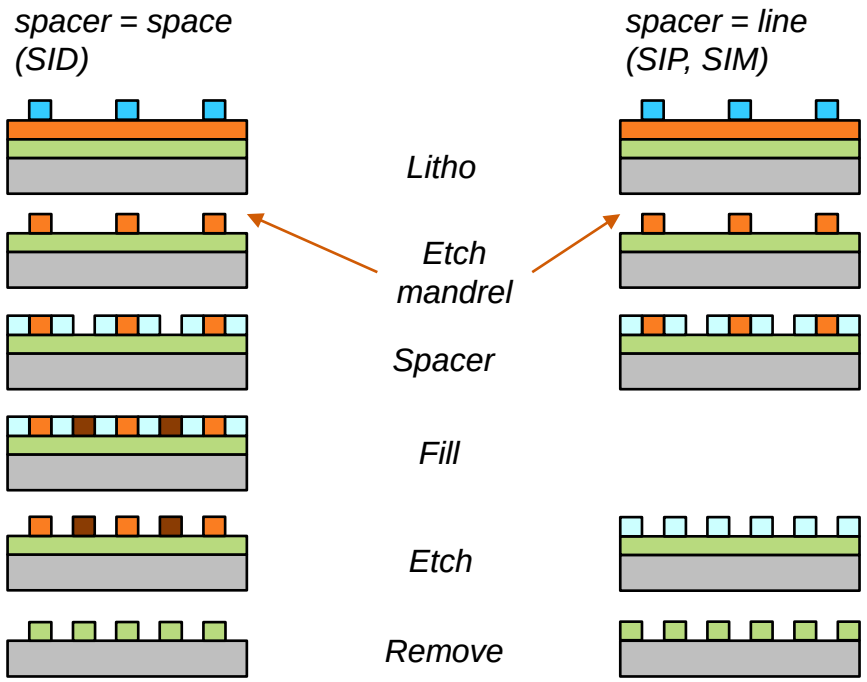
Double Patterning (DPT) Options

Litho-etch-litho-etch (LELE)



"Stitching" of patterns possible

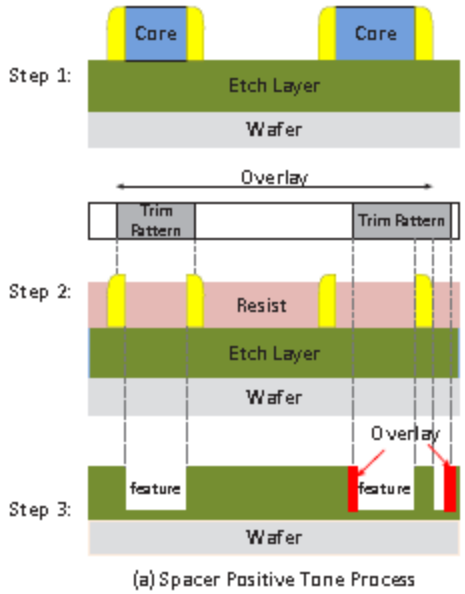
Self-aligned double patterning (SADP)



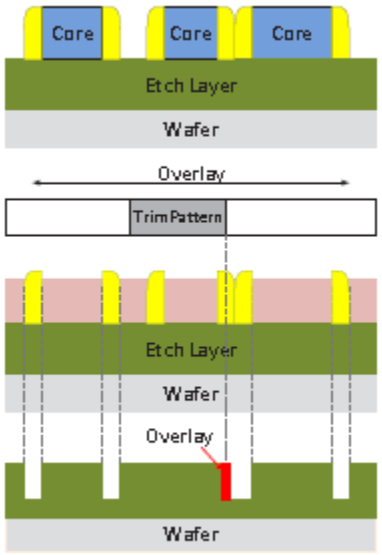
SADP requires additional trim masks

- Double patterning introduces significant variability in device and interconnect performance:
  - LELE: impacted by CD and overlay of each patterning step
  - Spacer: impacted by CD variation of mandrel, overlay only for trim masks (usually uncritical)
- Choice per layer depending on cost, variability needs

More on SADP – Positive / Negaive Tone



(a) Spacer Positive Tone Process



(b) Spacer Negative Tone Process

Positive Tone:

- Large flexibility on feature width and space
- Non-sidewall regions covered by trim mask are exposed
- Exposed material will be etched out to be the feature

Negative Tone:

- Sidewall regions define the trench
  - Design infelxibility
- Sidewall + NOT covered by trim is the trench / feature

Notice impact of sidewall / Trim on overlay

Diagrams from Zhang et al, 2013

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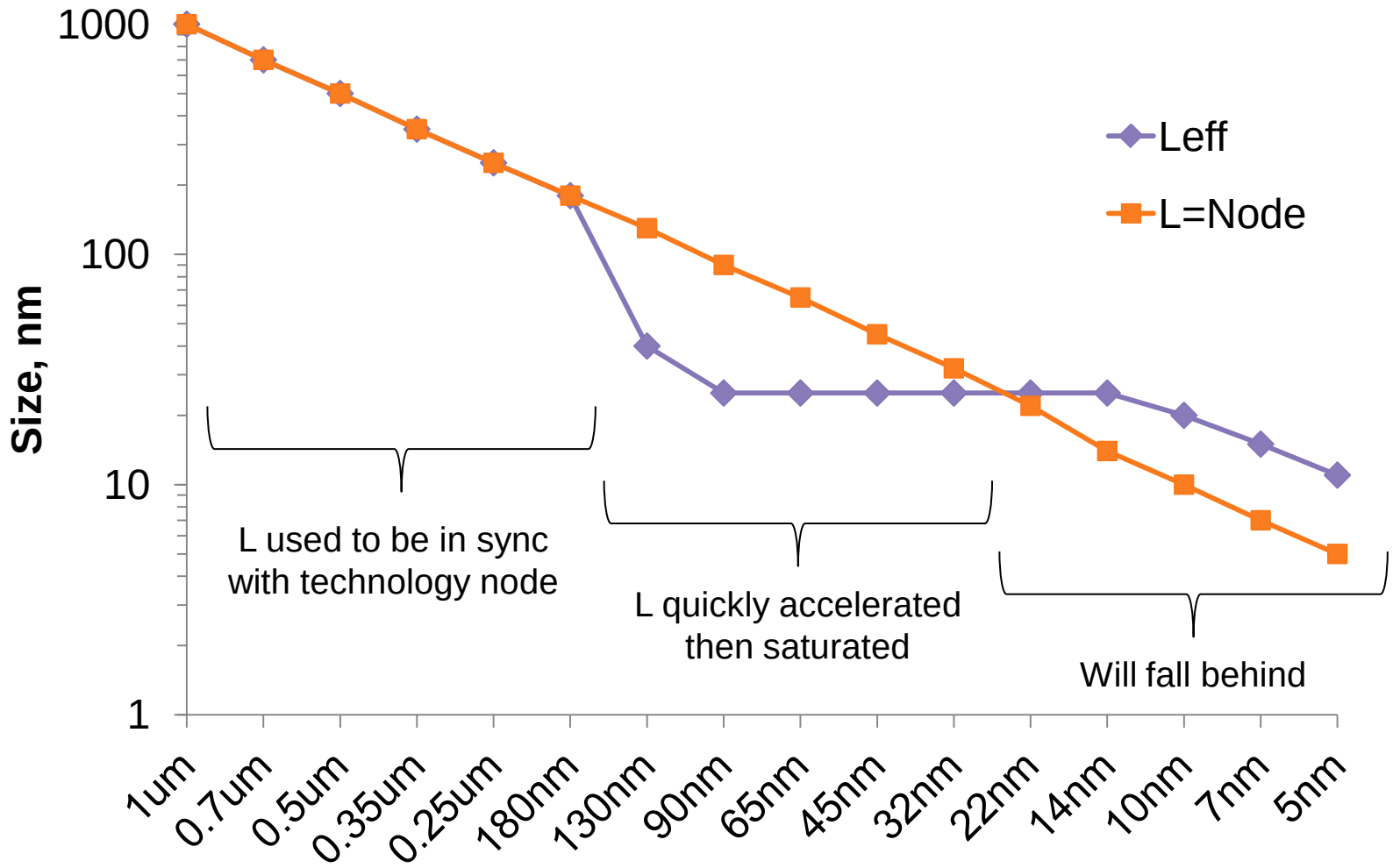
Evolution of Transistor Scaling

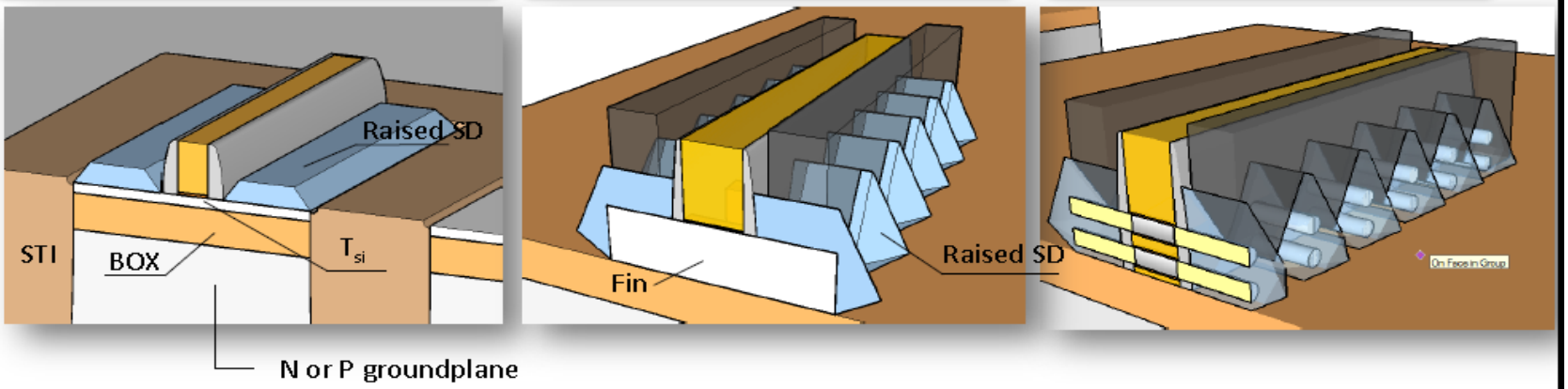


Device beyond 14nm: scaling to 3.5nm

Transistor Structure for 10nm and 7nm nodes

29

UTBB Ultra Thin Body & BOX	FinFET/Trigate	Nanowire



- Undoped channel
- Back-gate control using thin BOX capacitive coupling
- Raised S/D

- « Vertical » double gate
- Undoped or doped channel
- Multi-Fin
- Raised S/D

- Gate-All-Around
- Undoped channel
- Multi-wires
- Raised S/D

Challenges of 10nm and 7nm CMOS Technologies, IEDM Short Course, Dec. 8th 2013

From Frederic Boeuf, IEDM

Expected Design Rules

Foundry node	Gate pitch	L	Spa-cer	Fin top	Fin bottom	Fin height	Fin pitch	Contact size	EOT
16 / 14	90	25	18	5	15	35	48	29	0.9
10	63	20	11	5	11	32	34	21	0.85
7	44	15	7	5	7	30	24	15	0.8
5	32	11	5	5	Nano-wire	Stacked	20	11	0.8
3.5	22	7.5	3.5	4			13	7.5	
2.5	16	5	3		2D ma-terial		10	5	

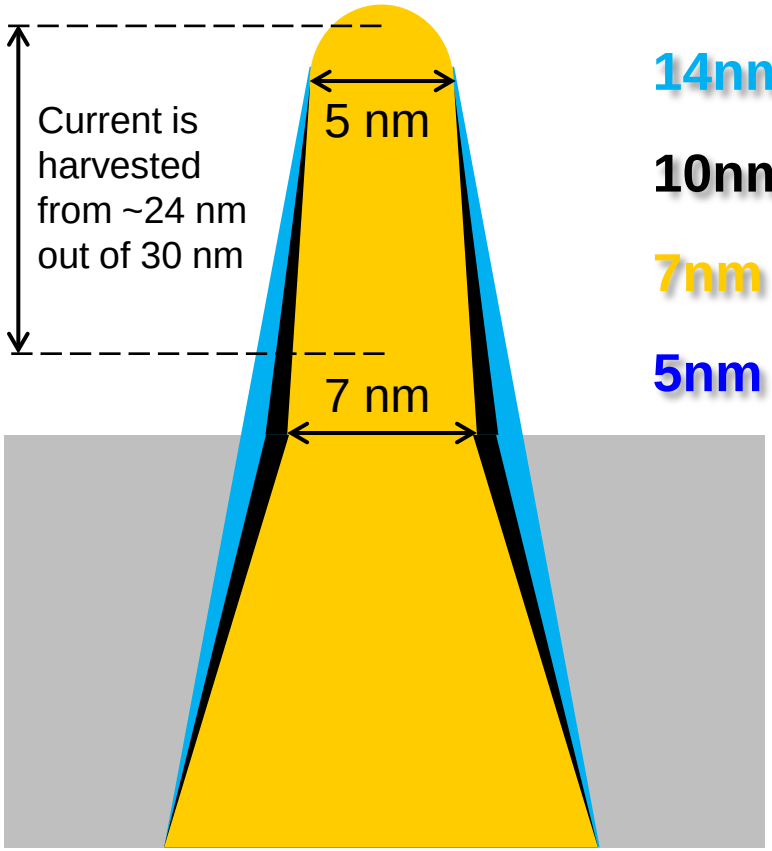
From Victor Moroz, Synopsys

Technology

Technology (foundries)	10nm	7nm	5nm	3.5nm	2.5nm
L, nm	20	15	11	7.5	5
Transistor architecture	FinFET	FinFET	Nano-wire	Nano-wire	2D material
Materials	Si	Si, SiGe, InGaAs	Si	Si	MoS_2
# of atoms in the channel	300 k	100 k	10 k	3 k	300

From Victor Moroz, Synopsys

Beyond FinFETs

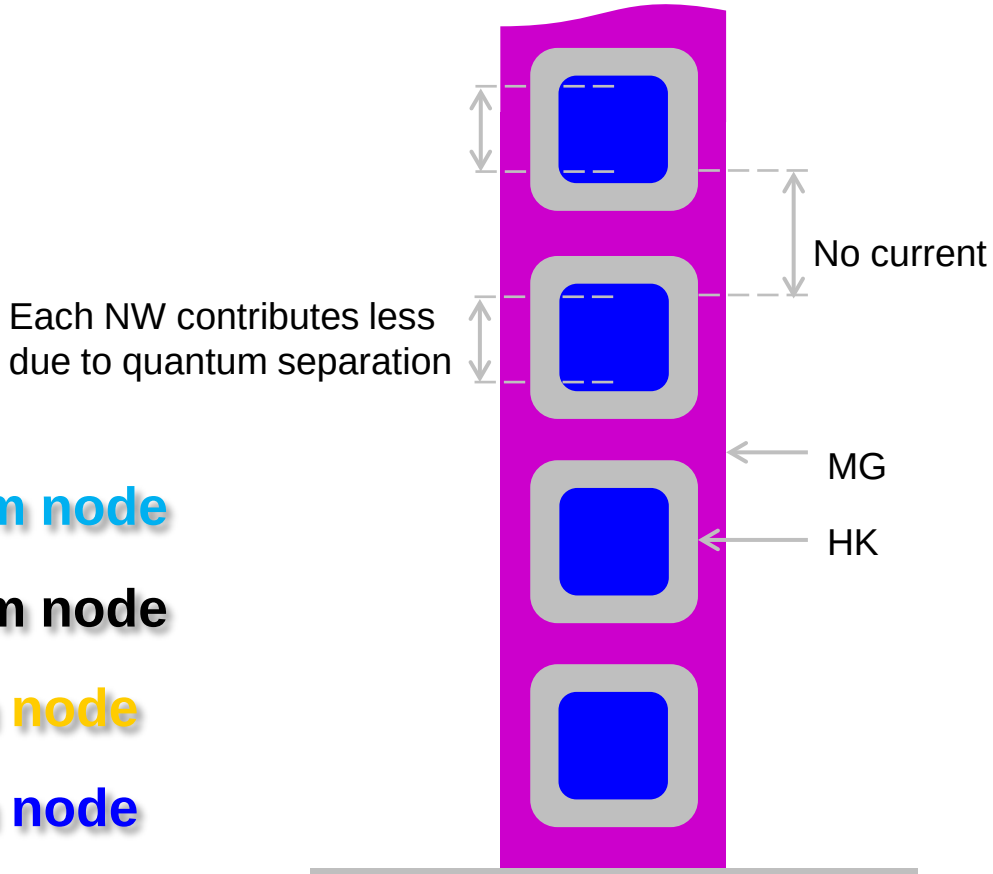


14nm node

10nm node

7nm node

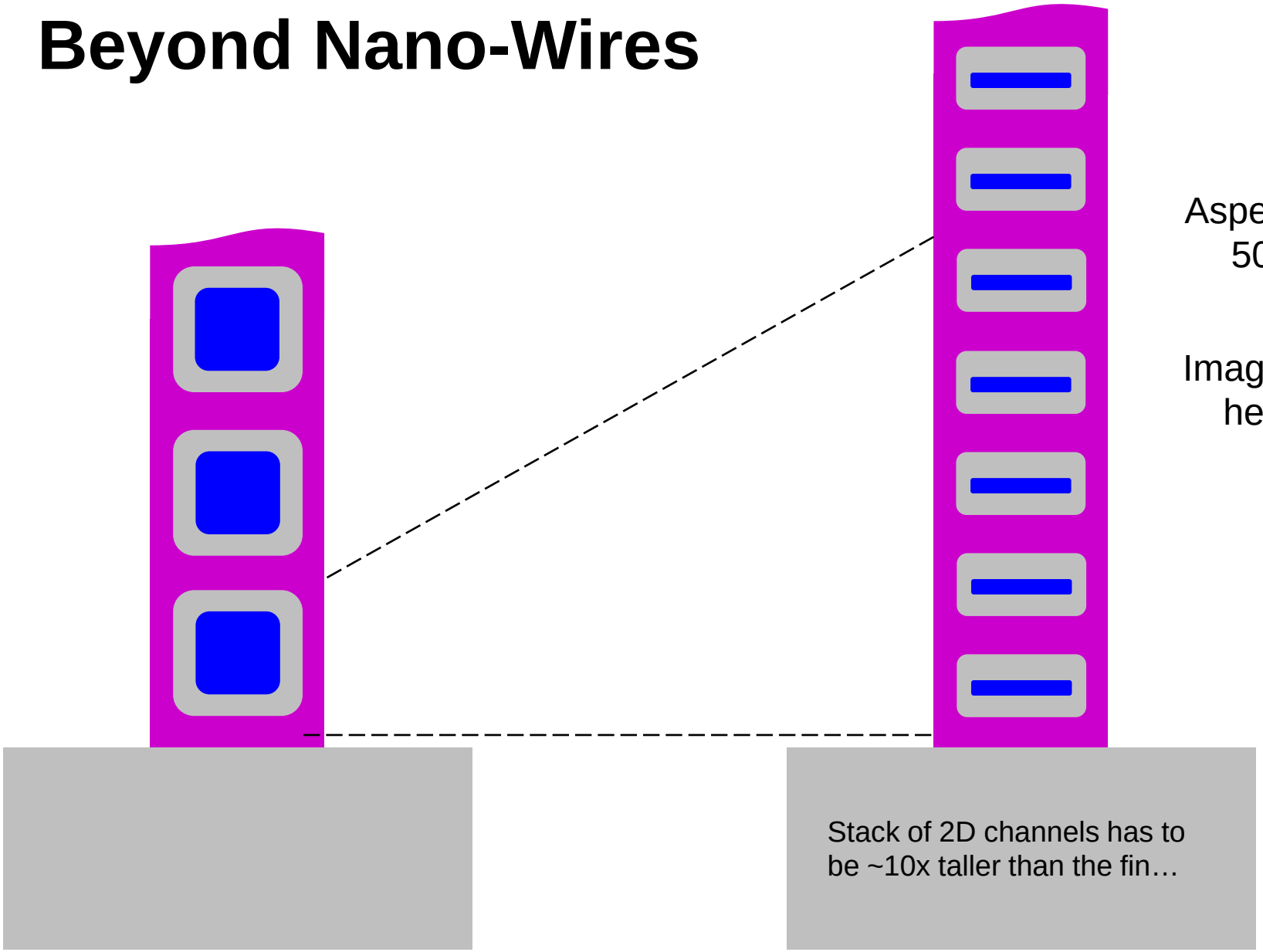
5nm node



Stack of NW has to be ~3x taller than the fin…

From Victor Moroz, Synopsys

Beyond Nano-Wires

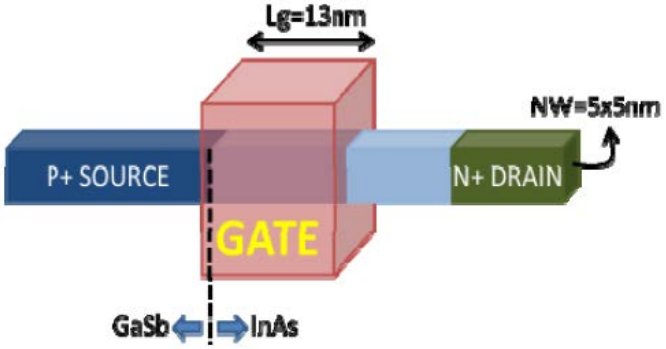


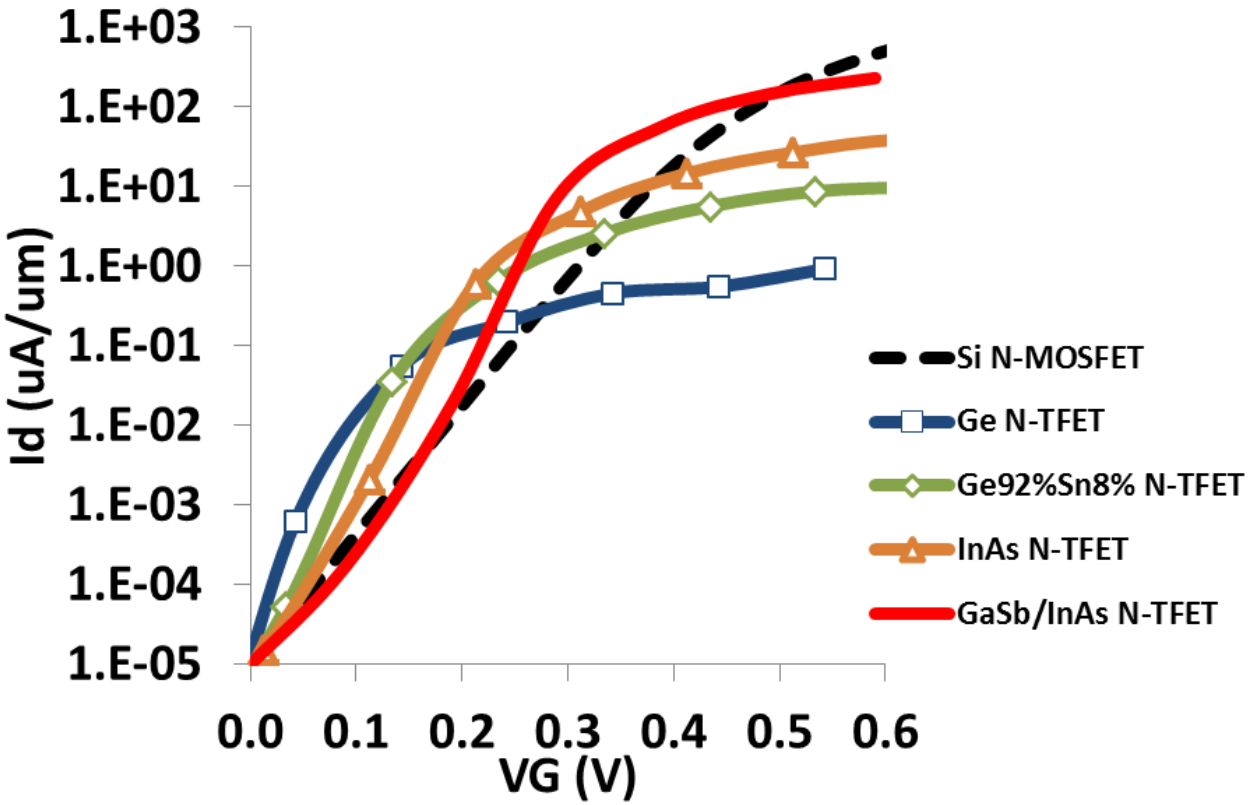
Aspect ratio: 50:1 !!!

Imaging self-heating!

From Victor Moroz, Synopsys

TFET

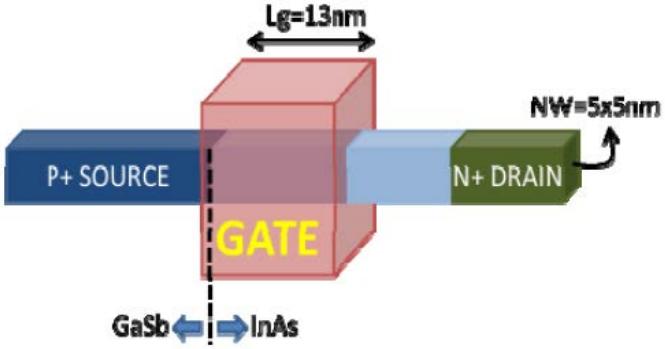


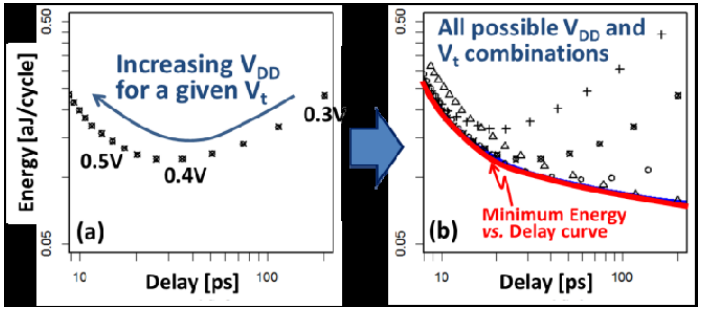


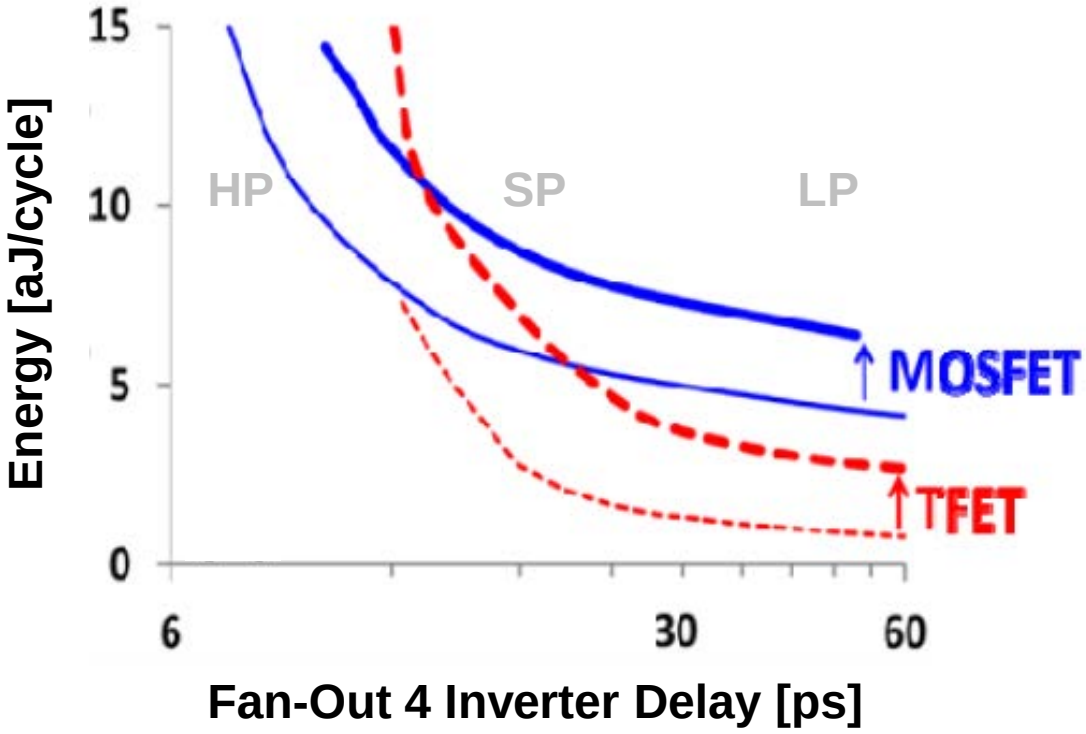
Comparison of drain current for different N-TFET materials and Si MOSFET using atomistic simulations. (Vds=0.3V, Lg=13nm and Ioff=10pA/um target)

- "Si MOSFET" NW has similar structure to the TFET shown, with n+ source and n+ drain
- Only one TFET material combination with broken gap hetero-junction gets close to the Si nano-wire
- And only for the n-type
- Nothing comparable has been found for the p-type so far

TFET







Power-performance without (thin lines) and with (thick lines) device variations is shown for 10% logic activity

- Surprizingly, TFET variability is comparable to the MOSFET's
- For both, variabilities are dominated by the WF due to the bad assumption of metal grains not shrinking between now and 2018
- The MOSFET beats TFET at HP
- They are comparable @SP
- The TFET is better @LP

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Summary

- 14/16nm on track, and 10nm is under development
- FinFETs are scalable to 7nm node, maybe beyond
- Interconnect challenges tremendous @ 10nm / beyond
- Manufacturability issues abound
- Variability trend is encouraging
- Non-Si channels boost Ion, but suffer BTBT leakage
- Self-heating will get worse over time
- Nano-wires and TFET devices promise scaling to 2.5nm
- TFETs have a promise of sub- 0.4V VDD scaling
- EDA tooling / IP techniques challenges NOT trivial