

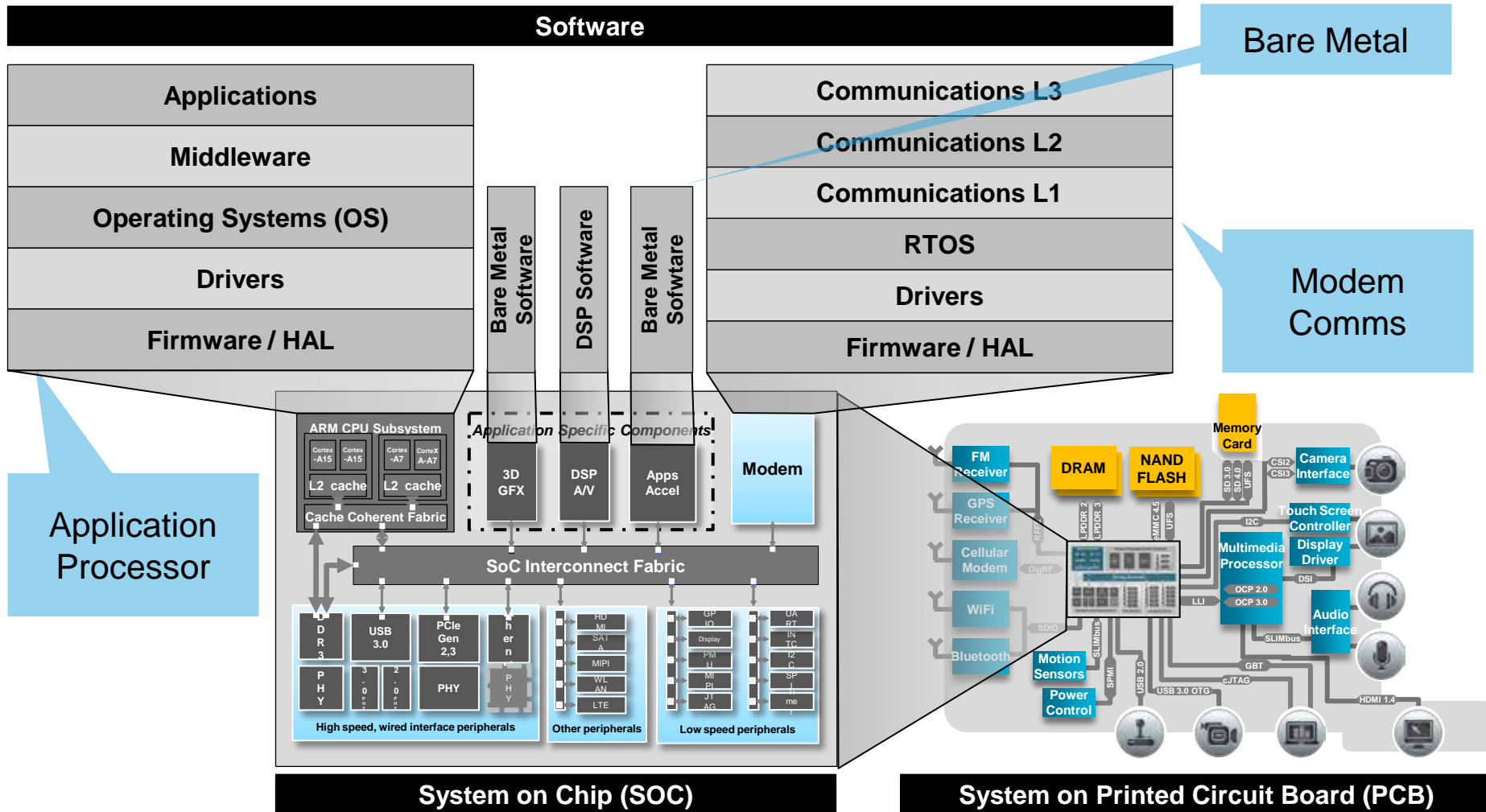


Top Semiconductor Design Flow Challenges System Level Integration

Frank Schirrmeister
EDPS
Monterey
April 17th 2014

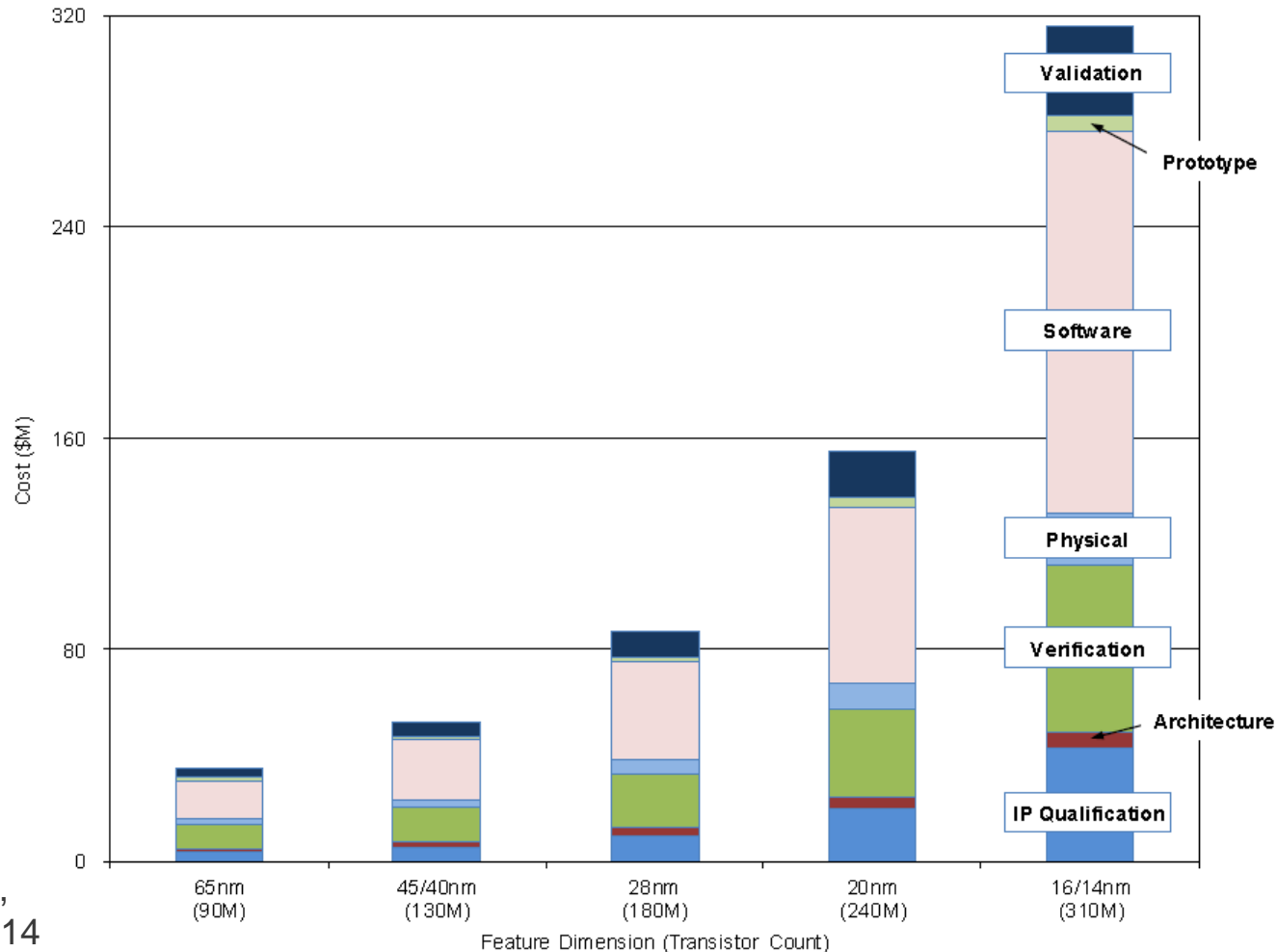
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What's in a System?



Just how complex and expensive will it get?

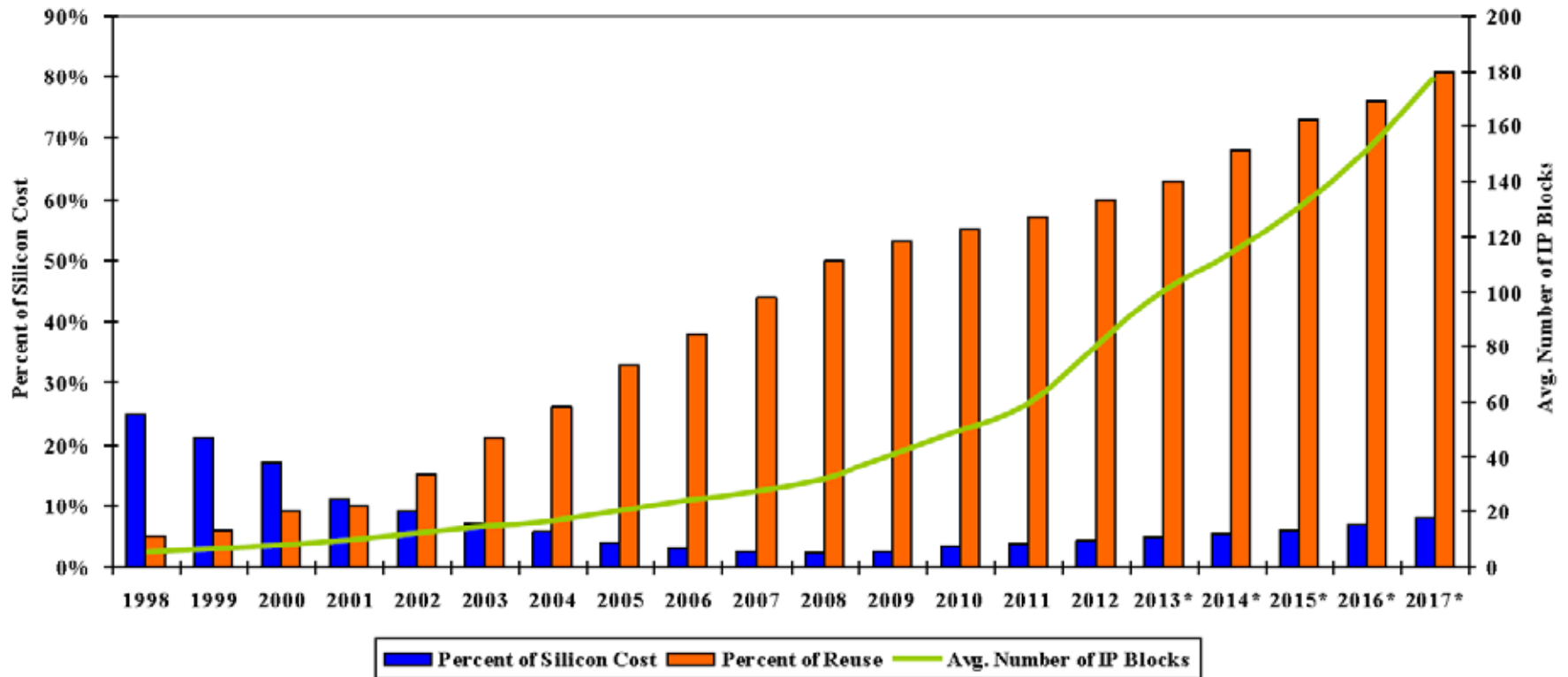
Cost of Developing New Products



Source: IBS,
February 2014

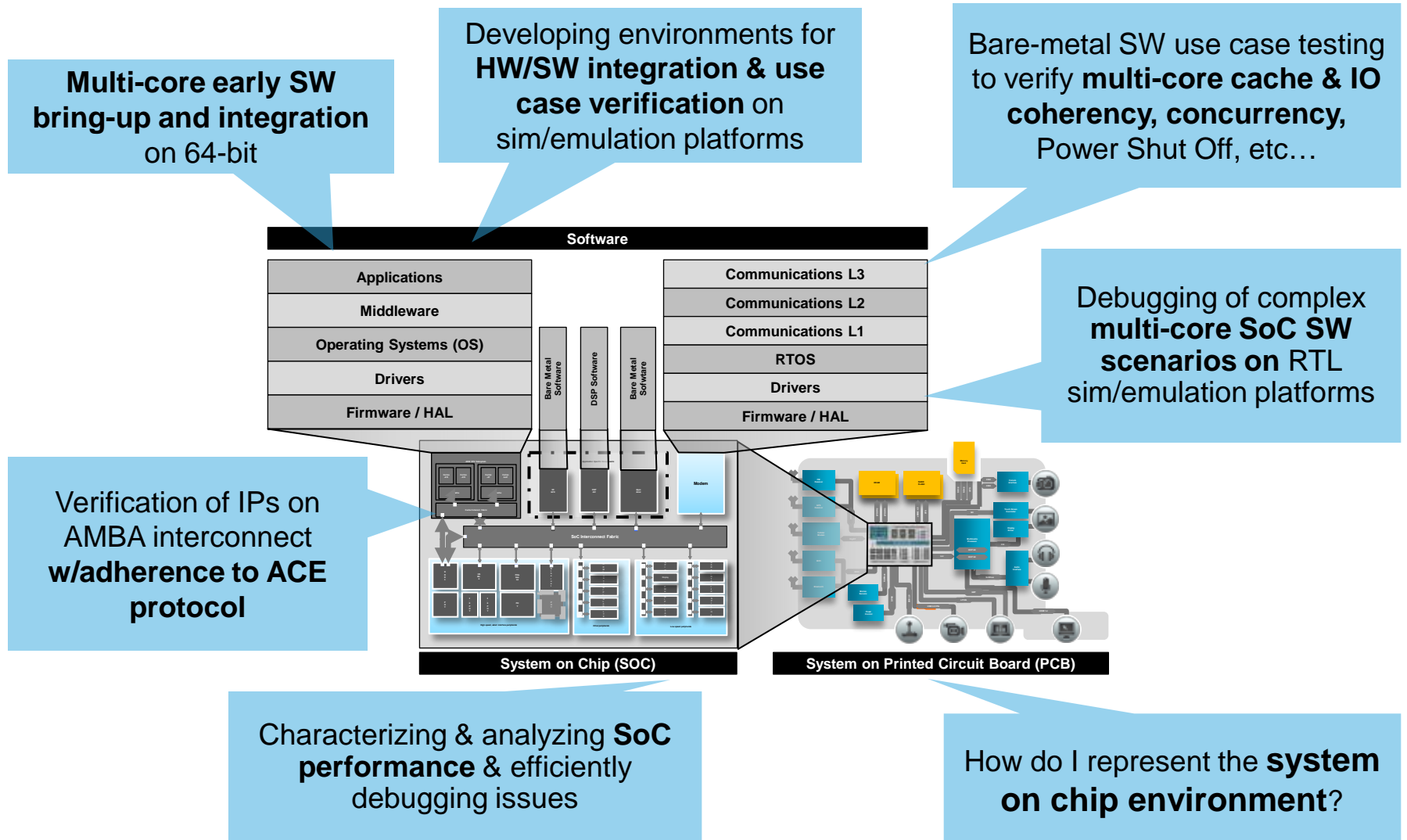
Just how complex and expensive will it get?

Growth of # of SIP Blocks per Design

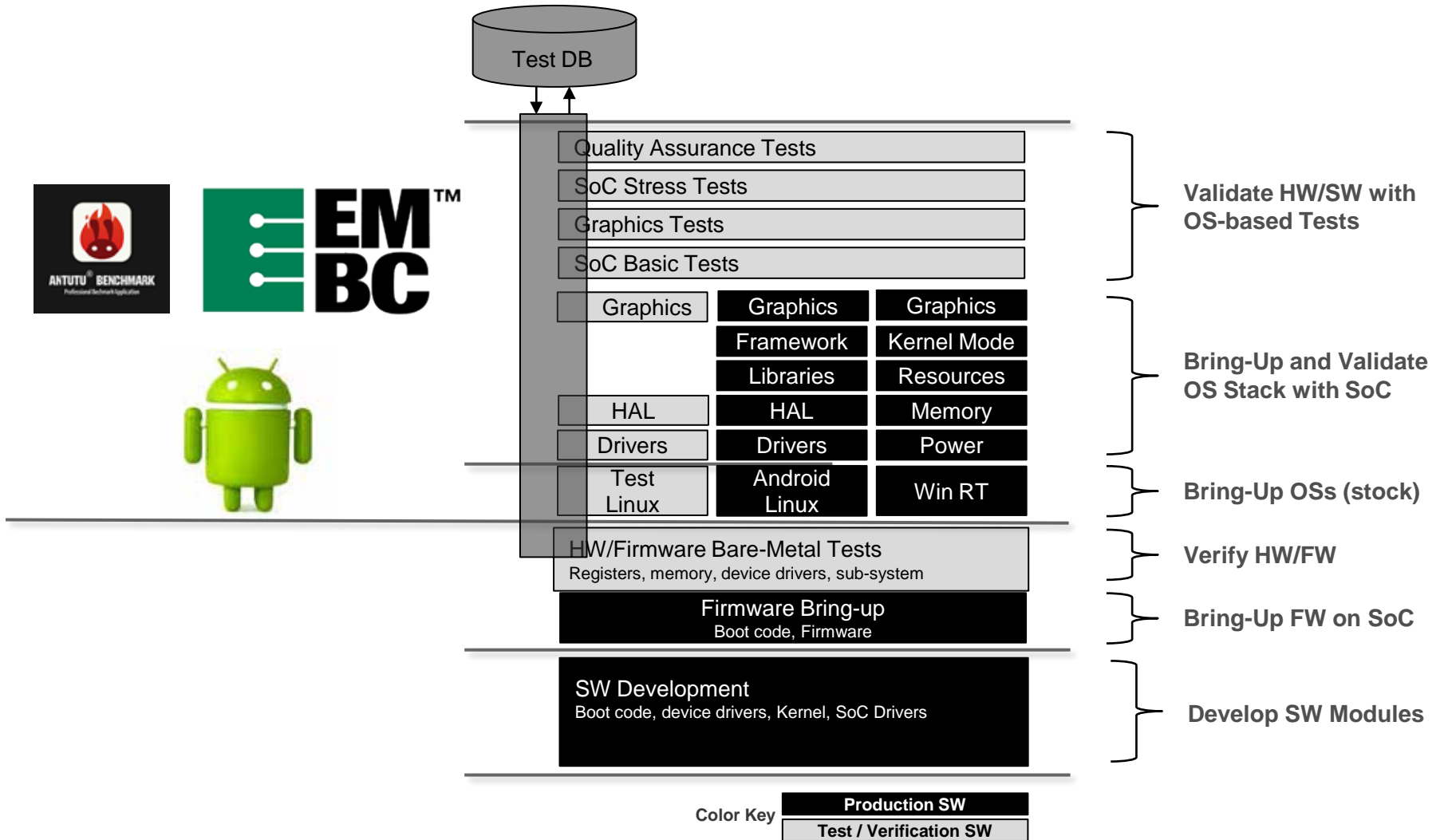


Source: Semico,
October 2013

Integrating at the System & Software Level

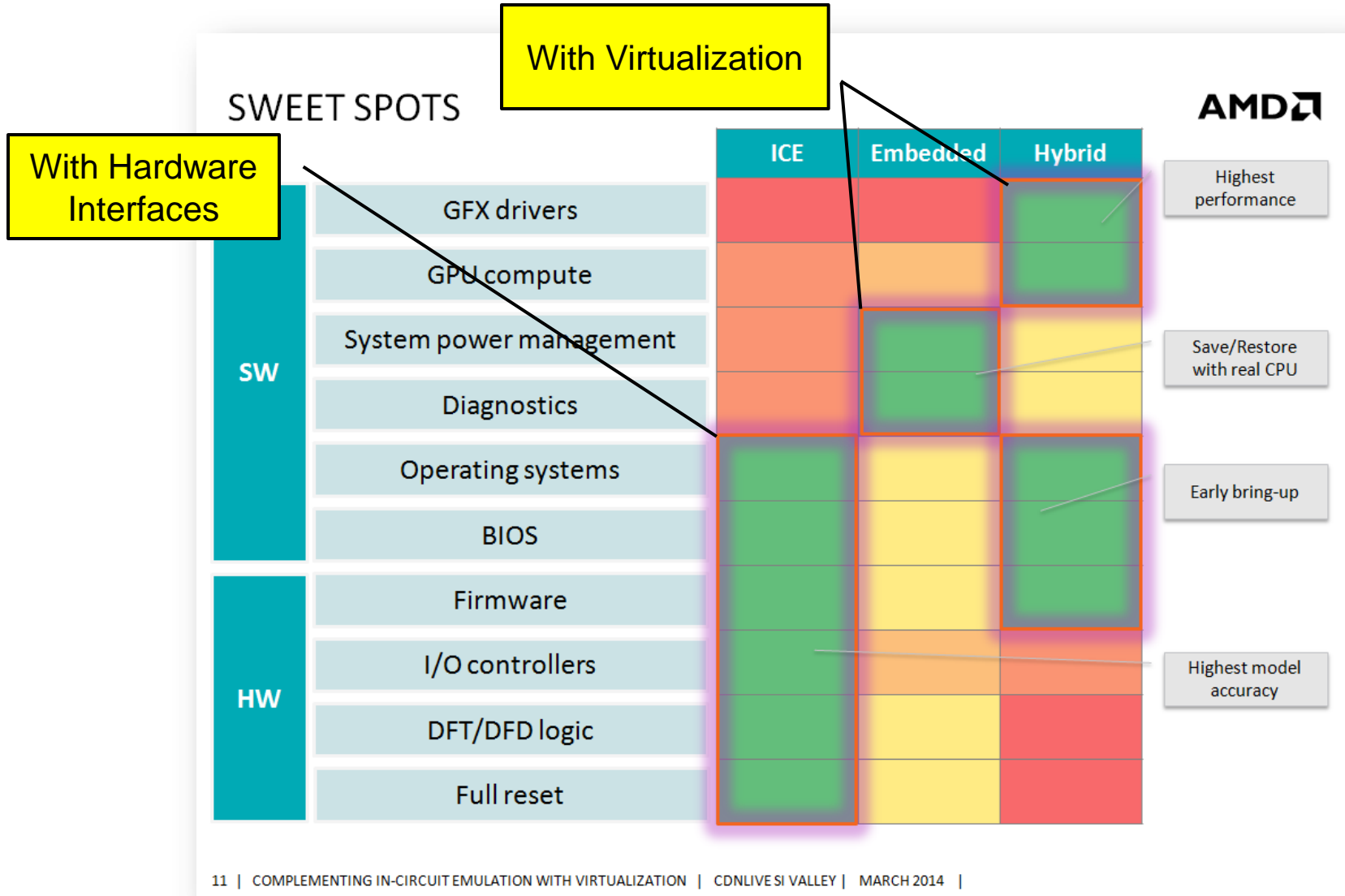


Software Based Testing and Benchmarking



Example System Integration Scenarios

Hardware Interfaces & Virtualization are complementary



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Hardware Interfaces & Virtualization are complementary

Performance

Virtualization

1. Migrate VIP-based verification to SoC & system-level on an acceleration platform
2. Validate HW/SW behavior early in development cycle by linking RTL with virtual system
3. Provide an acceleratable soft-model of a peripheral on the bus – such as a disk-drive

Hardware Interfaces

1. Validate HW/SW system interactively with live traffic including long sequences with multiple ports and increased bandwidth
2. Interface to testers & target systems for system level validation
3. Stress test with real applications & full protocol stacks

SpeedBridges

Accelerated
VIP

Simulation
VIP

Verification IP

1. Exhaustive verification of standard interfaces
2. Facilitate constrained-random simulation with VIP-supplied stimulus
3. At SoC level, check flow of commands and data across the chip

Block / IP
Verification

Sub-system / SoC
Verification

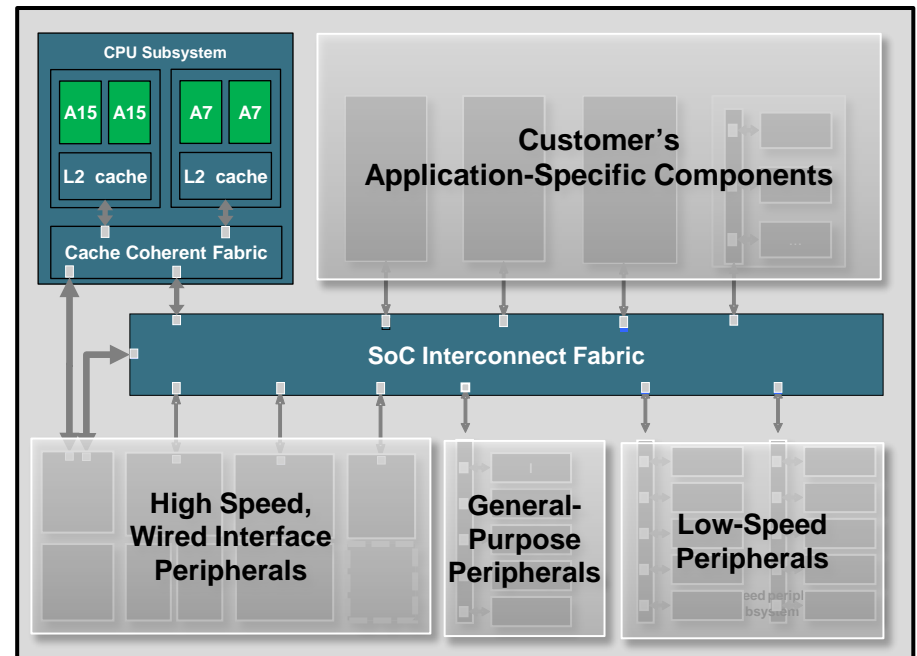
SoC level HW/FW
Integration

Full System
Validation w. App SW

Field
Prototype

System & Chip Design in 2017

- More complex designs
 - more at <90nm
 - overall less starts
- An average of 180 IP Blocks
- More than 80% re-use
- More than 60% of effort in software
- Multi-core
- Complex interconnect with cache coherency
- Software distributed across cores
- Low power issues
- Application specific issues
- High analog mixed signal content
- Hardware and virtualized system representations



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