# Top Semiconductor Design Flow Challenges System Level Integration

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April 17th 2014

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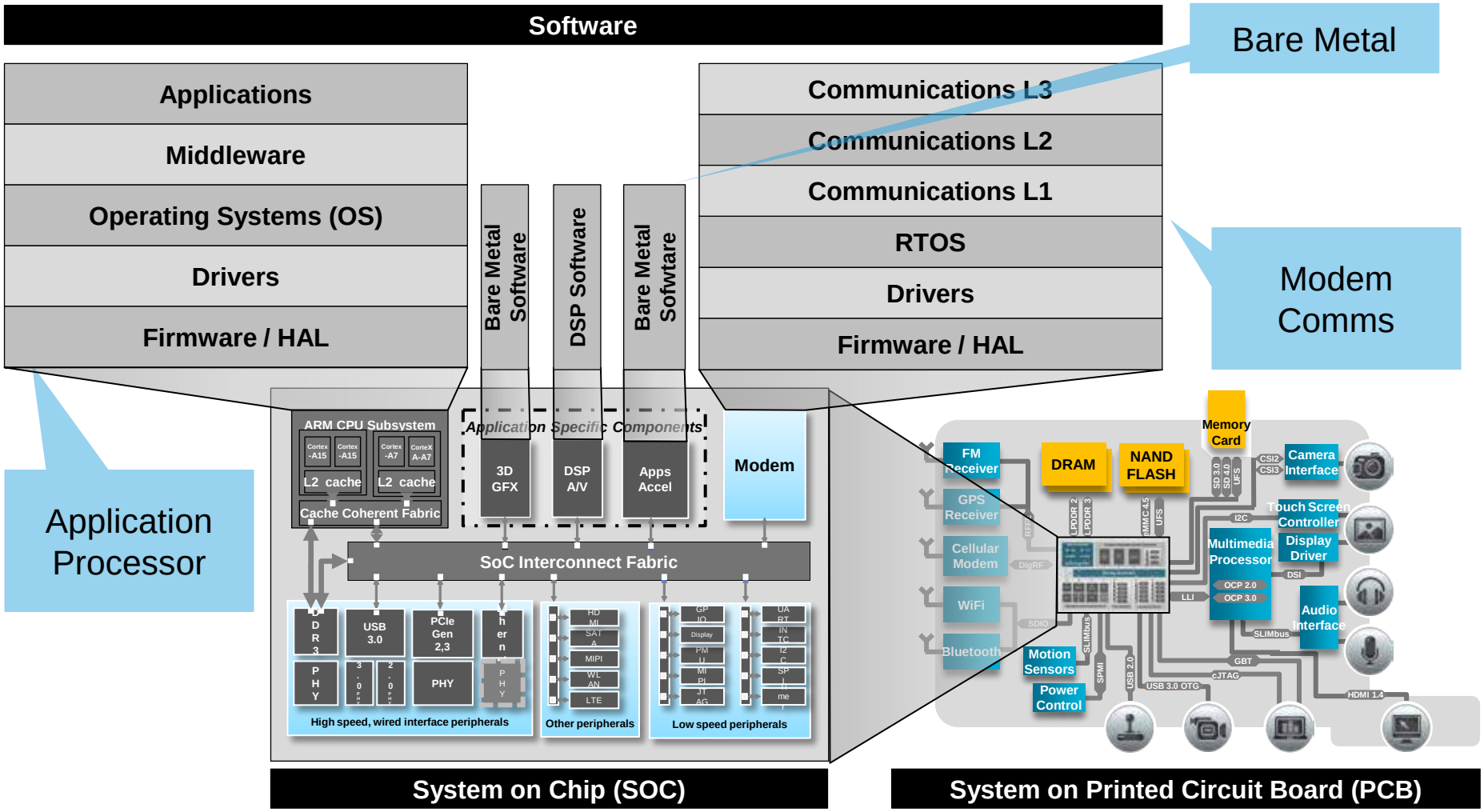
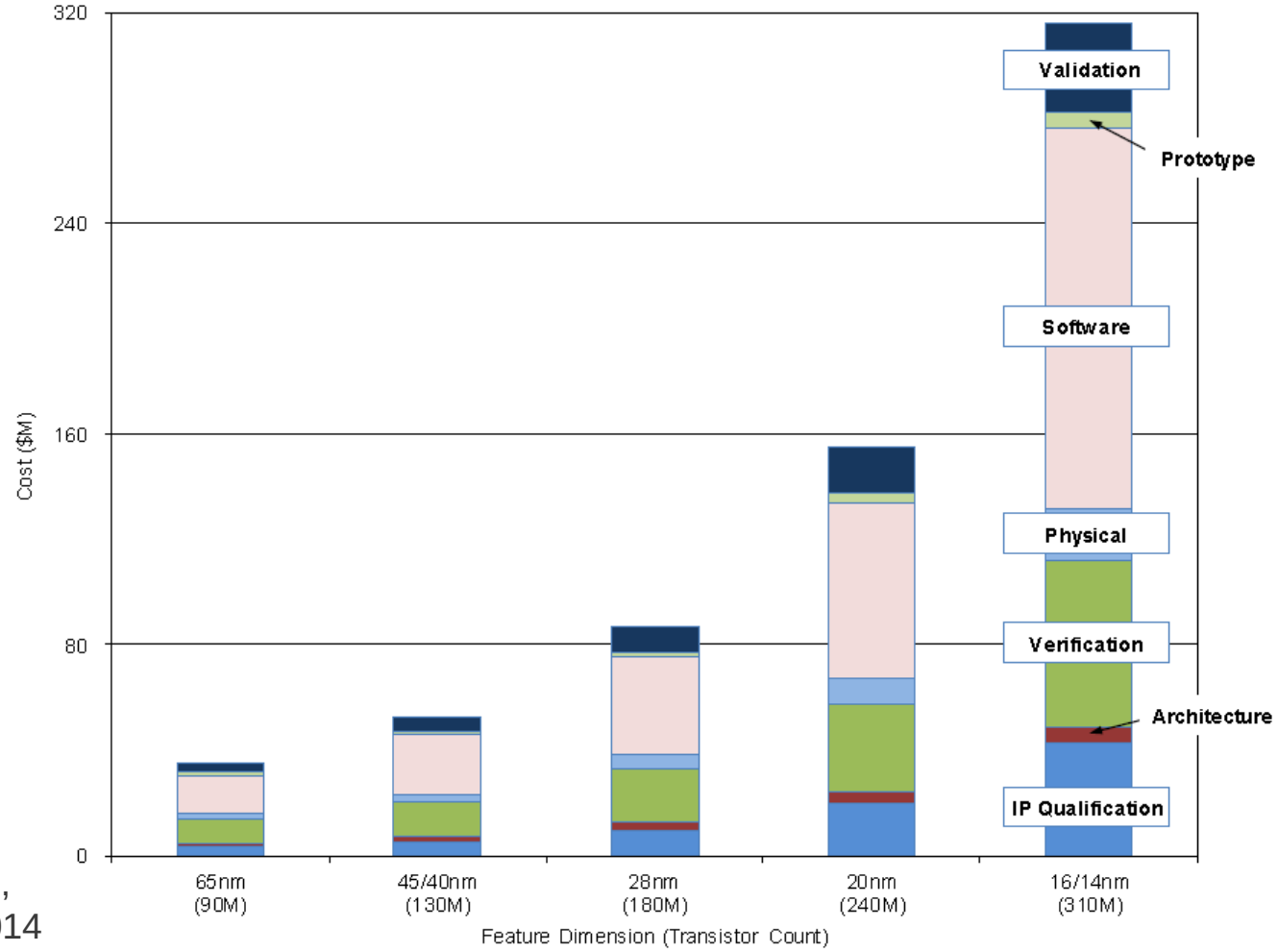
# What's in a System?

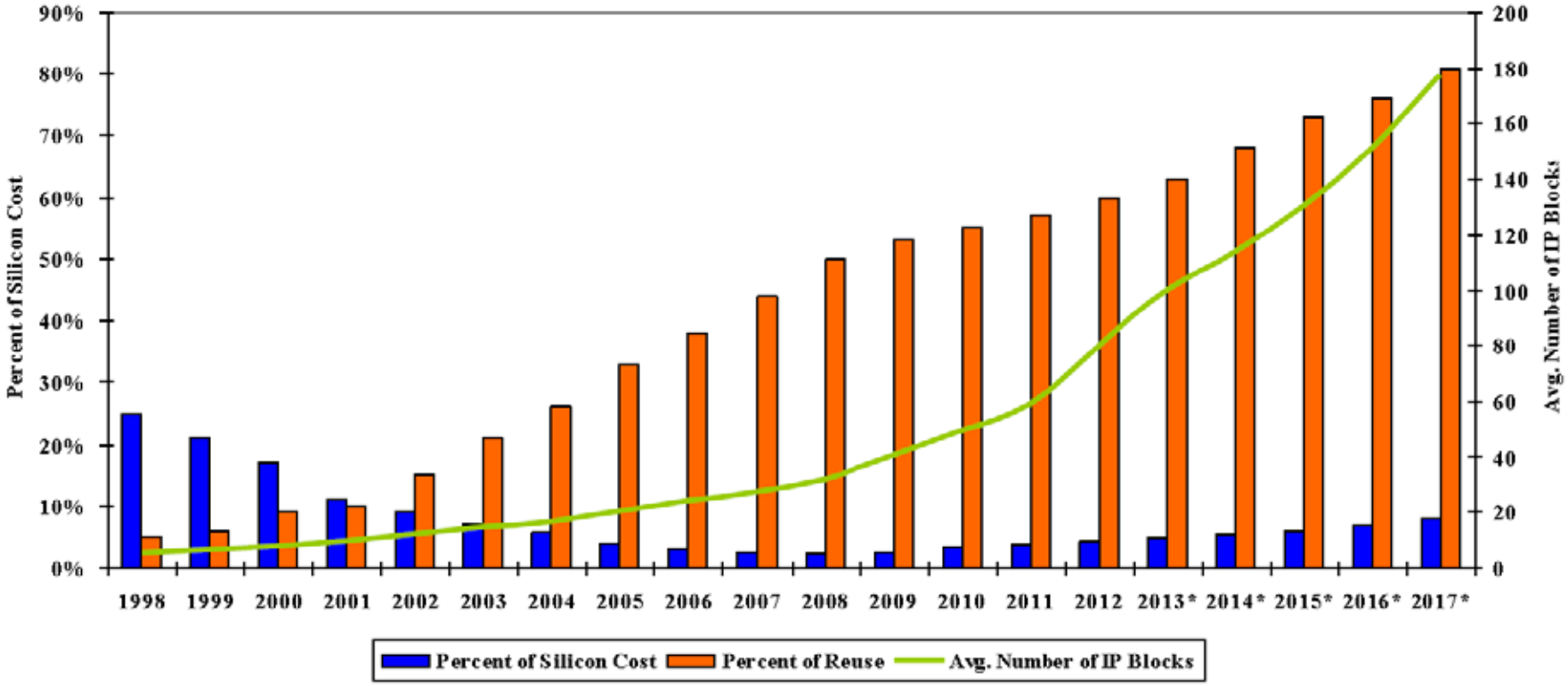


# Just how complex and expensive will it get?
## Cost of Developing New Products




Source: IBS, February 2014

# Just how complex and expensive will it get?
## Growth of # of SIP Blocks per Design




Source: Semico, October 2013



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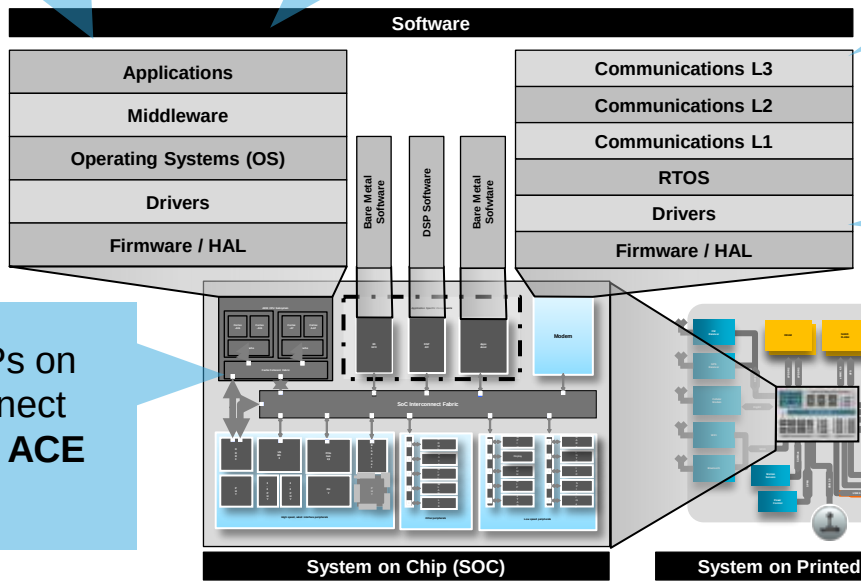
# Integrating at the System & Software Level

**Multi-core early SW bring-up and integration** on 64-bit

Developing environments for **HW/SW integration & use case verification** on sim/emulation platforms

Bare-metal SW use case testing to verify **multi-core cache & IO coherency, concurrency,** Power Shut Off, etc…



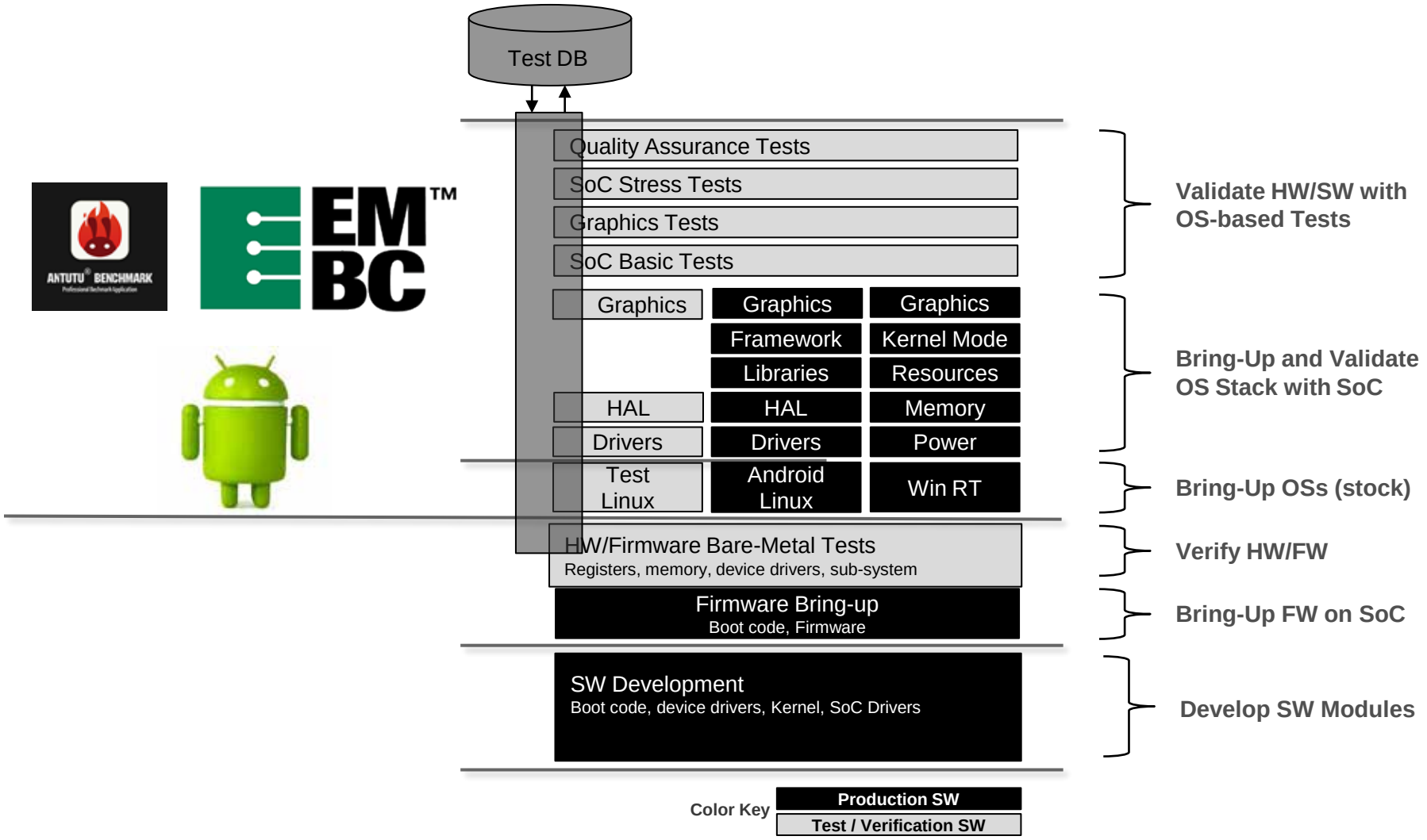

Debugging of complex **multi-core SoC SW scenarios on** RTL sim/emulation platforms

Verification of IPs on AMBA interconnect **w/adherence to ACE protocol**

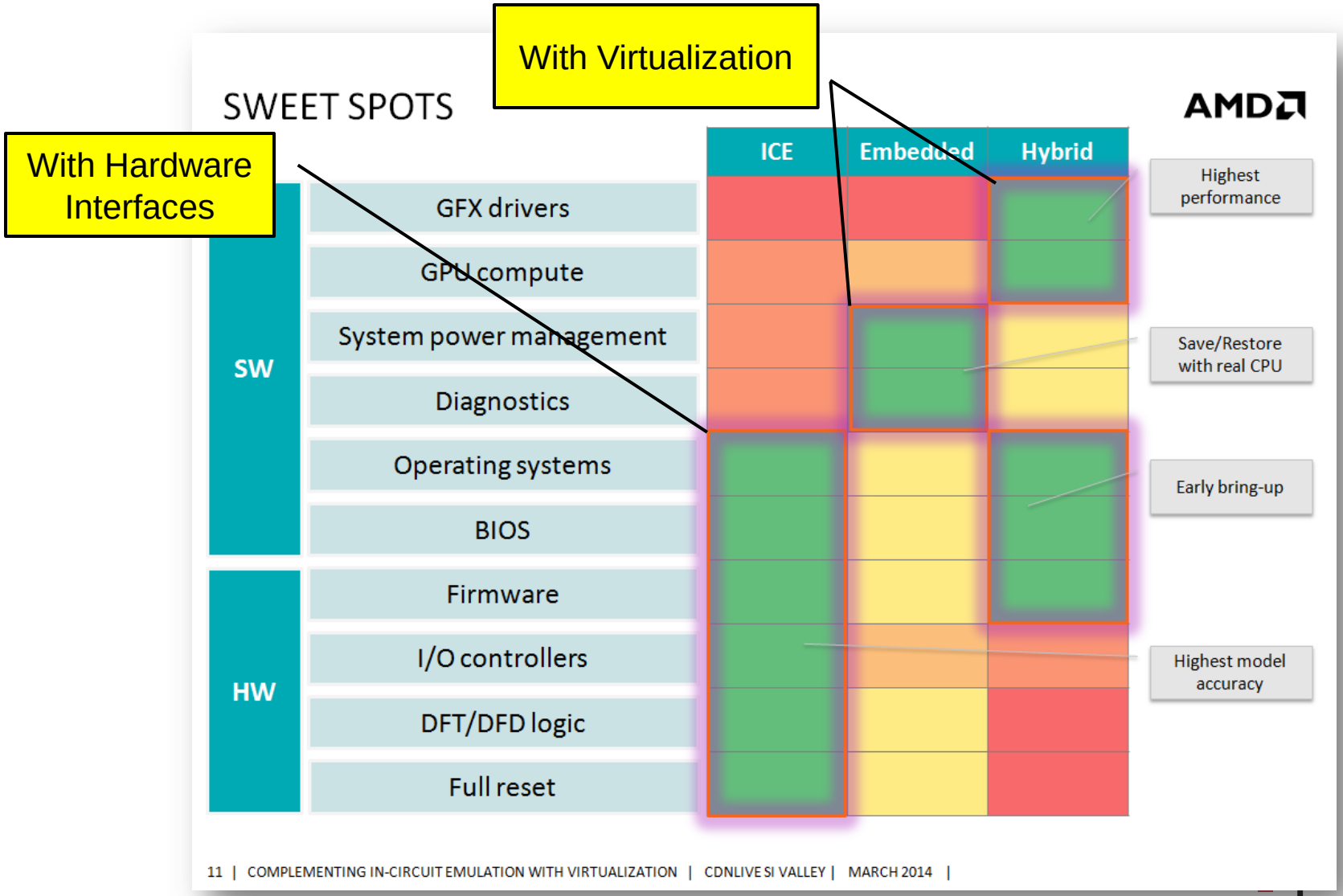
Characterizing & analyzing **SoC performance** & efficiently debugging issues

How do I represent the **system on chip environment**?

# Software Based Testing and Benchmarking



# Example System Integration Scenarios
## Hardware Interfaces & Virtualization are complementary



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# Example System Integration Scenarios
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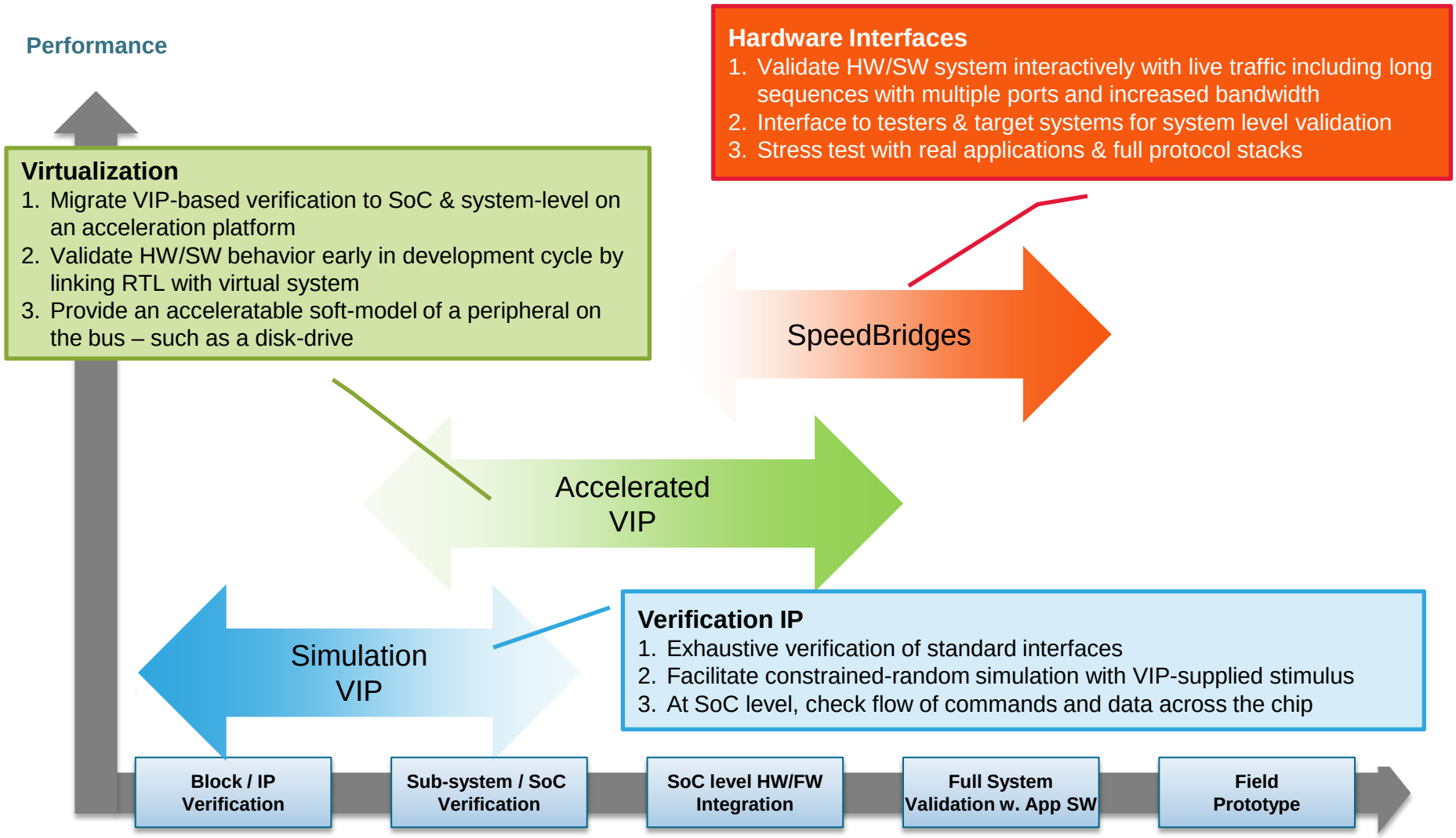




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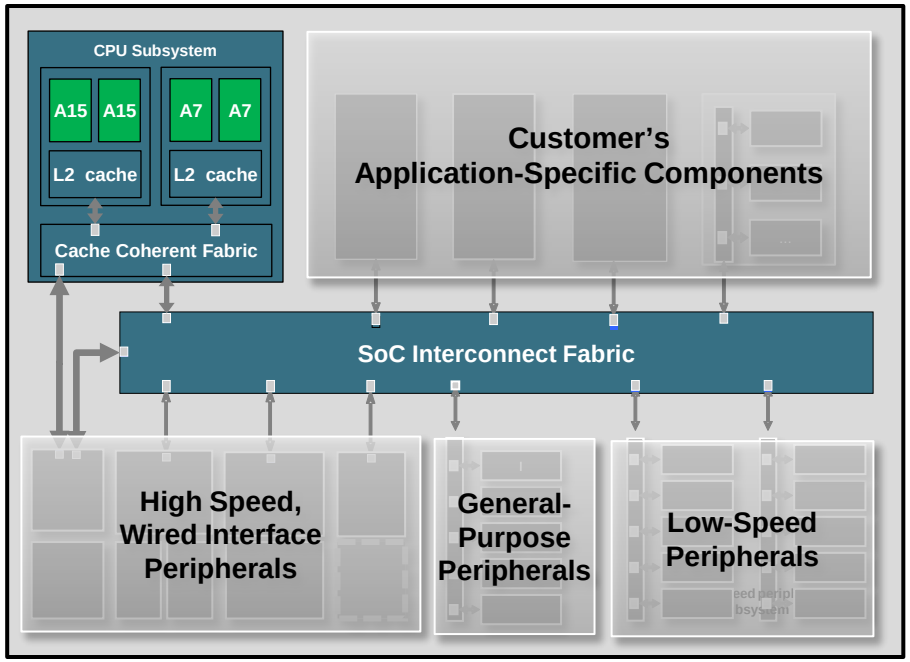
# System & Chip Design in 2017

- More complex designs
  - more at <90nm
  - overall less starts
- An average of 180 IP Blocks
- More than 80% re-use
- More than 60% of effort in software
- Multi-core
- Complex interconnect with cache coherency
- Software distributed across cores
- Low power issues
- Application specific issues
- High analog mixed signal content
- Hardware and virtualized system representations



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