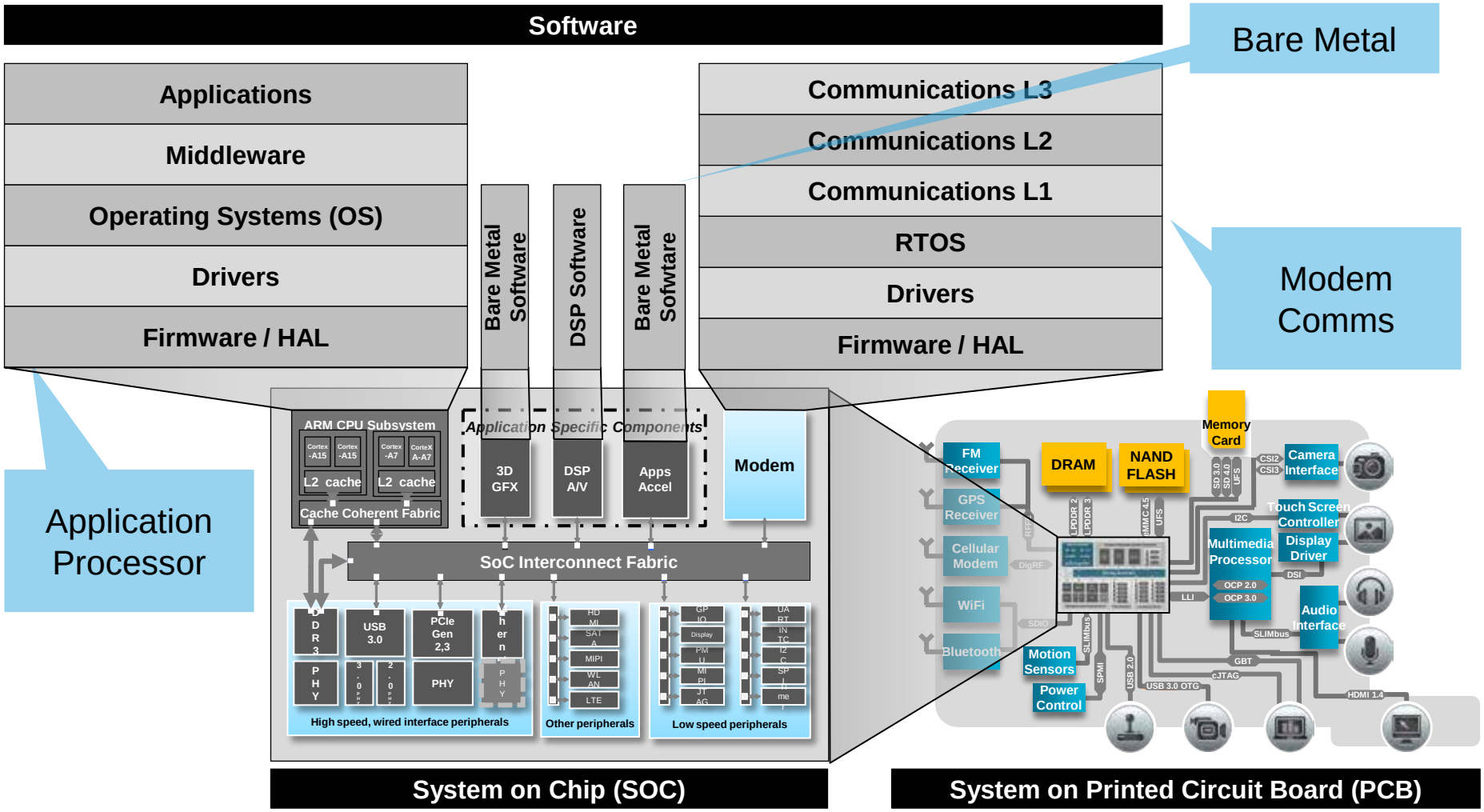
Combining TLM & RTL Techniques:
A Silver Bullet for Pre-Silicon HW/SW Integration

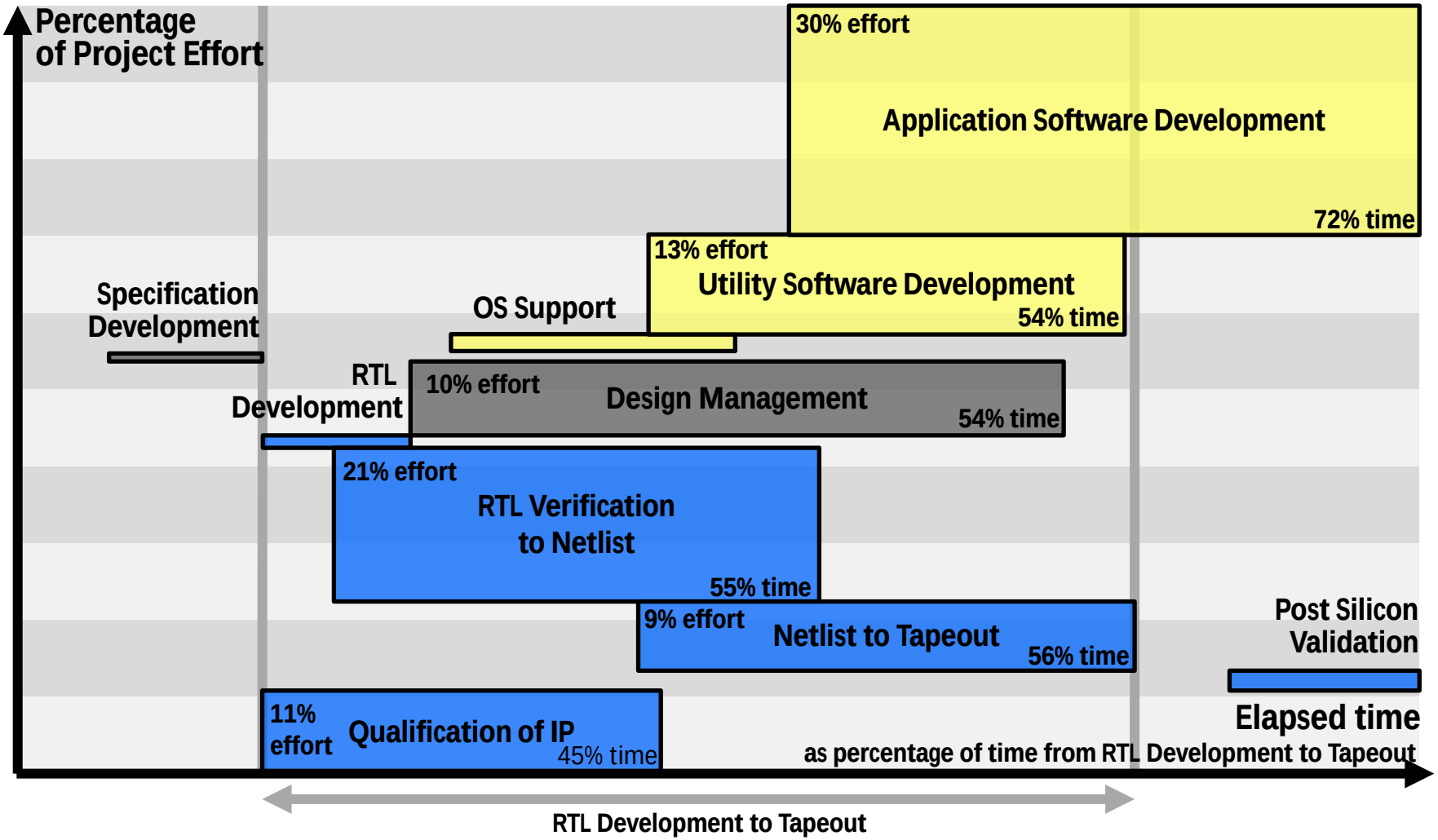
Frank Schirrmeister
EDPS
Monterey
April 17th 2014

cadence®

Hardware/Software Systems



A project schedule, reconstructed



Market Dynamics

Where do HW and SW meet, actually?

?

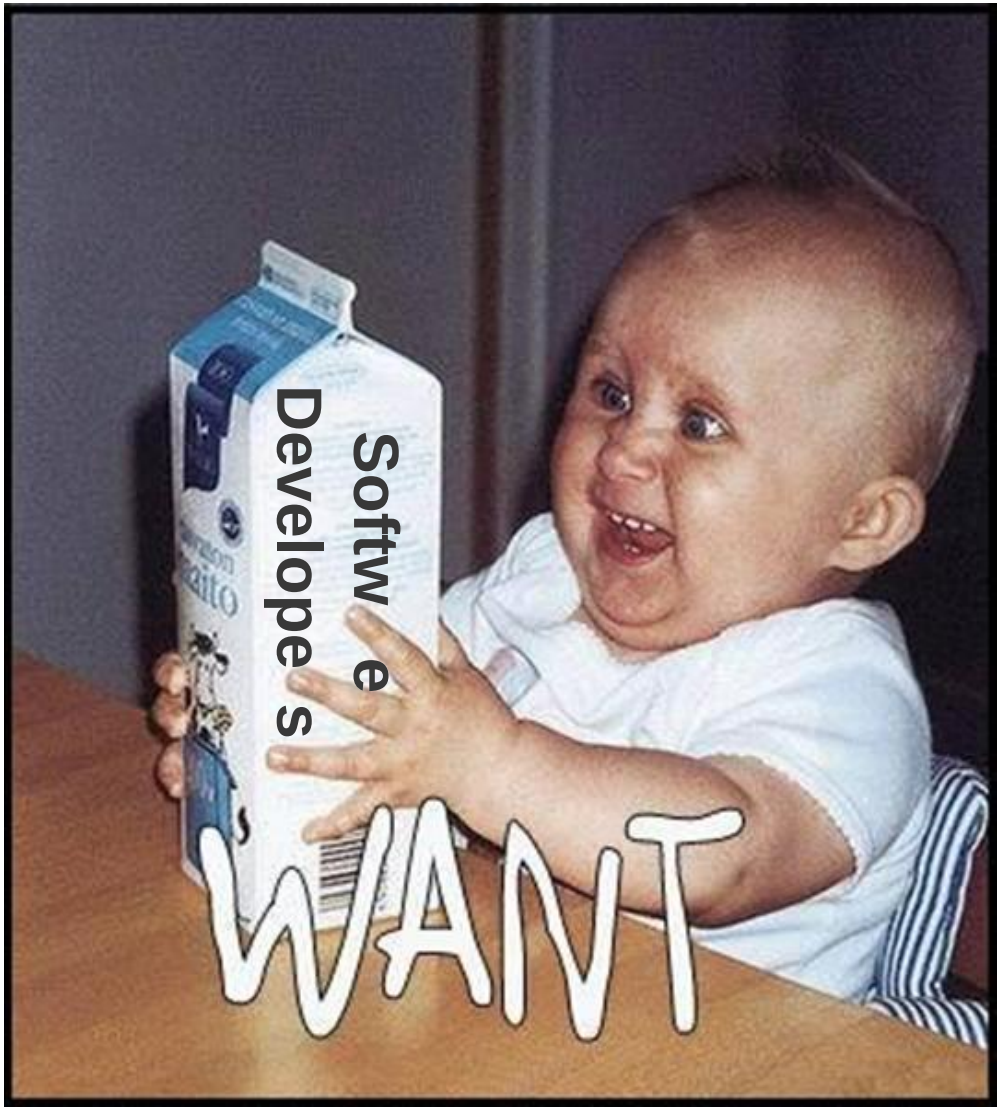
	eSW Tools	Content
Apps	Embedded Software Development Tools Assembler, Compiler, Linker, Debugger, …	***For end users, large # of developers***
Middleware		***Often licensed with OS***
Run/Real-Time Kernel		***Licensed IP;*** *sometimes developed in-House*
Drivers		***Expected to come with hardware IP****, otherwise be developed internally*

ü

	EDA
System Hardware	
PCB	***Board Integration: PCB Tool Sets***
System Design	***Software Enablement:*** *Emulation, Acceleration, FPGA based prototyping and Virtual Prototyping*
System on Chip	***Verification****: Verification IP, Silicon Virtual Prototype*
Sub-system	***Design:*** *Design IP, Interconnect, Analysis Tools*

cadence

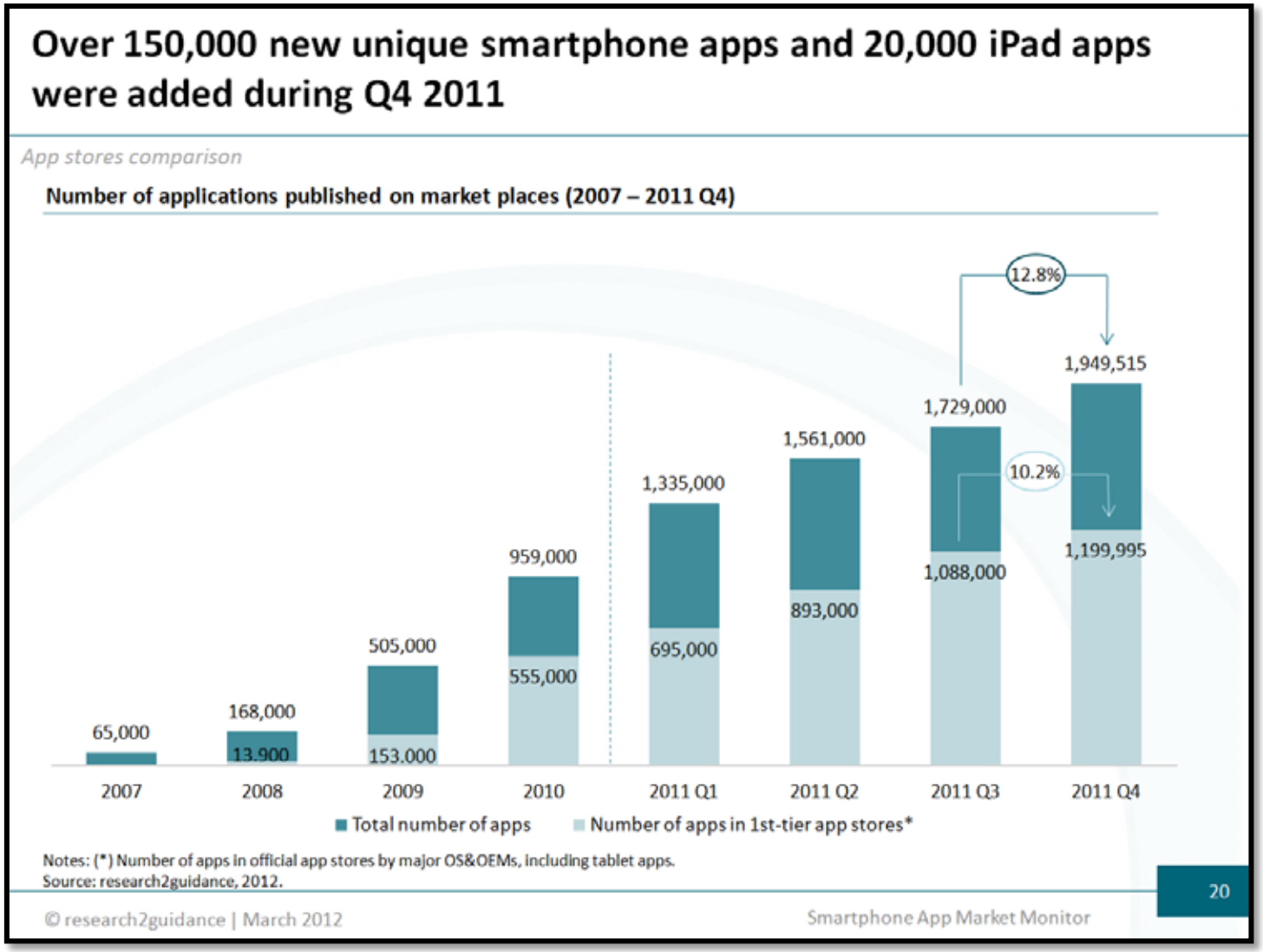
Why is EDA so excited?



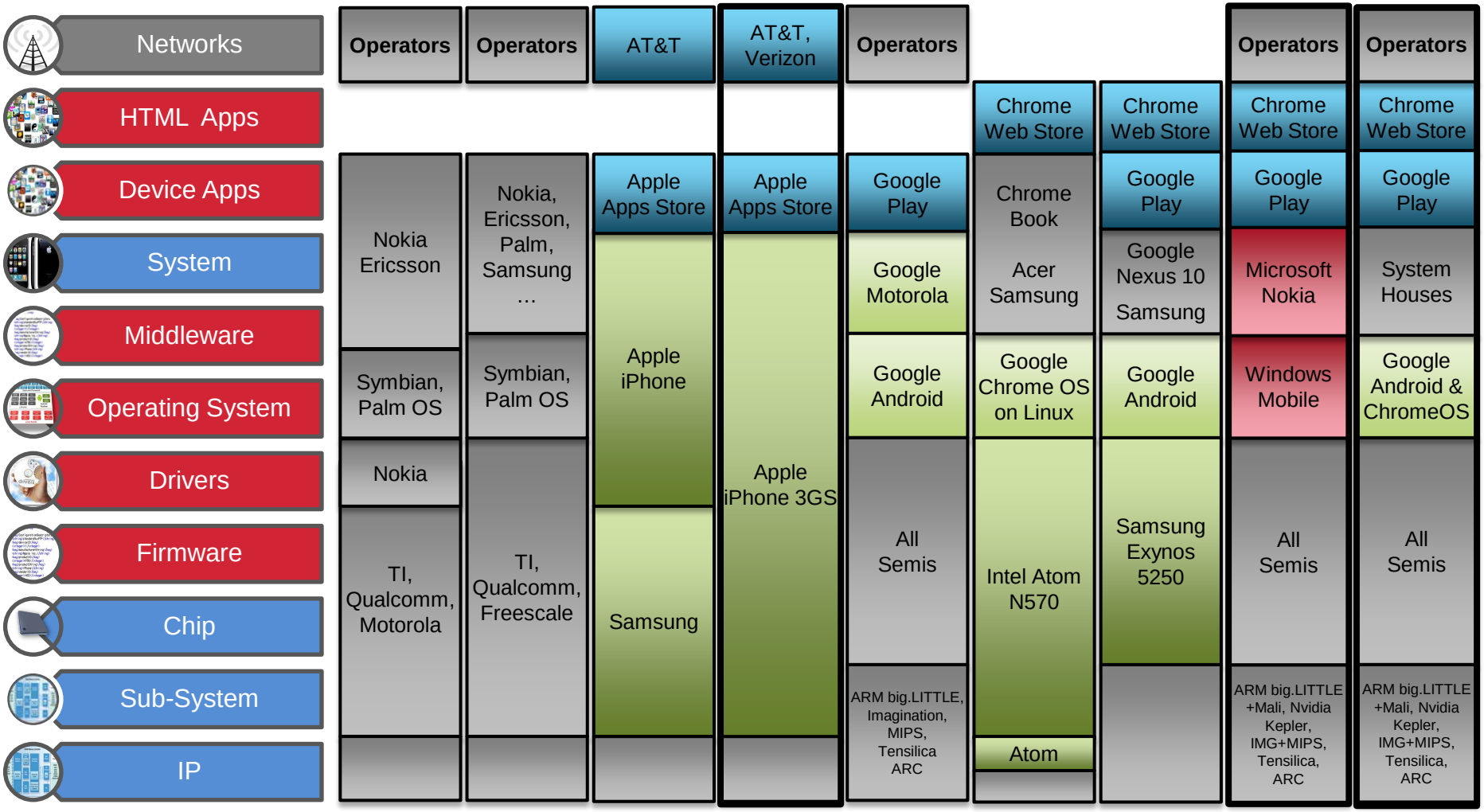
Source: http://bitsandpieces1.blogspot.in/

Why is EDA so excited?

Source: research2guidance

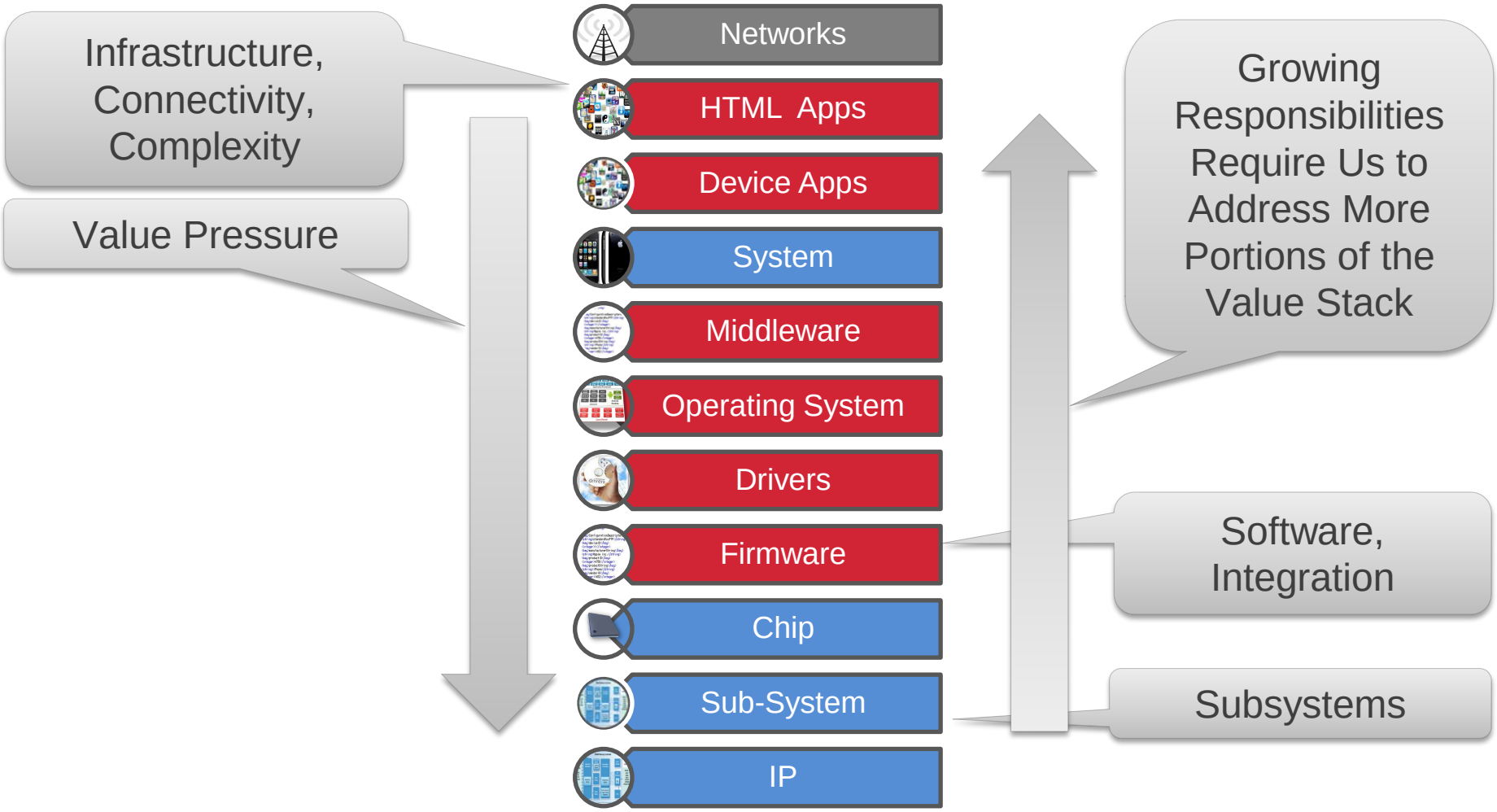


Who is doing what in a Changing World?



cadence®

Who Develops What? New Industry Dynamics!

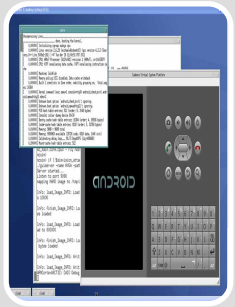
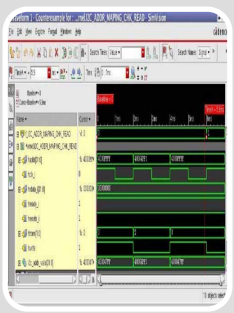


cadence

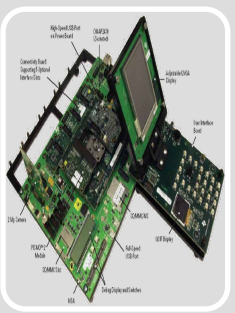
Development Engines

There is no “One Size Fits All”

Verification and Software platforms need to interoperate





SDK OS Simulation

- Highest speed
- Earliest in the flow
- Ignore hardware

Virtual Platform

- Almost at speed
- Less accurate (or slower)
- Before RTL
- Great to debug (but less detail)
- Easy replication

Formal Analysis

- Non-scalable
- Exhaustive
- Early RTL
- Great for IP
- No SW execution

HDL Simulation

- KHz range
- Accurate
- Excellent HW debug
- Broadly available
- Mixed-abstractions
- Limited SW execution

Acceleration Emulation

- MHz Range
- RTL accurate
- After RTL is available
- Good to debug with full detail
- Expensive to replicate

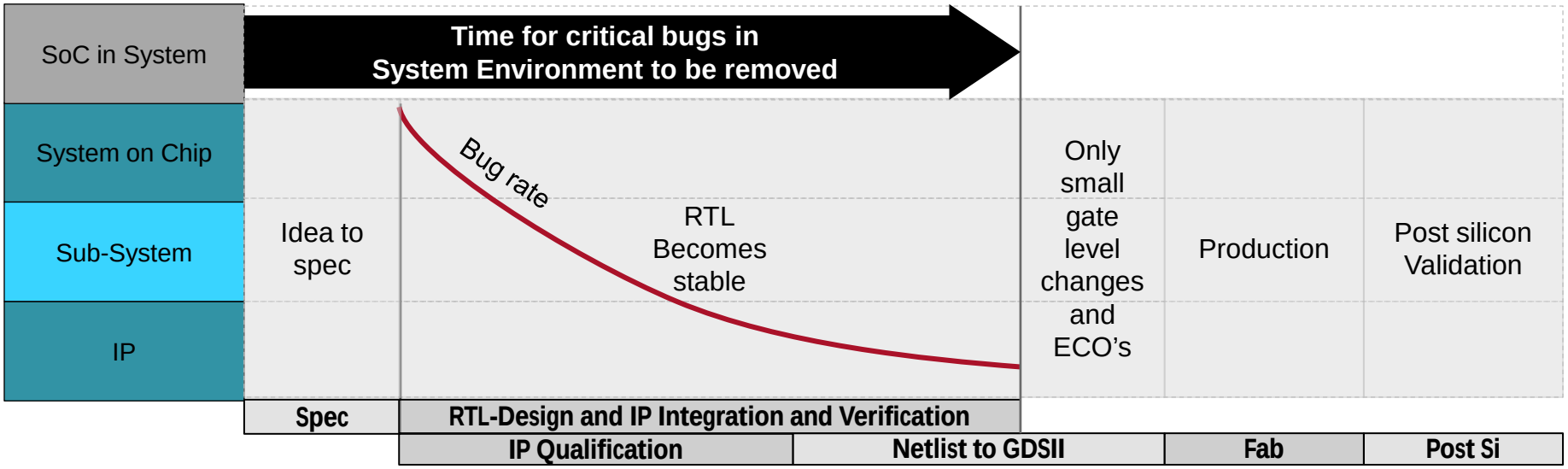
FPGA Prototype

- 10’s of MHz
- RTL accurate
- After stable RTL is available
- OK to debug
- More expensive than software to replicate

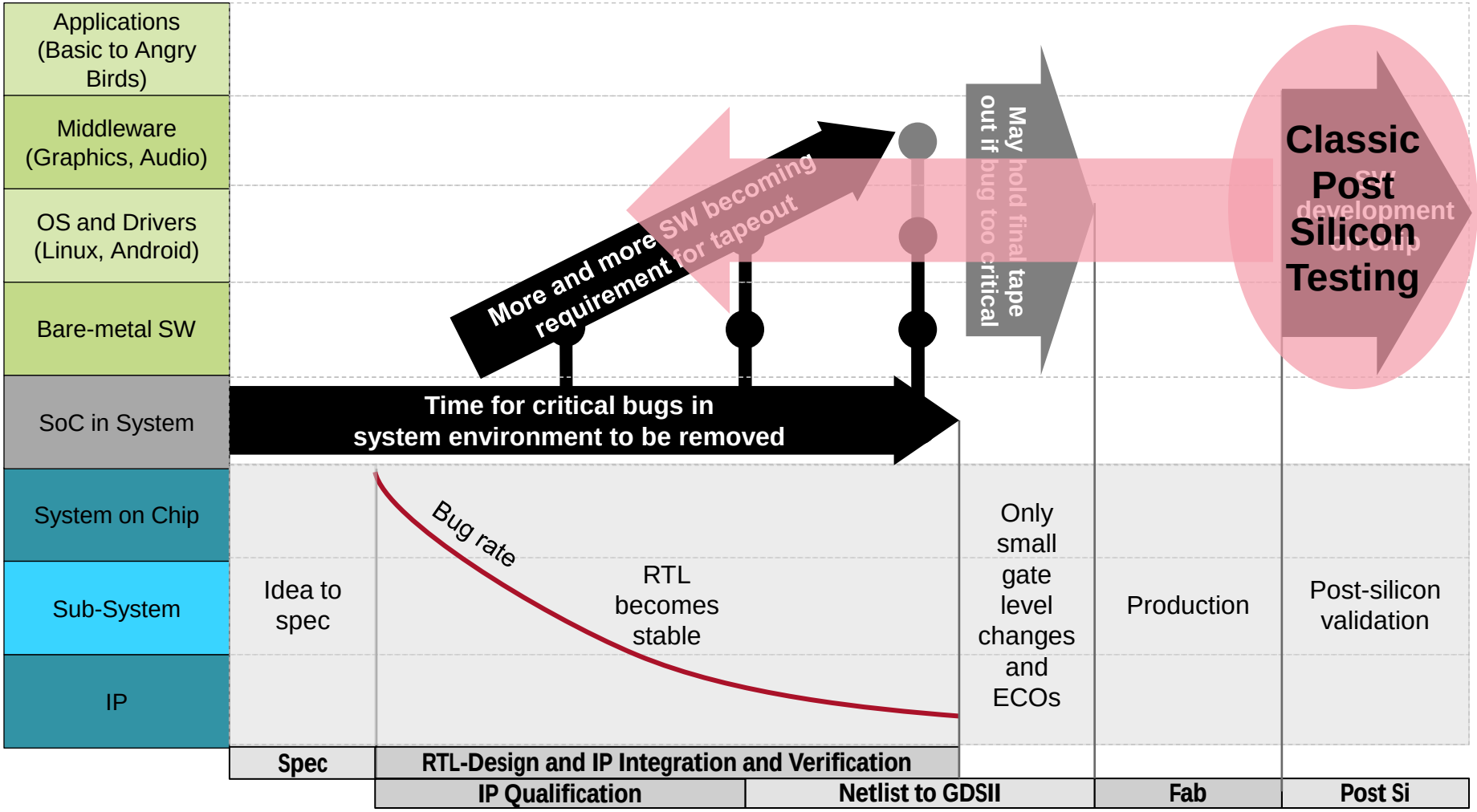
Prototyping Board

- Real time speed
- Fully accurate
- Post Silicon
- Difficult to debug
- Sometimes hard to replicate

Timing is Critical for HW/SW Development

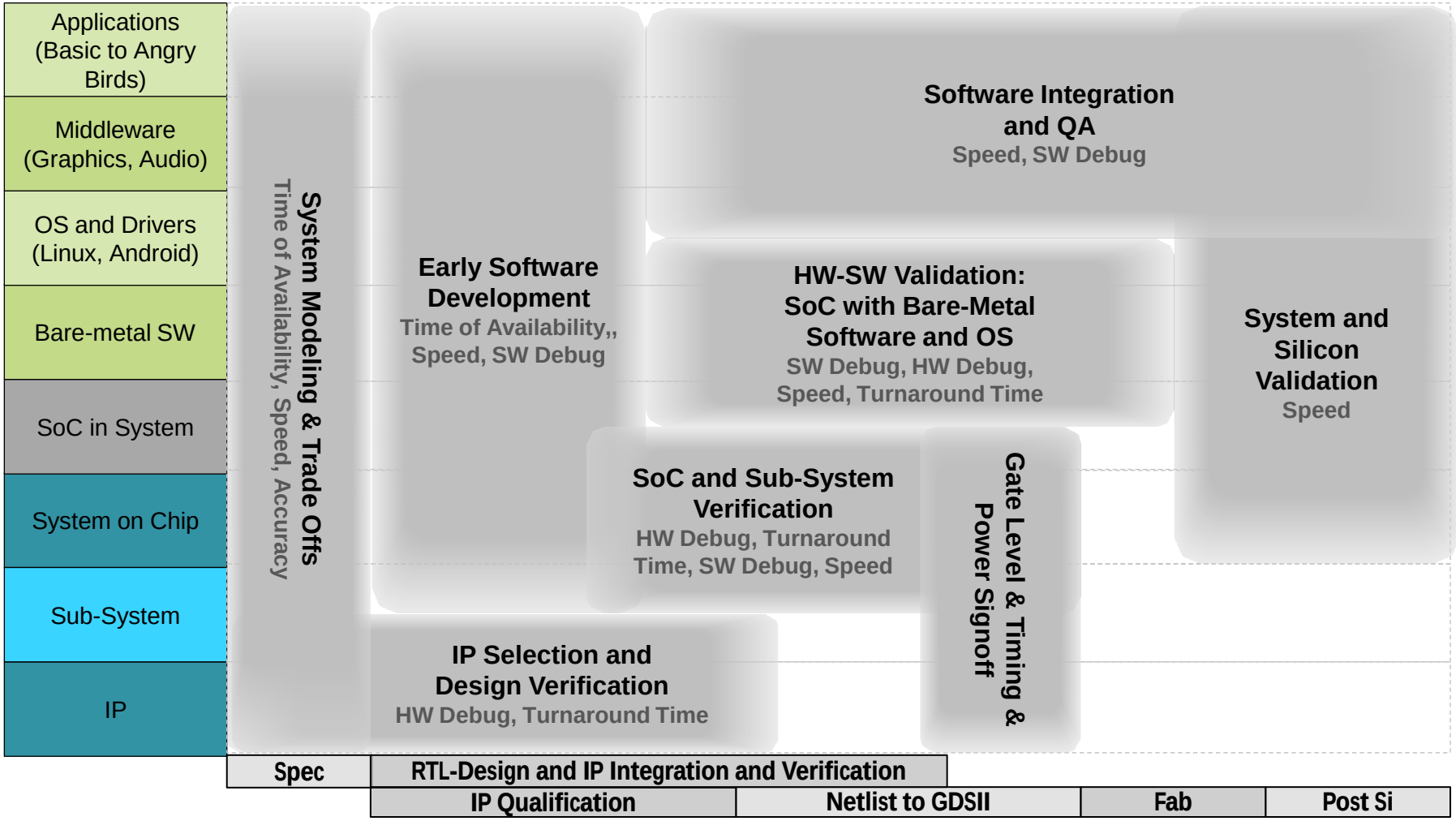


Timing is Critical for Modeling for Software

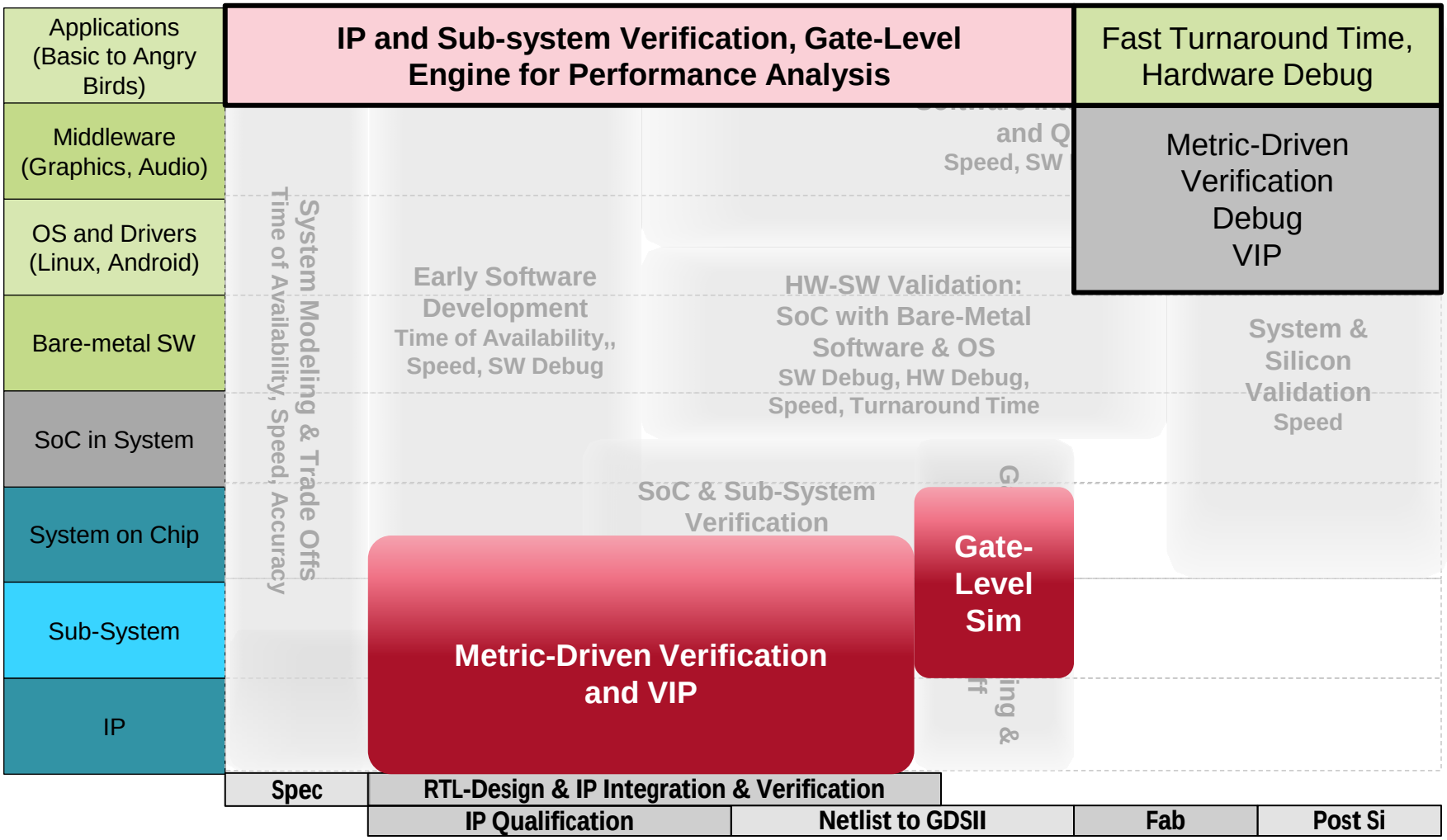


cadence

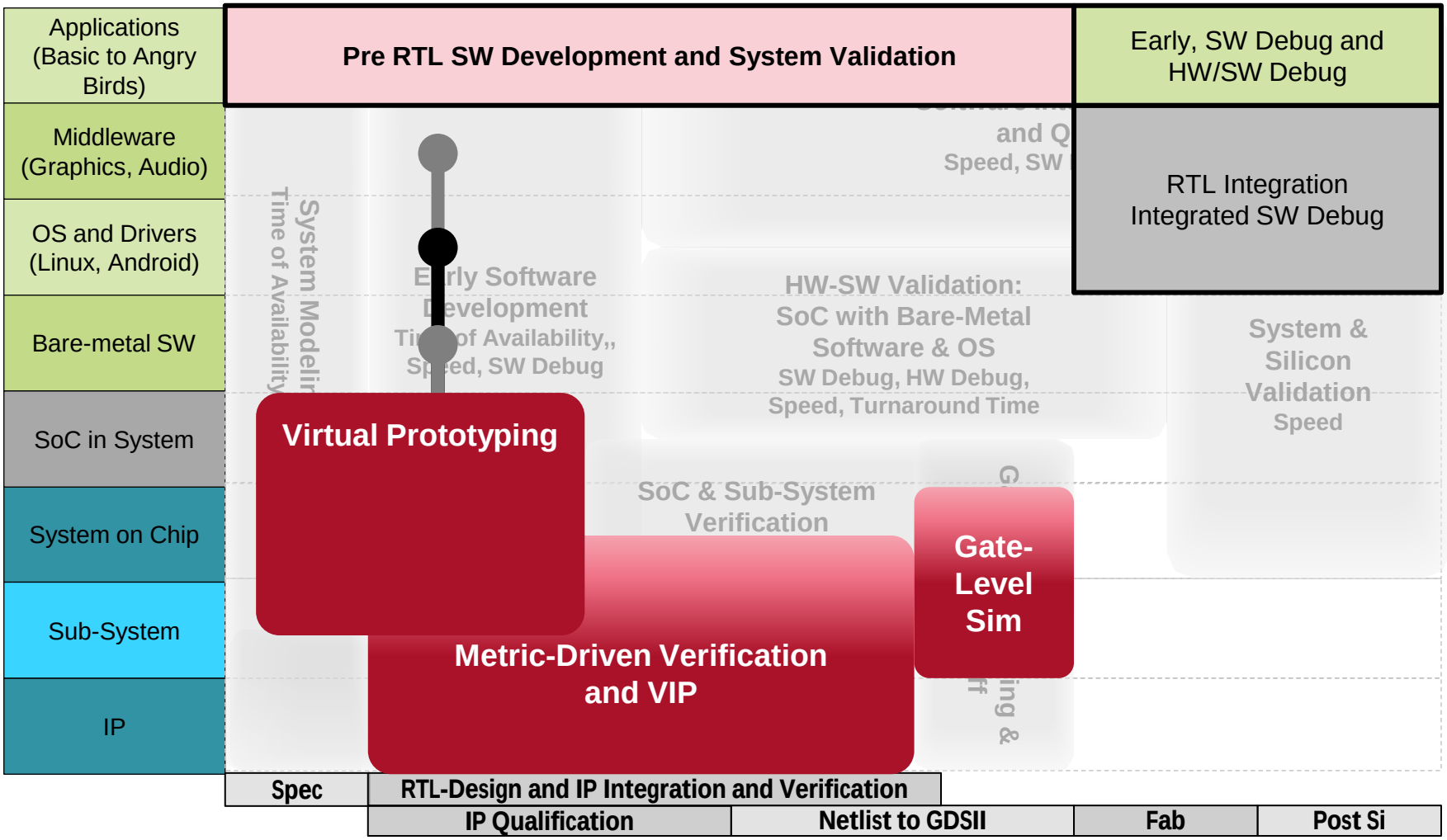
User Tasks and Requirements



RTL Simulation

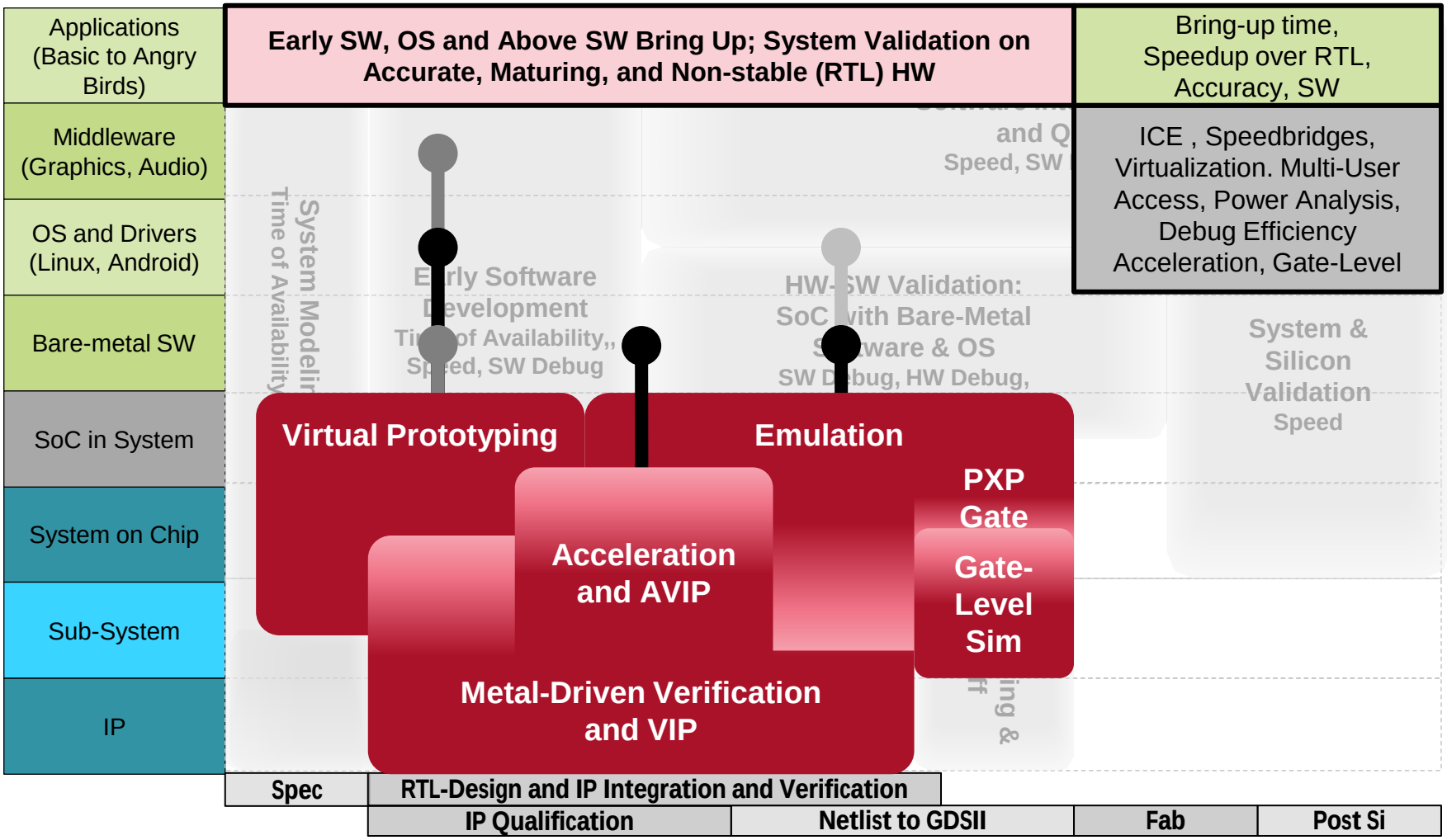


Virtual Prototyping



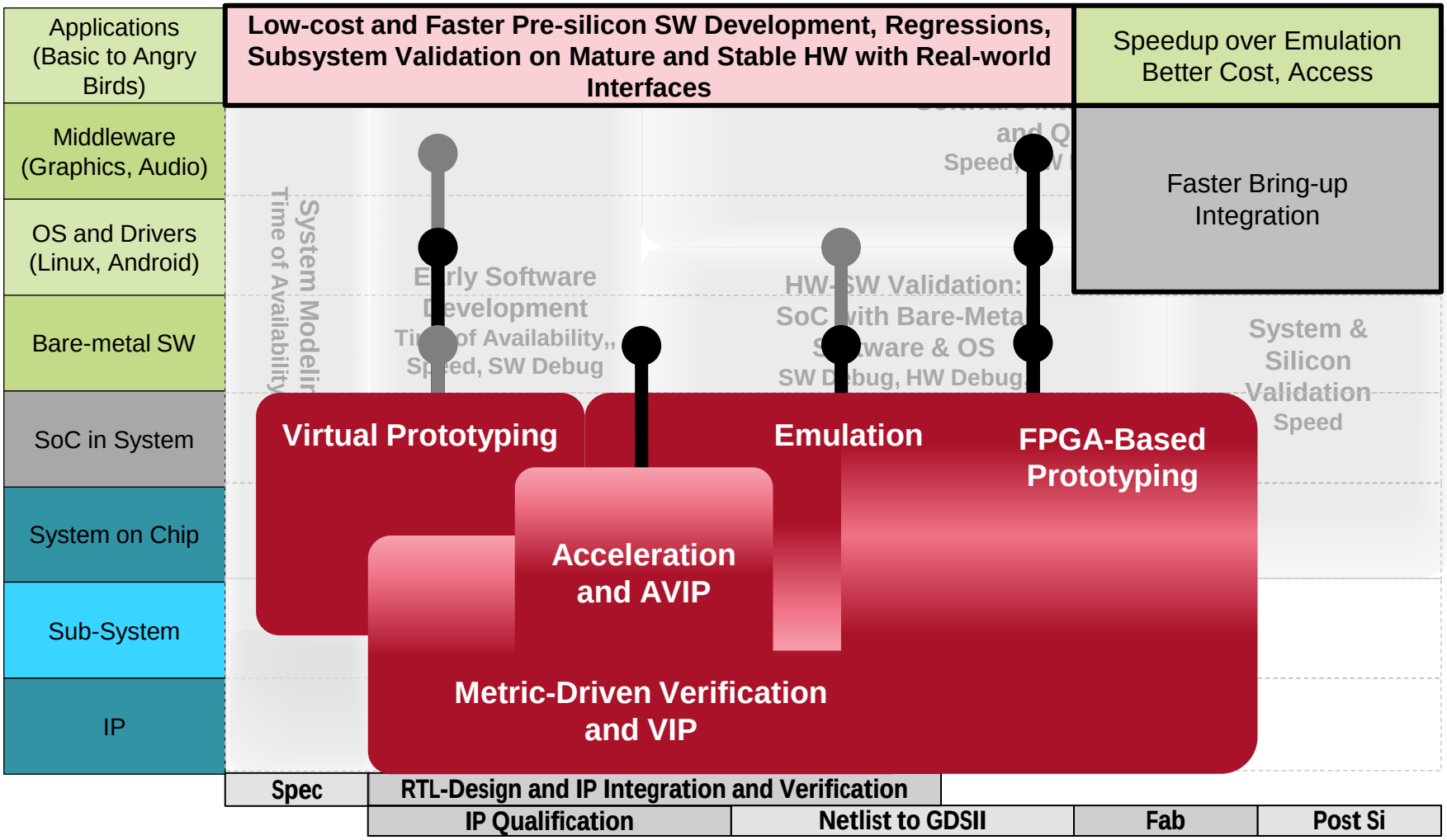
16

Acceleration and Emulation

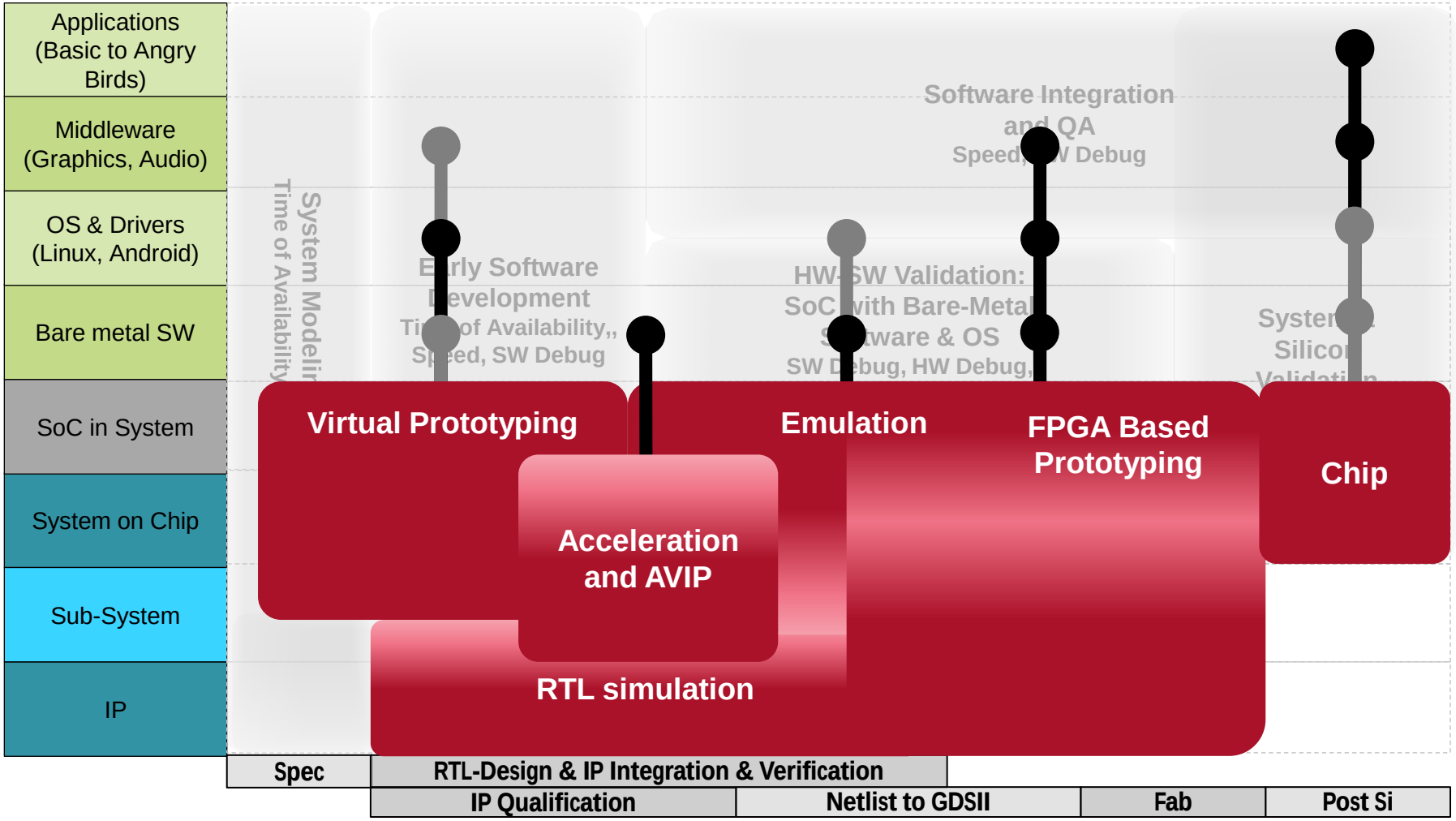


17

FPGA-Based Prototyping

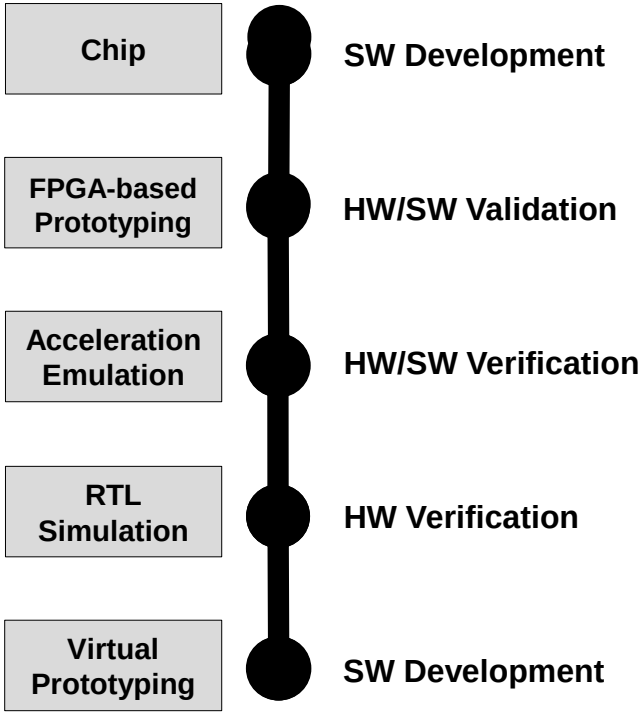


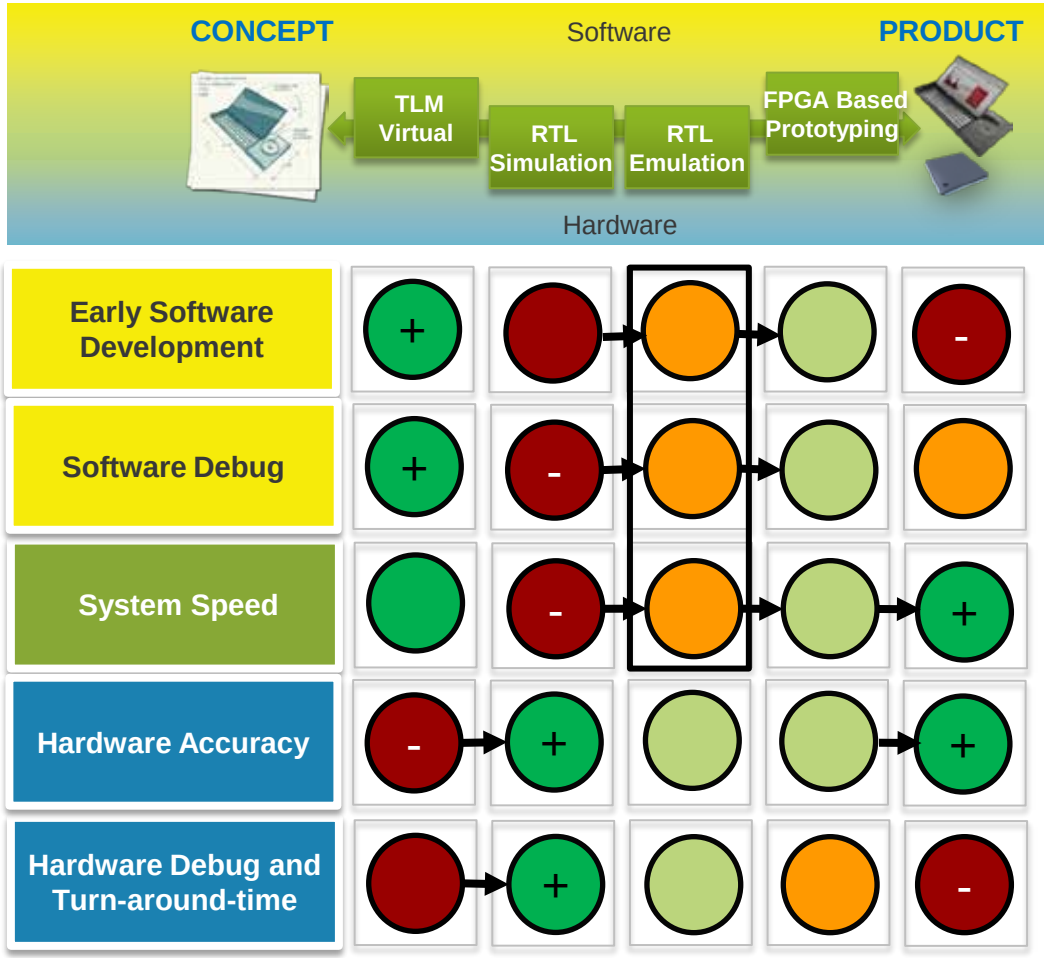
Software Development on the Actual Chip

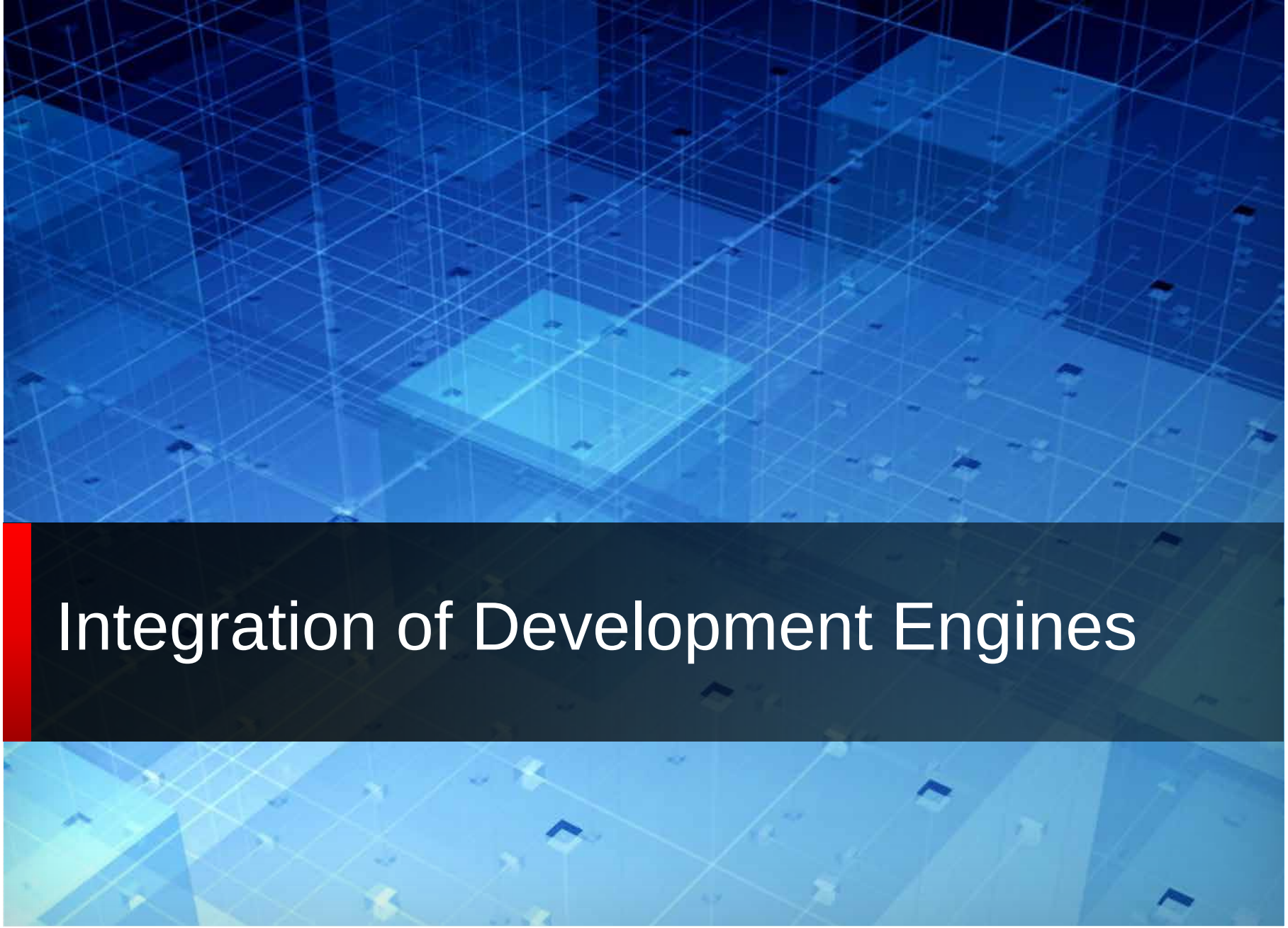


cadence

HW/SW Development Care Abouts

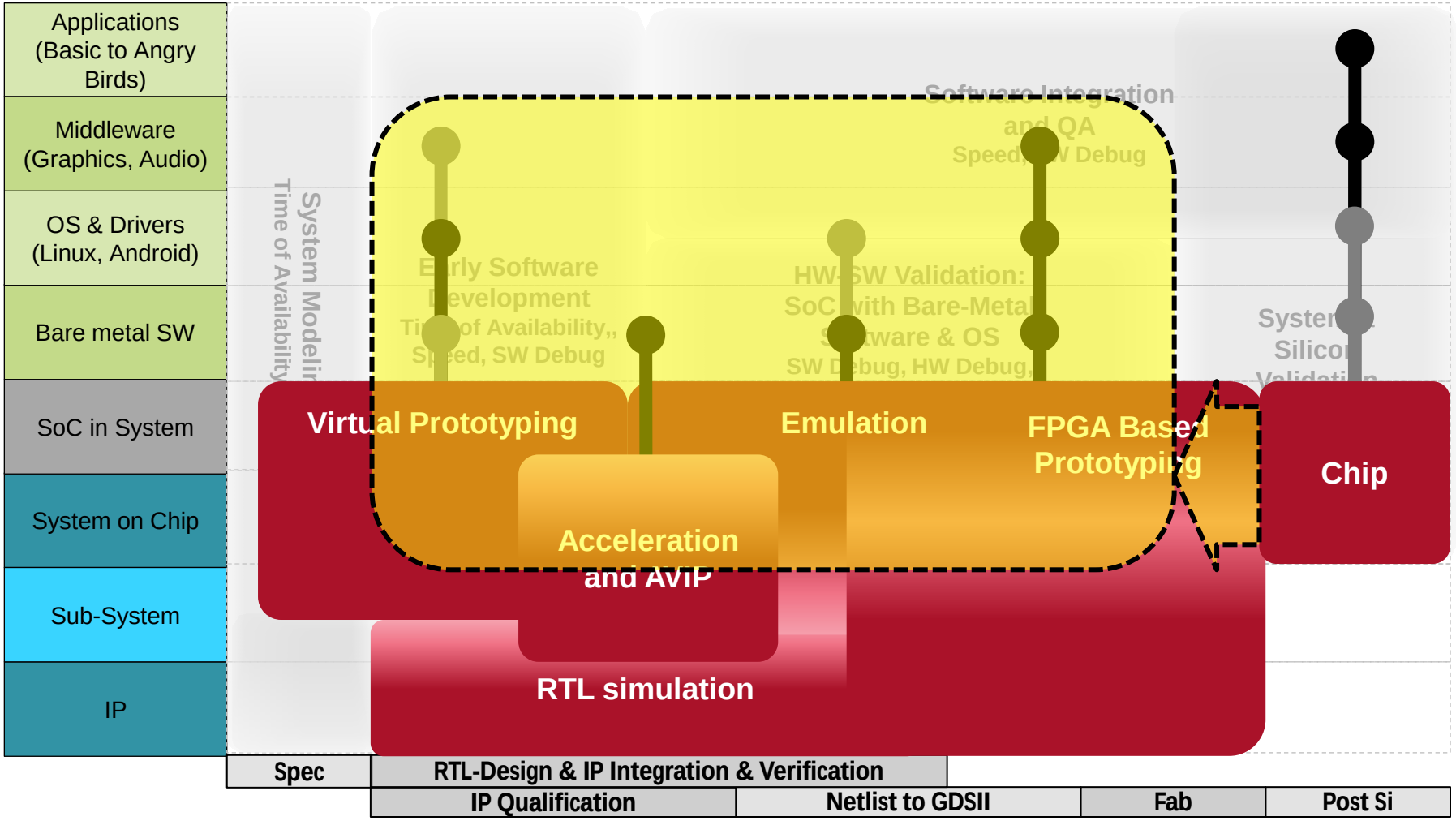






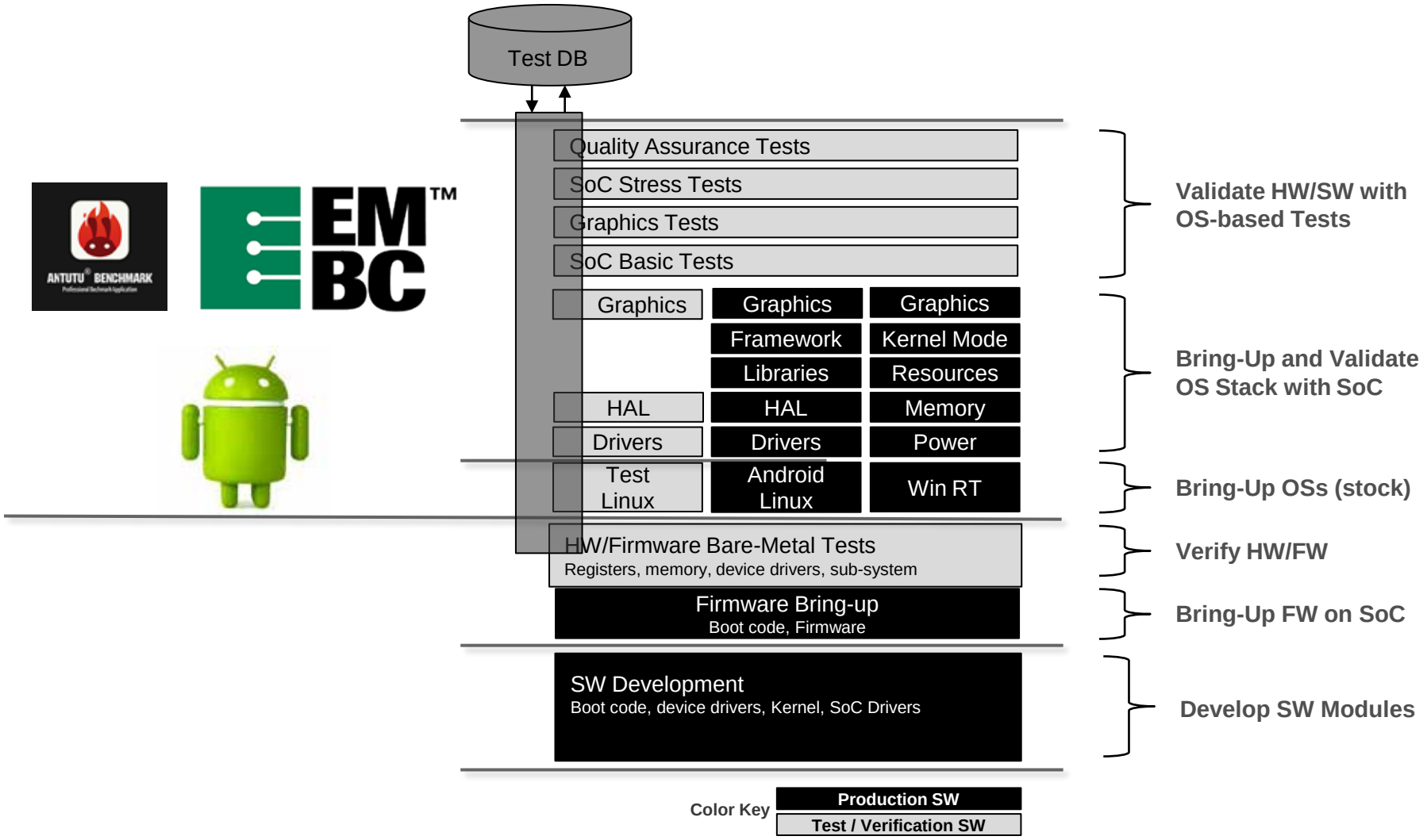
Integration of Development Engines

The Challenge of Bug Re-Production
Consistent HW/SW Verification Environment



cadence

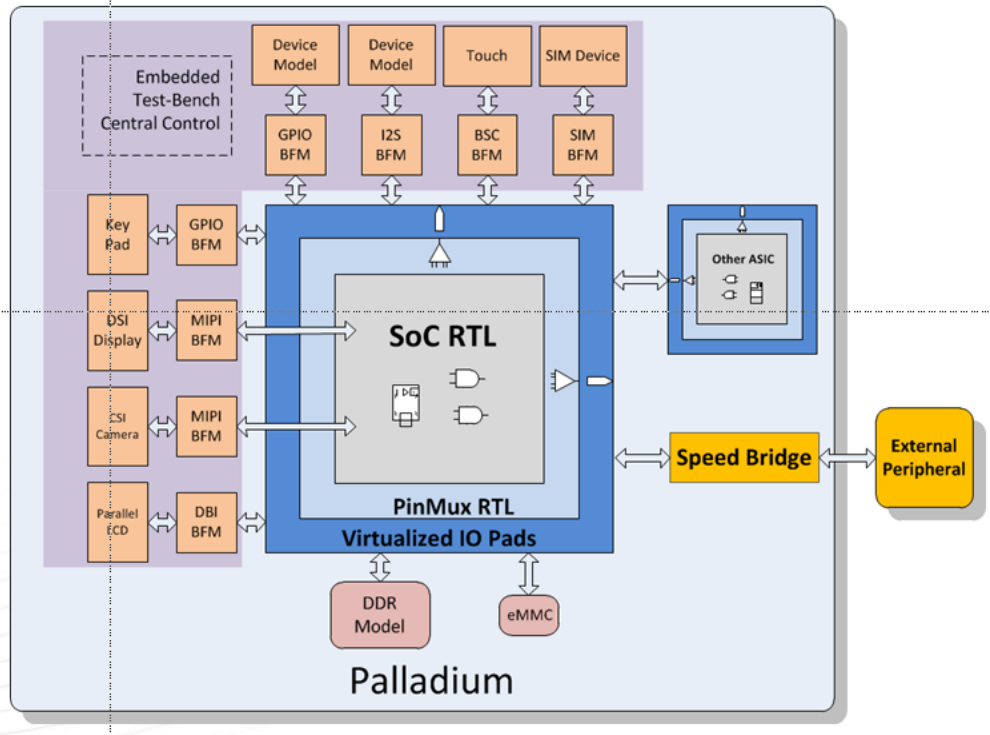
Software Based Testing and Benchmarking



Broadcom Example 1/3

EMBEDDED TEST-BENCH ON PALLADIUM

- **Fully Synthesizable Test Bench**
  - Bus Functional Models (BFMs) for standard interfaces such as SPI, I²S, SIM, SDIO, and I²C
  - Firmware-controlled peripheral models capable of behaving like the actual device (PID, VID, transfer size, and buffer size) for camera, LCD, SIM, etc.
  - Capable of injecting errors and faults
  - Validates data received
- **Virtual Display, Touch, and Keypad on the Console**
- **Test Software and ETB Code Coordinate Tests**
- **Can Be Used for Device Driver Development**



Source: Verification Summit, September 2013

Broadcom Example 2/3

ADVANTAGES OF USE OF EMBEDDED TEST-BENCH ON PALLADIUM

BROADCOM.

- **Full Visibility of Internal Design for Debugging**
  - Use SimVision® to visualize
- **Validate and Verify SoC Design and Performance**
  - Software tests are designed to verify SoC on Palladium during simulation, and then tested in silicon
    - Minimize platform-specific code
    - Built-in infrastructure to take advantage of Palladium-specific support while keeping mobility across simulation, emulation, and silicon test platforms
  - Tests are not as short as they could be for Palladium, but are portable
- **Debugging**
  - Aids debugging by having identical order of events simplifying Palladium replay
  - Almost real-time tests when running on Palladium
- **Very Powerful Pre-Silicon Verification Tool**
  - Critical issues uncovered and resolved before tape-out
  - Numbers are respectable

20

Source: Verification Summit, September 2013

cadence®

Broadcom Example 3/3

ADVANTAGES OF USE OF EMBEDDED TEST-BENCH ON PALLADIUM

BROADCOM.

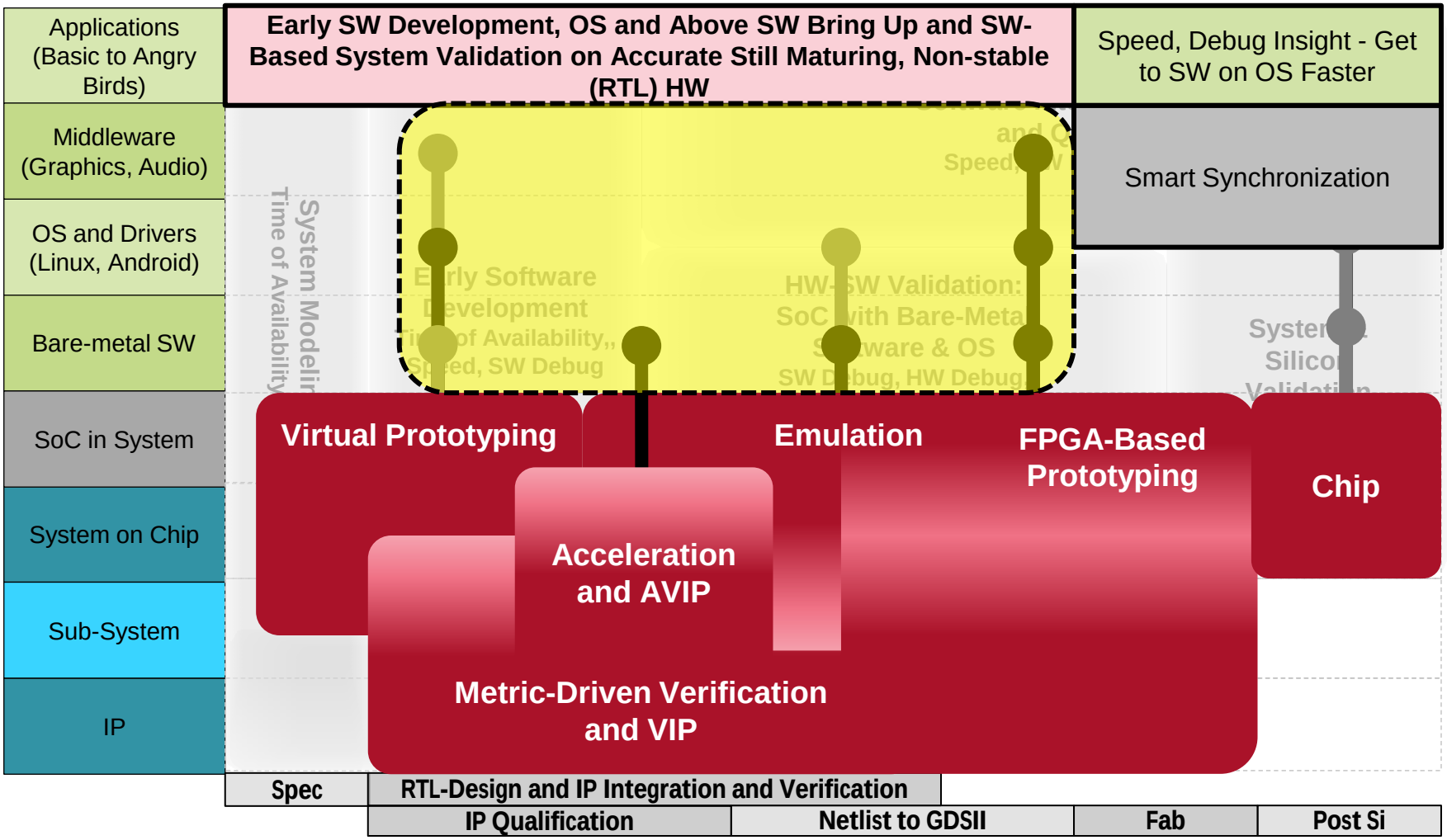
- **Connectivity at I/O Pad Level**
  - Including pin-mux programming
- **Reconfigurable**
  - Peripheral arrangement and quantities
- **Firmware Controllable Peripheral Devices**
  - Embedded models can be used to represent the real device (as the firmware allows)
  - Possibility of error injection
  - Reusable C-based tests, including stress and negative test scenarios
- **Performance Measurement**
  - Complicated and long data transactions can be used
  - Test bench and SoC clocks are representative of actual performance measurements
  - SoC internal logic (FIFOs and switches) are stimulated in the same manner as the actual performance measurements

21

Source: Verification Summit, September 2013

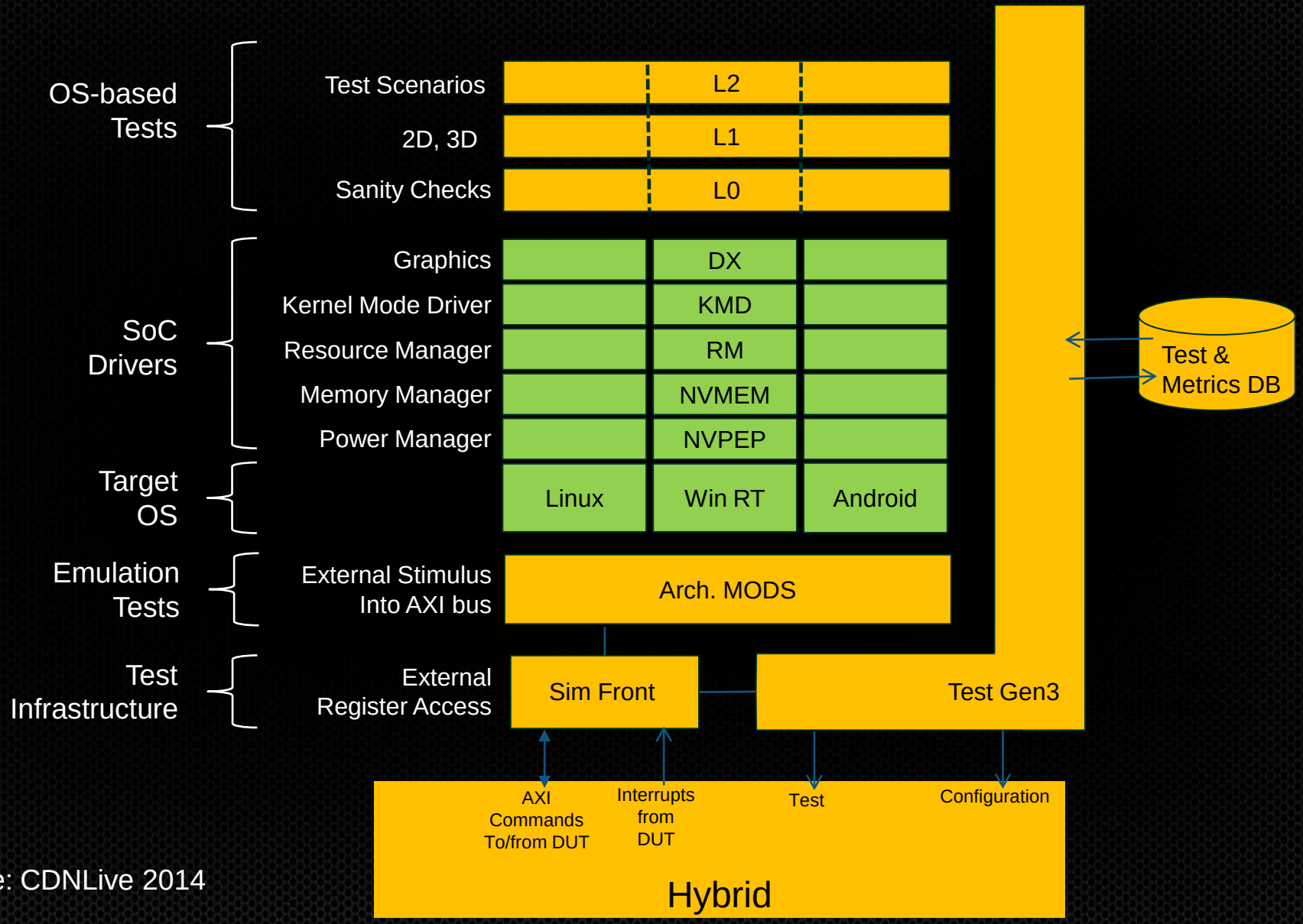
cadence

Hybrids TLM & Accelerated RTL
The Best of Both Worlds



27

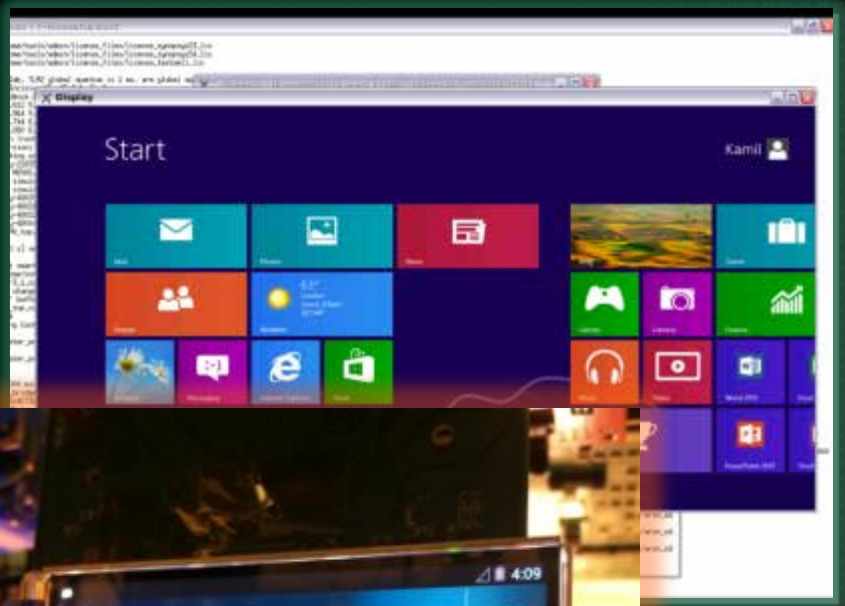
NVIDIA SW Validation with Palladium/VSP Hybrid



Source: CDNLive 2014

Performance Results

- Boot OSes, run real world applications and benchmarks
- Linux kernel boot
  - Palladium only = 45 mins
  - Hybrid = 2 mins
- Android
  - Palladium only = Hours*
  - Hybrid = 40 – 50 mins
- Windows
  - Palladium only = Days*
  - Hybrid = 75 – 90 mins



Source: CDNLive 2014

SW Validation Results

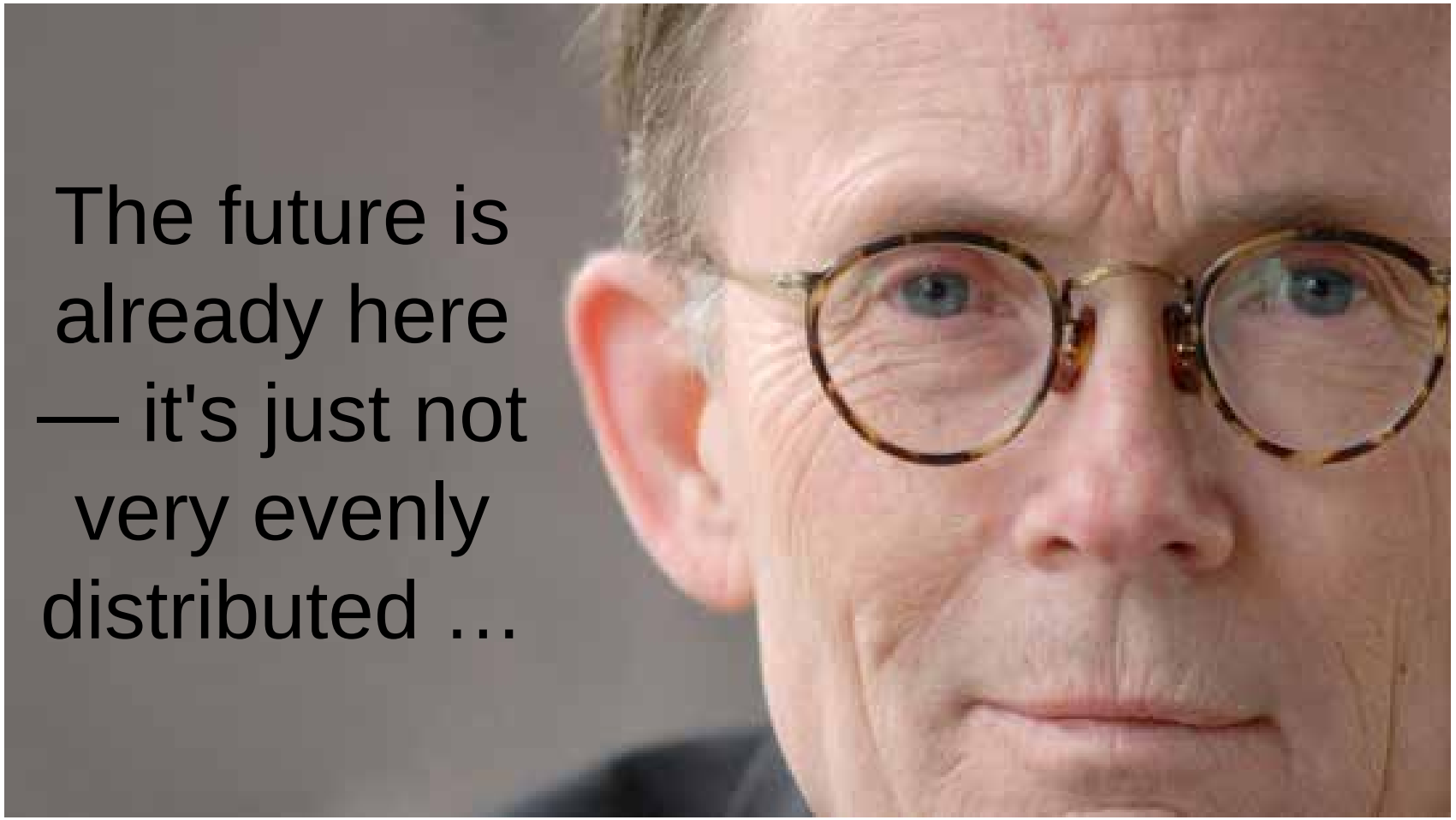
- Eliminated reliance on other pre-silicon platforms
- SW problems found prior to Silicon return
  - SW race conditions
  - Memory management bugs
  - Code completeness
- After silicon return
  - Contributed to smoother bring-up
  - SW Ready to demo product at SOL
  - Less bugs resulted in focused effort to tune for power and perf

Source: CDNLive 2014

Summary

- There is a huge opportunity to optimize development at the hardware/software interface
- Lower layers of software - up to the OS and base apps - need to be part of verification prior to chip tape out
- The market of users is constantly changing
- Software developers are increasing distance, and when not then they need more accuracy, driving needs in …
  - verification re-use and
  - hybrid engine combinations

So what does this mean for EDA?



"The Science in Science Fiction" on *Talk of the Nation*, NPR (30 November 1999, Timecode 11:55), William Gibson

32


cadence®