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Collaborate to Innovate – FinFET Design Ecosystem Challenges and Solutions

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Deputy Director, Open Innovation Platform®
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Agenda

- Lifestyle Trends Drive Product Requirements
- Concurrent Technology and Design Development
- FinFET Design Challenges
- FinFET Ecosystem Solutions

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Future Lifestyle Trends

Mobile Convergence

Augmented Reality

Cloud Computing

Ubiquitous Connectivity

Internet of Things

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Enabling Product Requirements

Mobile Convergence

- Connectivity
- Integration
- Battery life
- Form factor

Augmented Reality

- Service availability
- Latency
- Bandwidth
- Battery life

Cloud Computing

- Latency
- Throughput
- Performance/ W/ $

Ubiquitous Connectivity

- Service availability
- Bandwidth
- Battery life

Internet of Things

- Connectivity
- Reliability
- Battery life
- Cost

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Enabling Product Functionality

Mobile Convergence

- CMOS Image Sensor
- Wireless Transceiver
- Power Management
- Accelerometer
- Gyroscope
- E-Compass

Augmented Reality

- CMOS Image Sensor
- Wireless Transceiver
- Pico Projector
- Gyroscope
- Accelerometer
- Power Management

Cloud Computing

- Power Management

Ubiquitous Connectivity

- Wireless Transceiver
- Power Management

Internet of Things

- Micro-controller
- Wireless Transceiver
- Power Management

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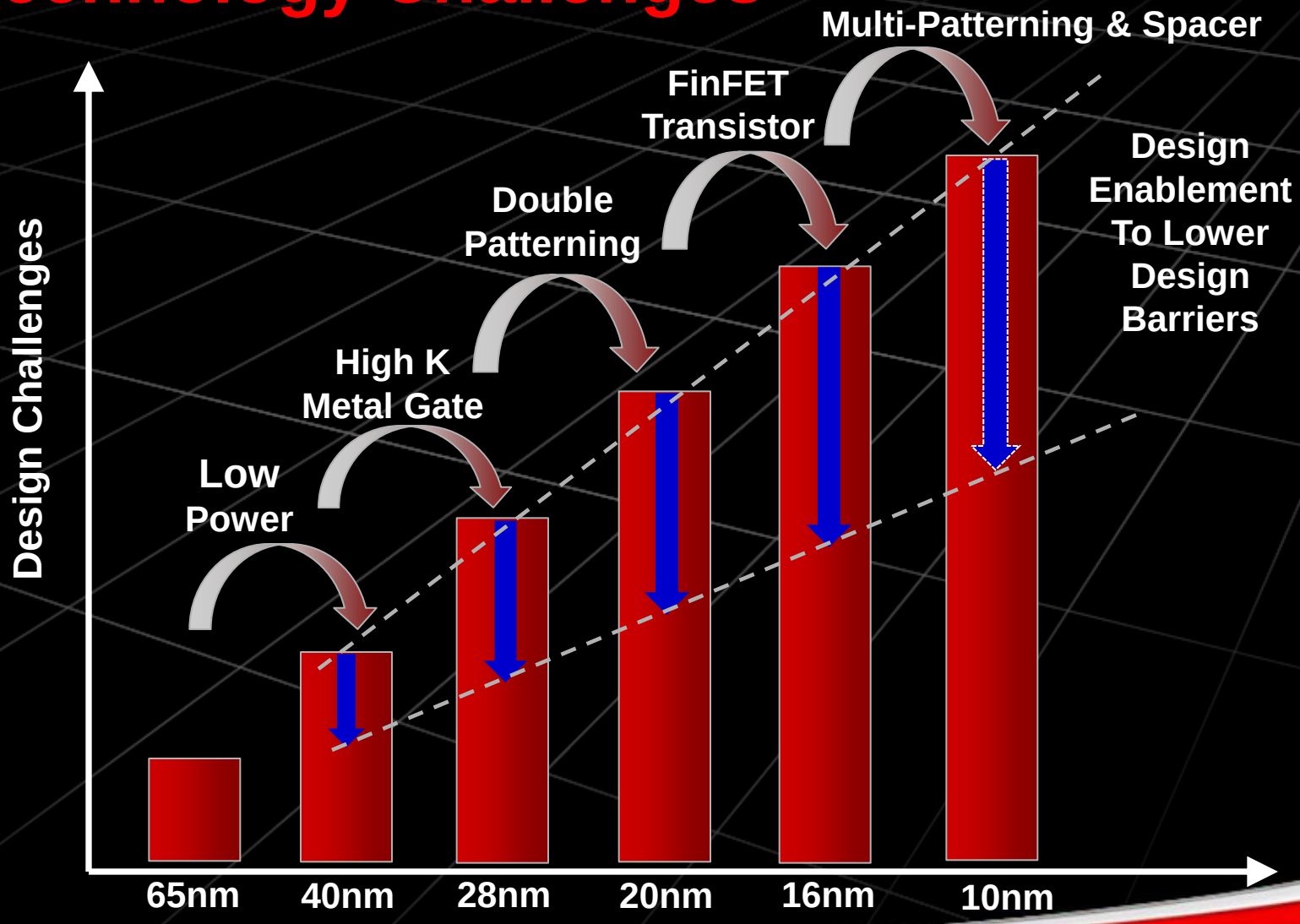
Design Collaboration to Reduce New Technology Challenges



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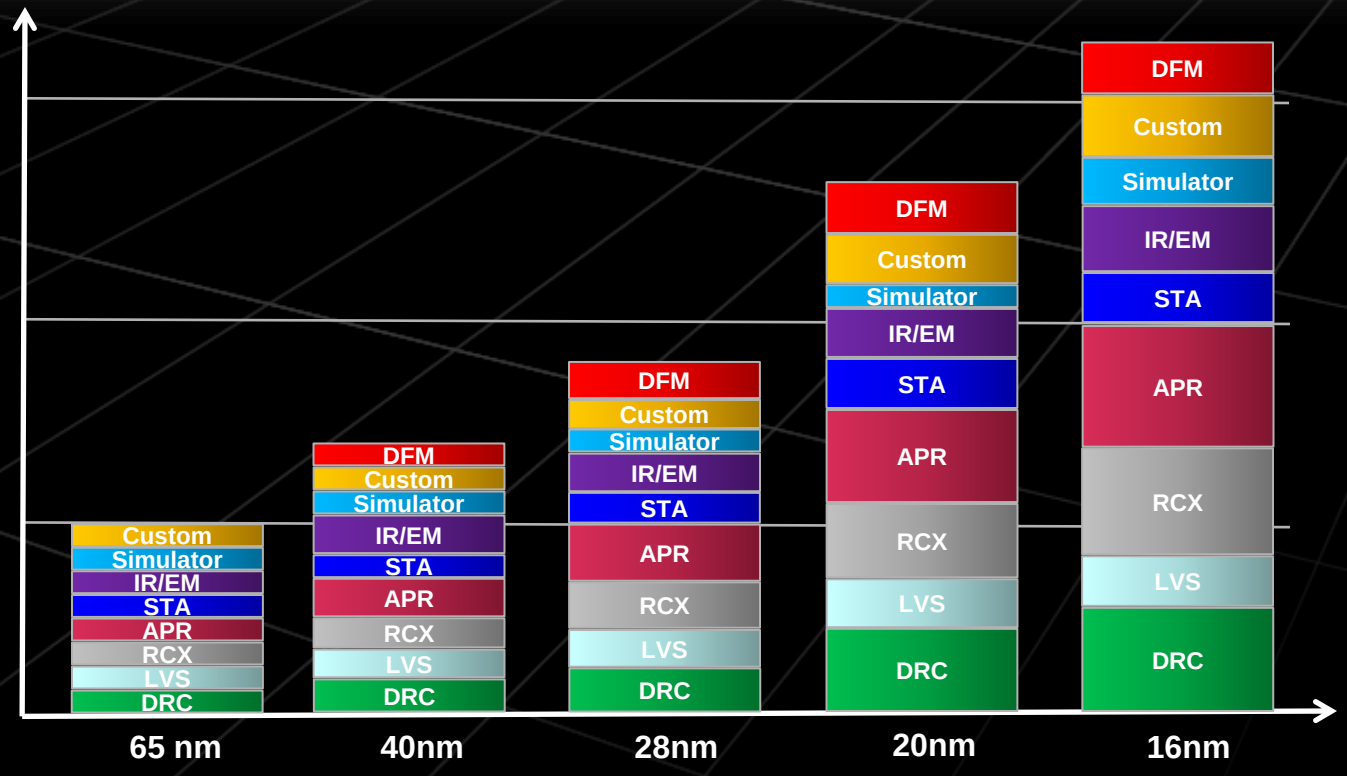
Increasing EDA Tools and Feature Sets to Enable Customer Designs

Number of Supported EDA Tools and Features by Process Node



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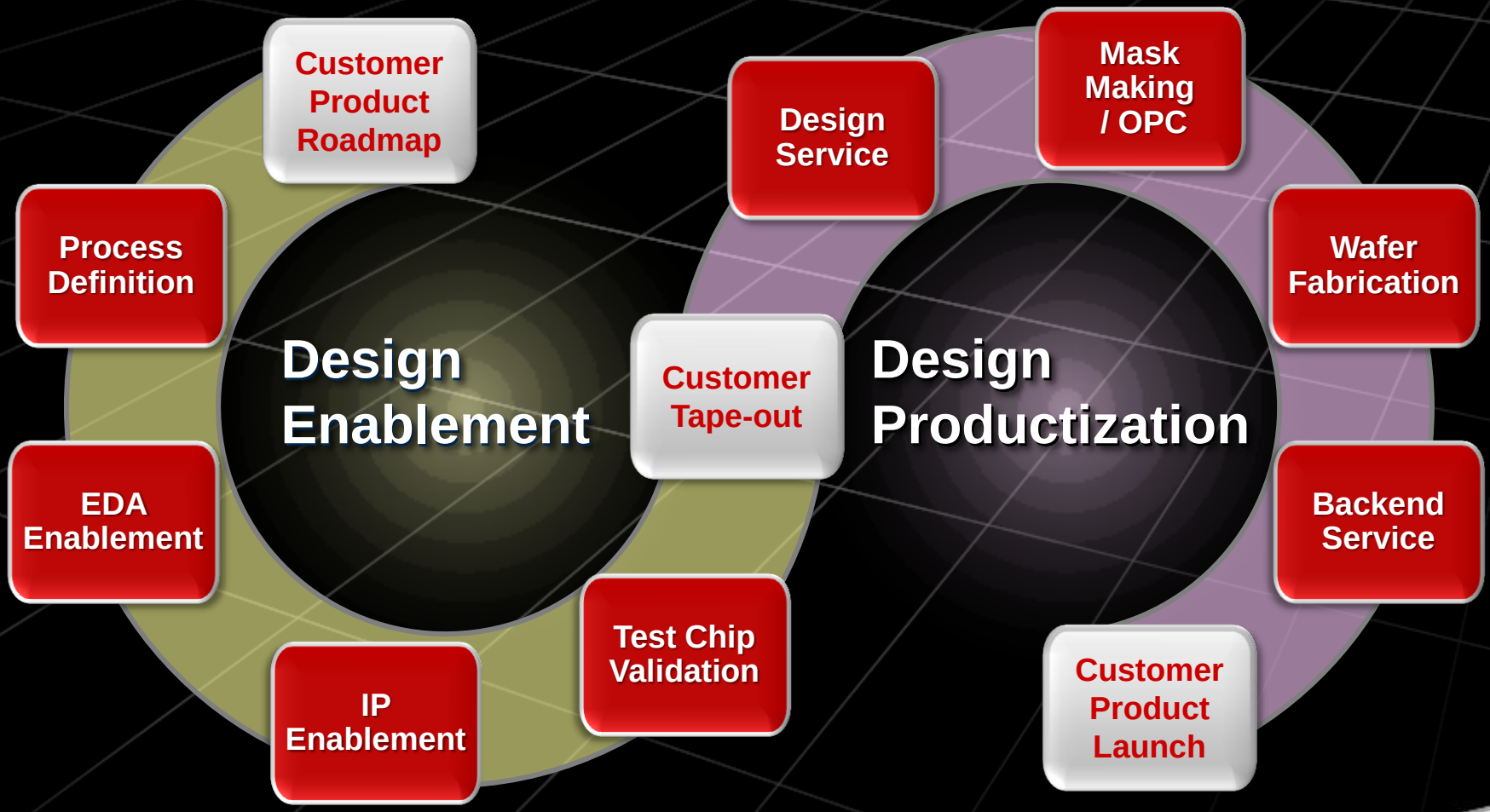
An Ecosystem for Innovation



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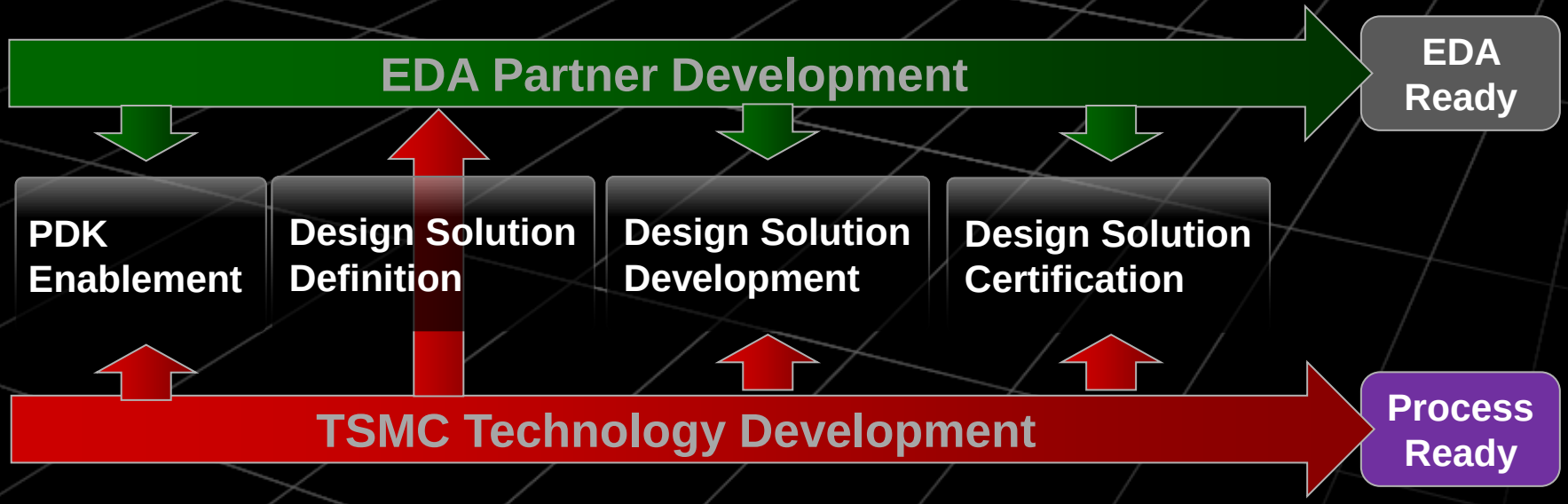
Concurrent Technology and Design -- EDA Partner Collaboration



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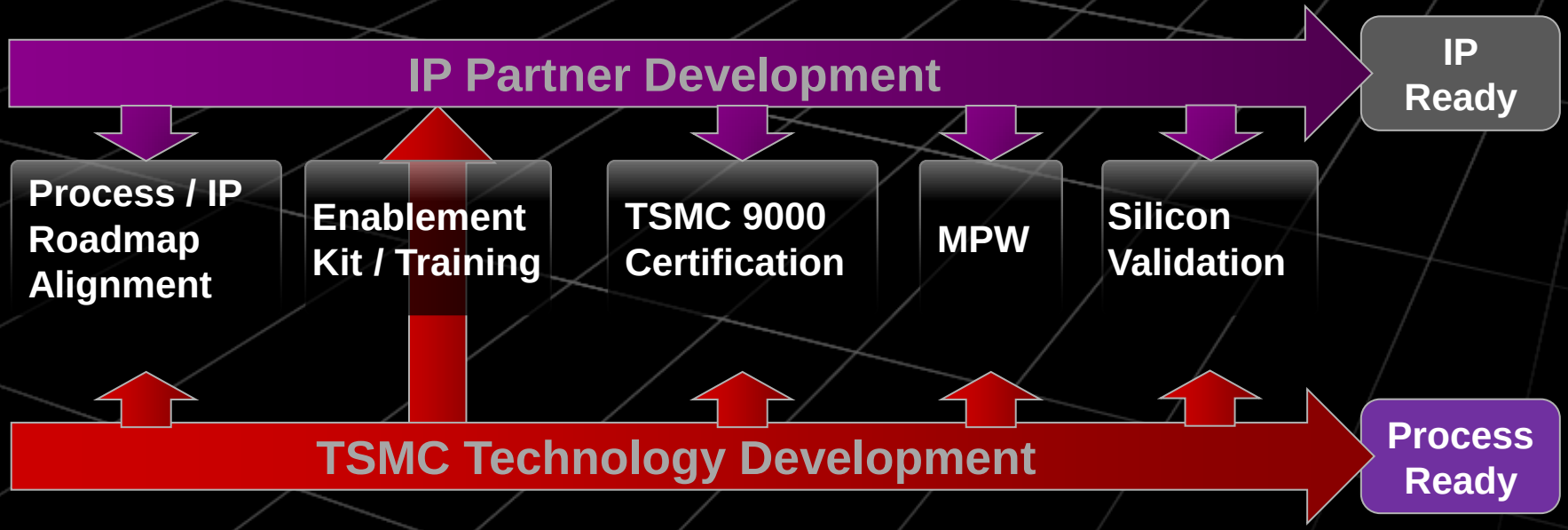
Concurrent Technology and Design -- IP Partner Collaboration



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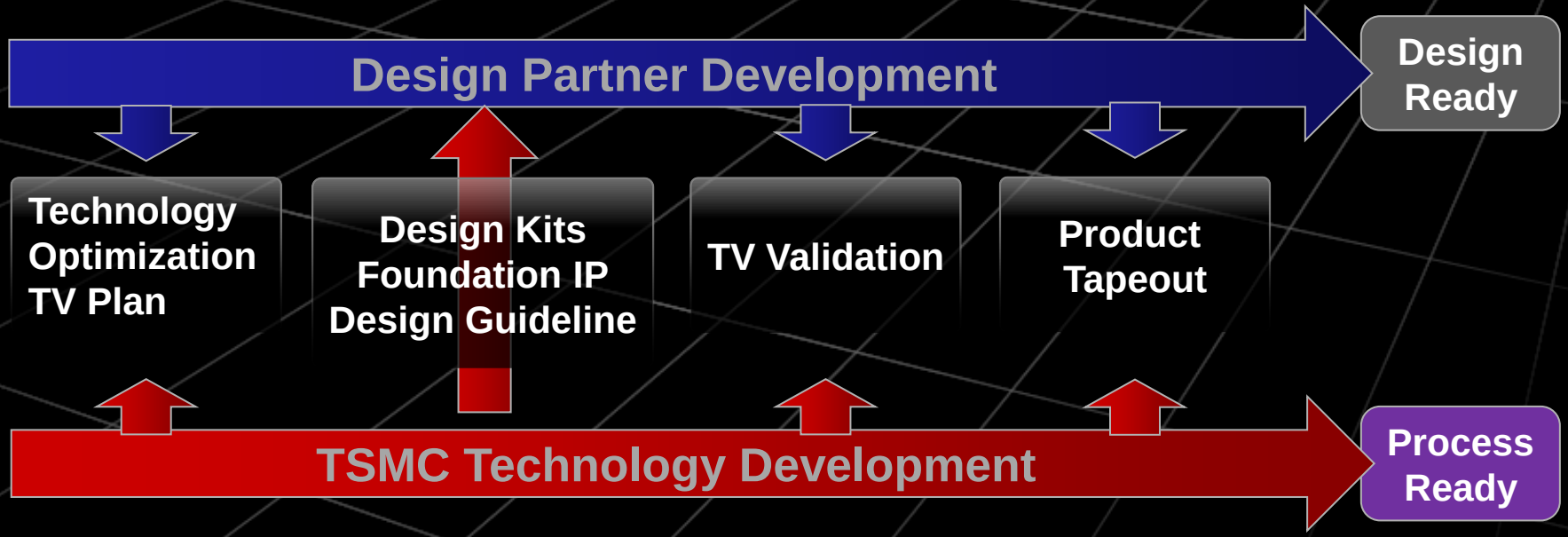
Concurrent Technology and Design -- Design Partner Collaboration



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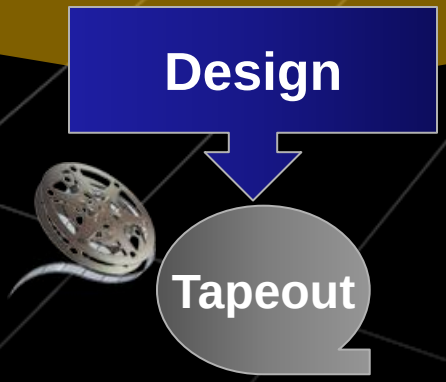
Concurrent Design & Technology Readiness

TSMC-Online
- Design rules
- SPICE model
- Tech files/PDK
- Design kits
- Utilities
- Ref Flow

Certified EDA Tools
- DRC/LVS/RC
- DFM
- P&R
- STA/IR/EM
- Simulation
- Layout editor

Certified IP Portfolio
- Foundation IP
- Interface IP
- Embedded CPU
- Embedded GPU
- Analog IP
- OTP/MTP



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A look back at 50 years of Silicon

Julius Blank
Eugene Kleiner
Robert Noyce
Victor Grinich
Jay Last
Sheldon Roberts
Jean Hoerni
Gordon Moore

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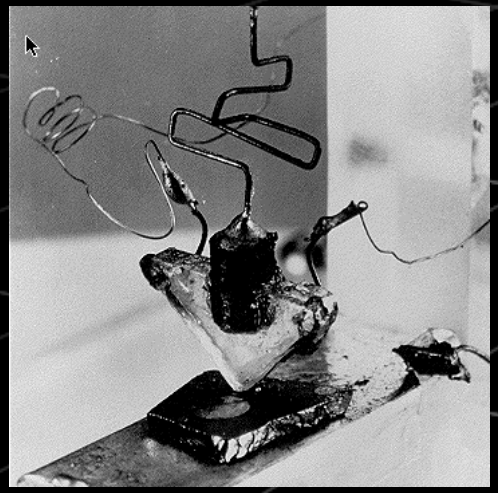
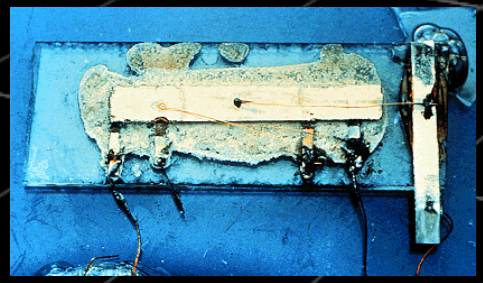
Transistor to IC



First Transistor

Bell Labs

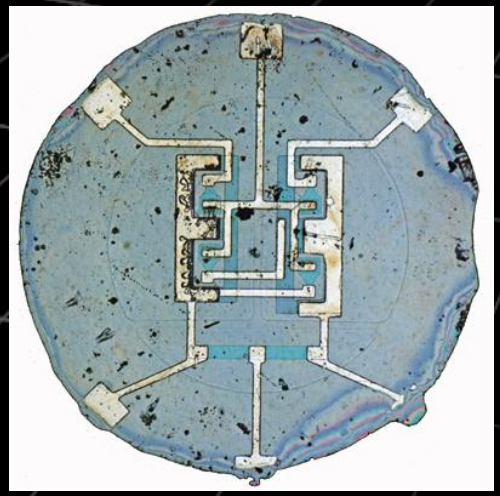
1947



First IC

TI

1958



First Planar IC

Fairchild

1960

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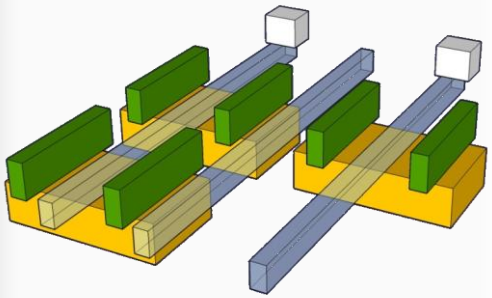
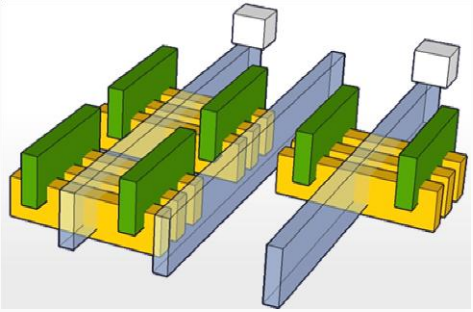
FinFET vs. Planar Characteristics

- **FinFET Benefits**
  - Lower leakage
  - Higher driving current
  - Low-voltage operability
  - Better mismatch
  - Higher intrinsic gain
- **FinFET Challenges**
  - Higher parasitic capacitance due to 3D profile
  - Higher parasitic resistance due to local interconnect
  - Quantized device widths

Planar Device



FinFET



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FinFET Value Proposition

- ~2X gate density improvement compared to 28nm
- 16nmFinFET offers extra 20% speed gain @ same total power or 35% power saving @ same speed with similar gate density compared to 20nm

	16FF/28HPM	16FF/20SoC
Speed @ same total power	38%	20%
Total power saving @ same speed	54%	35%
Gate density	2X	1.1X

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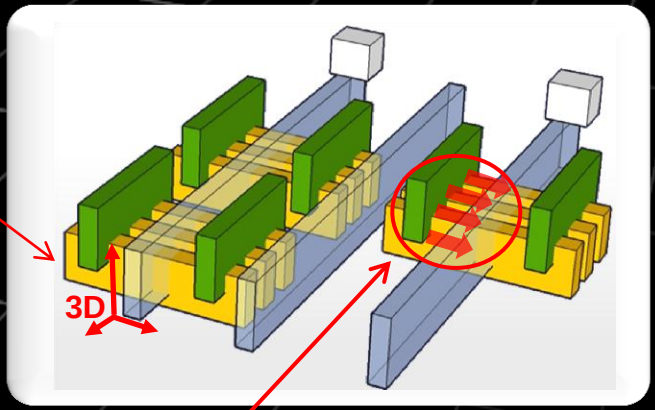
FinFET Design Enablement Requires Collaboration Among Foundry, EDA and Lead Partners

- Parasitic RC extraction: 3D profile support, accuracy
- Design methodology for low voltage operation
- Design methodology for interconnect resistance minimization
- EM reliability and power integrity: High drive current



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FinFET Design Flow Requirements

- 3D FinFET device structure
  - Advanced SPICE modeling for 3D structure
  - Modeling layout dependent effects in 3D structure
- Accurate RC extraction
  - Higher parasitic capacitance due to 3D profile
  - Higher parasitic resistance due to local interconnects
- Quantized device width due to fin pitch/grid requirements
- PODE device handling in designs, EDA tools and IPs
- High-drive current leads to EM reliability and power integrity issues

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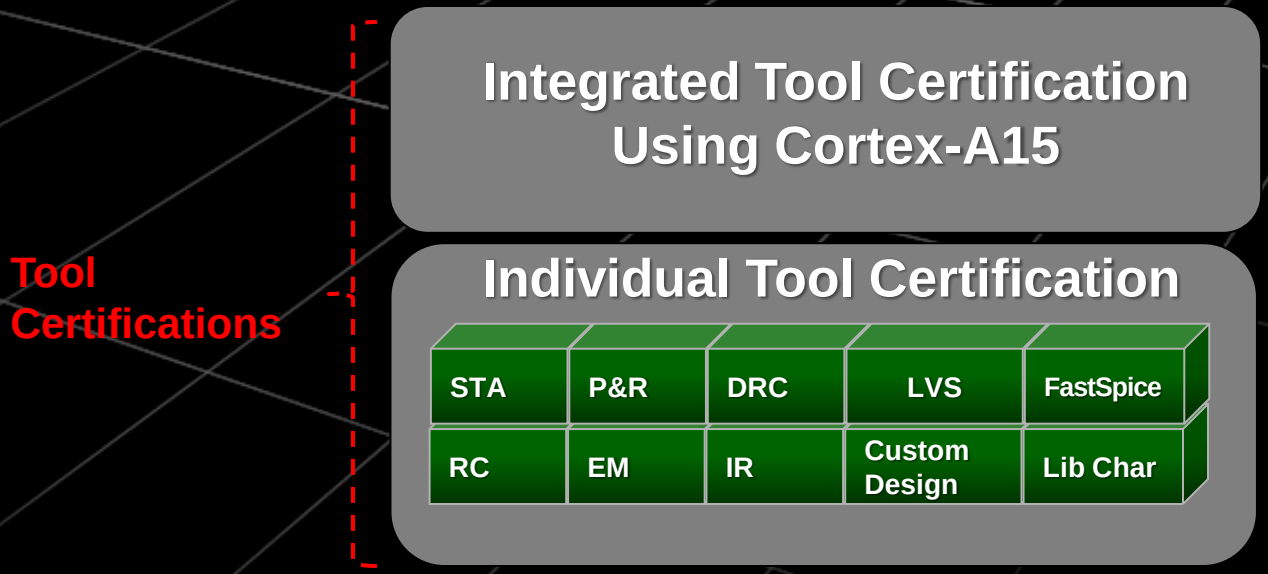
FinFET EDA Tool Certification

- Two levels of tool certification
- Tool certifications as the foundation of FinFET design infrastructure



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Summary

- Technology advancements are driving earlier, wider and deeper ecosystem collaboration to deliver enabling design solutions
- TSMC's collaborative ecosystem unleashes innovations to address FinFET design challenges
- TSMC Open Innovation Platform® has a proven record of success and is more critical than ever for 16nm and beyond

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