FinFETs & SRAM Design

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Agenda

FinFET – the Device

SRAM Design with FinFETs

Reliability in FinFETs

Summary

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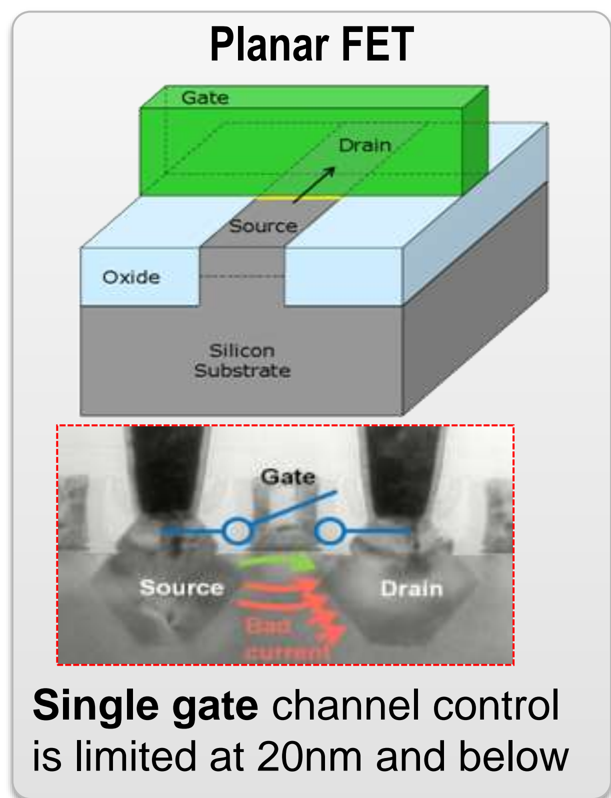
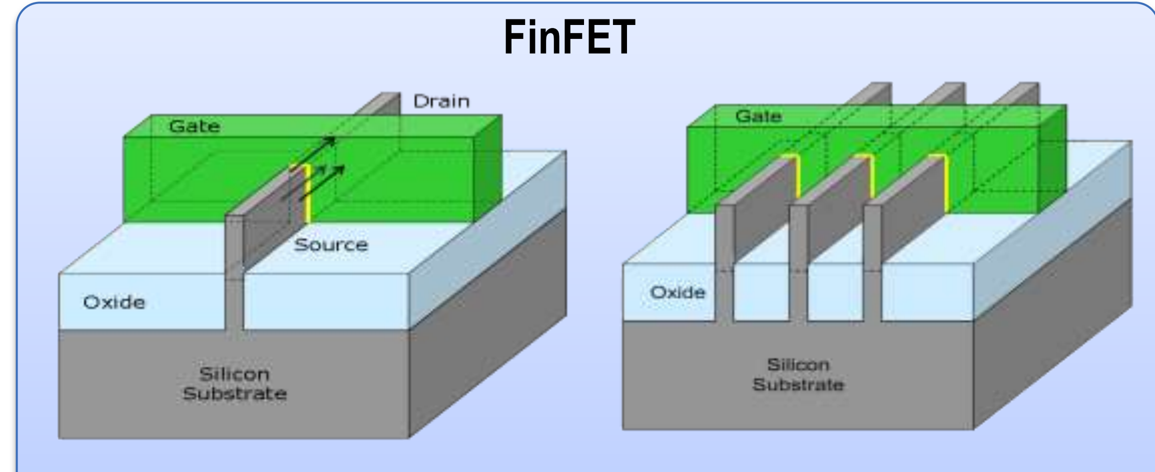
How FinFETs Work

Field Effect Transistors: It is all about Gate(s) Control of the Channel



Single gate channel control is limited at 20nm and below

- Increasing sub-threshold leakage
- Increasing gate leakage
- Decreasing mobility



“**Multiple” gate** surrounds a thin channel and can “fully deplete” it of carriers. This results in much better electrical characteristics.

- Better control of SCE
- Lower DIBL and lower SS
- Higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

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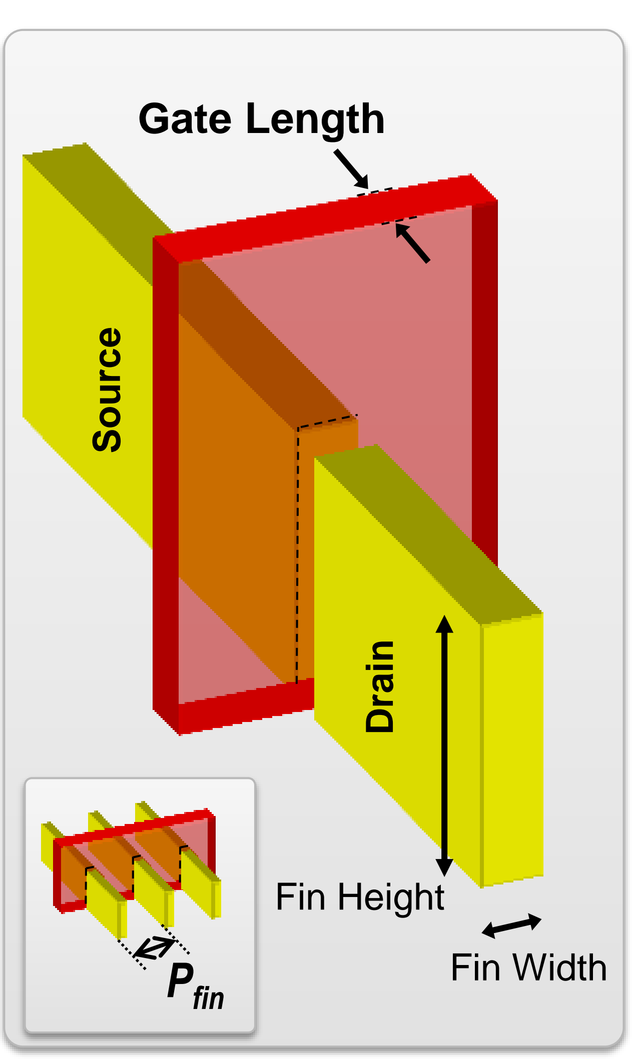
FinFET Advantages & Considerations

Clear Advantages

- Excellent short channel control leads to
  - Lower leakage (lower DIBL and lower SS)
  - low V_t variability due to low channel doping
  - Less variability caused by random dopant fluctuations
  - Lower operating voltage -> 50% dynamic power savings

Additional Considerations

- Quantized widths (and channel lengths)
- Body biasing totally ineffective
- Higher parasitics
- Potential Self-Heating issues
- Thermal aspects of ESD can be an issue
- Degradation and aging: NBTI a bit worse than planar



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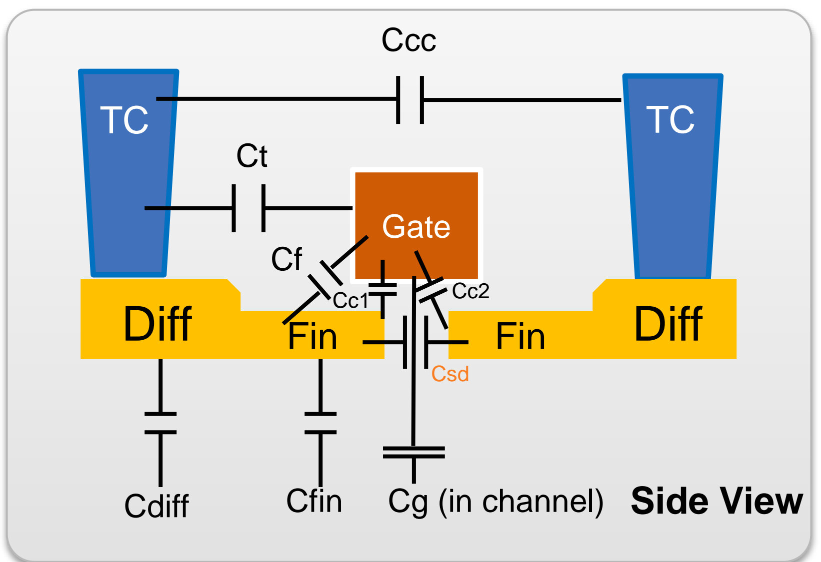
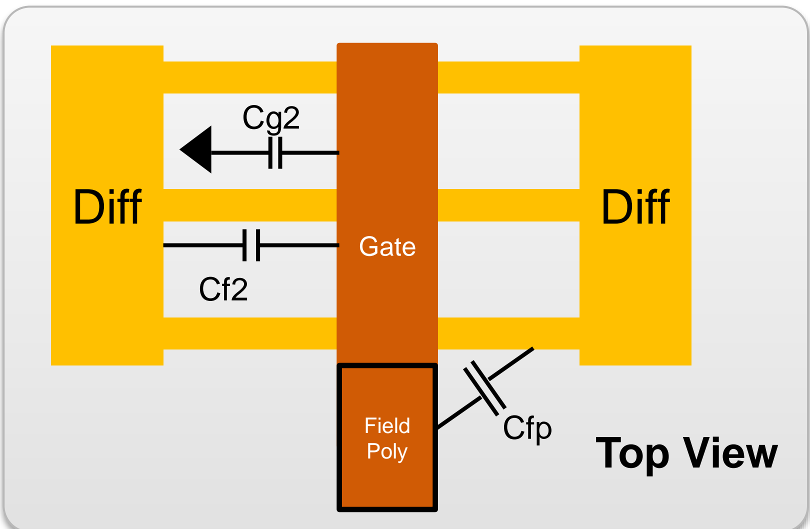
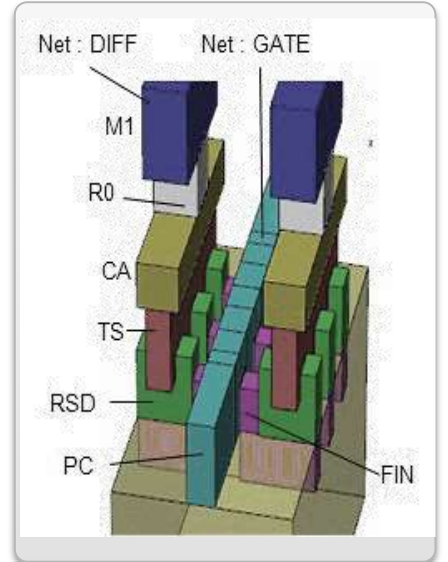
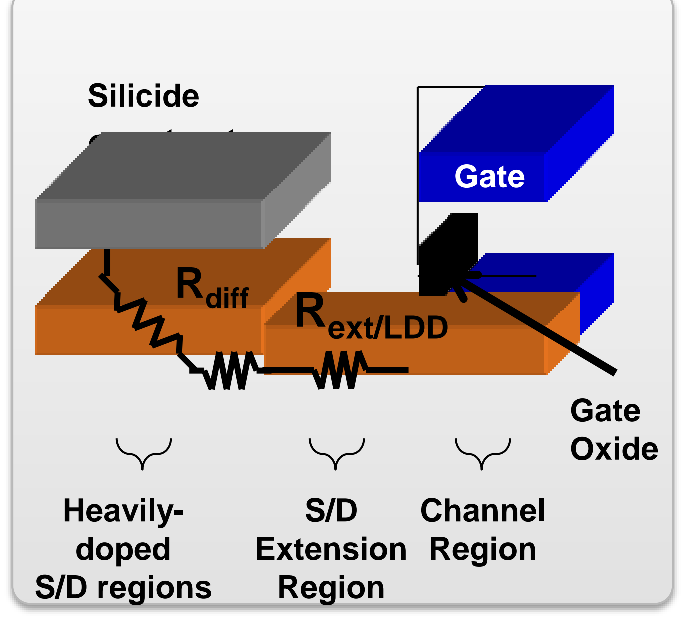
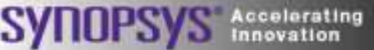
FinFET Device Complexity











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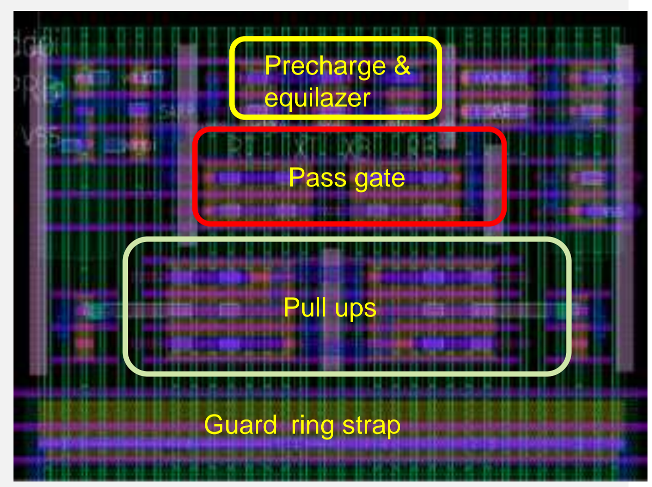
FinFET SRAMs
The Good News

- Higher performance and lower leakage compared to planar
- Operates at lower Vdd than planar
- Good static noise margin (SNM) at low Vdd
  – Decent noise to signal ratio can be achieved (with a β=2 for example)
  – Good (Low) Variability
  – Read Margin and Write Margin distribution narrower than in planar

Source: Kawasaki et al, 2006 Symposium on VLSI technology Digest of Technical Papers



Synopsys 14 nm Sense AMP

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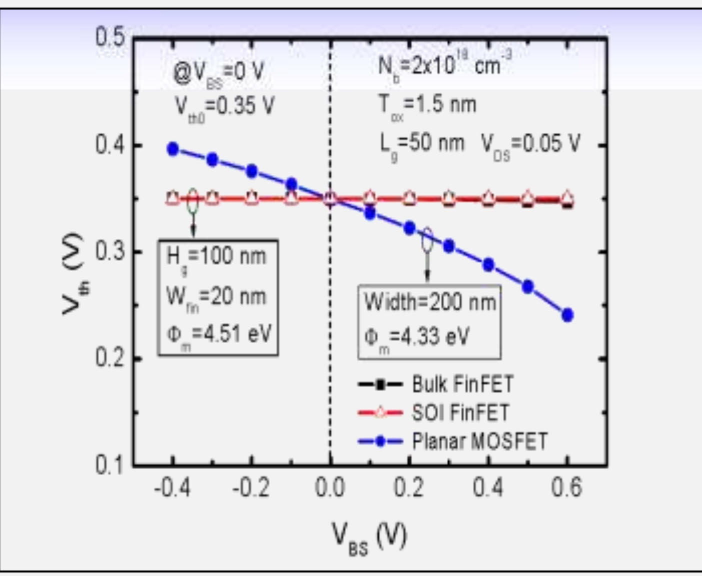
FinFET SRAM Challenges

- The β ratio is a quantized number thus fine-tuning β is not possible
  - Poses challenges for both the read and write margins
  - Requires assist circuitry for reliable operation
- Body-bias techniques are not efficient – New techniques needed
- Realizing long channel devices is litho driven (DP vs. spacer) and has limited options
  - Stack short channels in series
  - Manipulation of spacer (very limited)
  - Multi-Fin pitch



Source: Jong-Ho Lee Seoul National University Thesis

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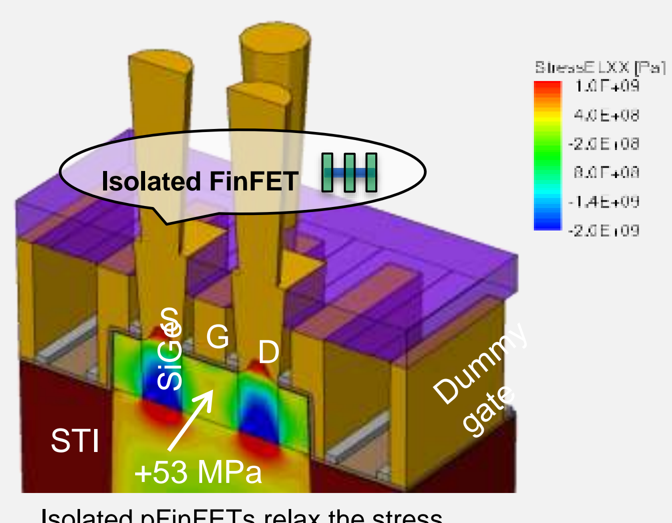
FinFET SRAM Challenges (cont.)

- Layout effects on devices critical (lonely FinFET phenomena)
- Self-heating could be a problem since fins are less efficiently cooled
  - Need to be properly modeled and accounted for
- With node scaling, channel area decreases and σV_t increases
  - Vt mismatch issues (challenges stemming from variation of T_{ox}, ε_{ox}) and work function along the fin height
- Aging simulation is important. NBTI dominates PBTI



Isolated pFinFETs relax the stress
(Driving current drops significantly!)

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SRAM Assist Schemes Survey

TECHNIQUE	HELPS	CONCEPT	COMMENTS
Constant negative-level write buffer (CNL-WB)	Write margin	BL-level adjustment	Suitable for memory compilers
Dynamic power supply (column based)	Read and Write margins	SRAM cell voltage to be switched dynamically based on the actual read, write	Various techniques, some need IO VDD source . Can have dummy read issues
Negative bit-line capacitive coupling	Write margin	Improves pass-gate transistor drive compared to pull-up	No dummy read problems, No area/ power penalty, No external VDD needed.
Adaptive dynamic word-line underdrive	Read margin /Write margin	Forward bias/ reverse bias pull-up for higher / lower drive	Each done separately at the expense of the other margin
Sense AMP bit-line amplification	Read margin	Provides full BL amplification to half-selected columns. Full BL amplification	Significant overhead cost
Word-line lowering	Read margin	Weaken pass-gate transistor drive	Bad for power
BL pulsing	Read margin	Improves the discharge rate of the low-node of the cell	Deteriorates writability
WL pulsing	Read margin	Provides data recovery by writing back the original data prior to the disturb.	Deteriorates writability
Dual Supply	Read margin		Has power savings angle in addition to read margin improvement
RMW (Read Modify Write)	Read margin	Use pre-column sense amp. All cells are read first and re-written	Sense amp timing is critical

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Reliability in FinFETs

- **HCI in FinFETs :** The narrower the FIN, the better the HCI immunity due to smaller half-life of the hot electrons
  - In general, HCI immunity for FinFET is better than planer
- NBTI/PBTI (Negative / Positive Bias Temperature Instability): a function of the high-K gate stack not of the device.
  - In theory should be very similar to planar
  - **There are indications it is worse for FinFET because of higher density of hydrogen dangling bonds at the Fin-Gate stack interface due to the <110> orientation of channel**
  - More significant for FinFETs due to lower nominal Vt and nominal VDD
  - Not enough data available to establish a defined trend

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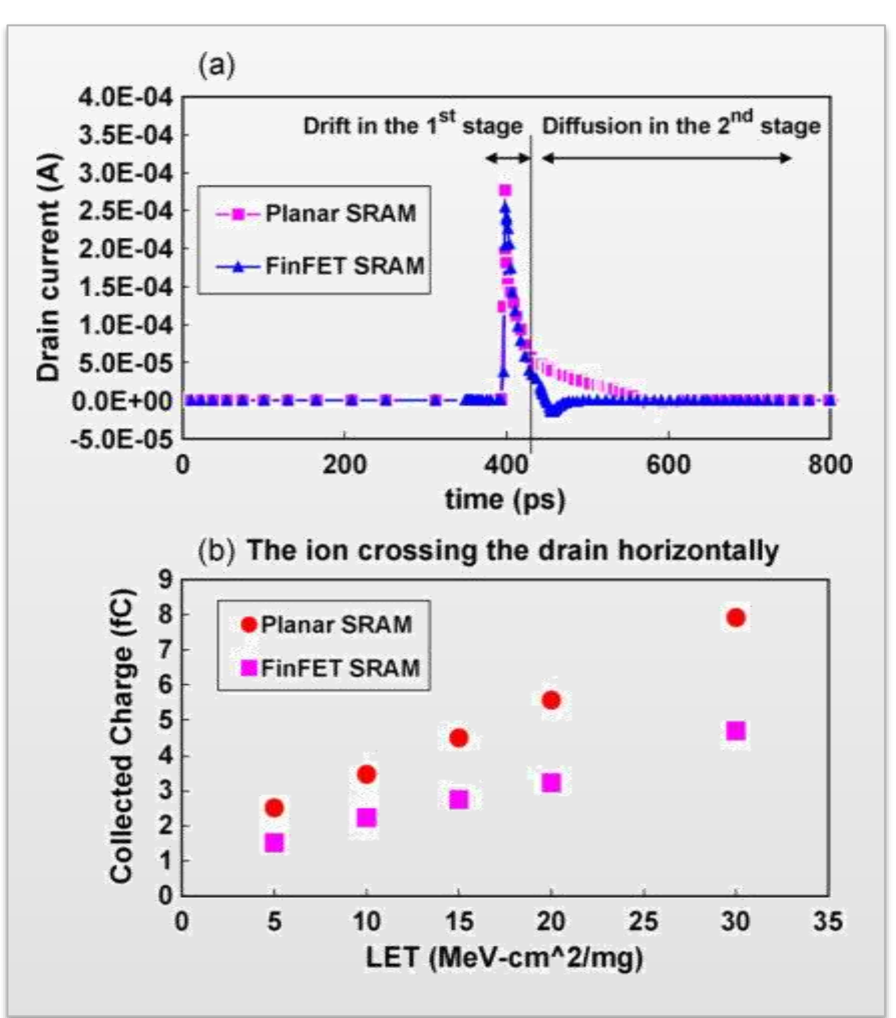
Soft Error Rate – FinFETs vs. Planar

- TCAD simulation indicates that with all identical variables, SER rate in bulk FinFET- based SRAM is better than planar
- Charge generation caused by energetic impinging particles is in the substrate. In planar, a lot of it can reach the drain
- In FinFET, the conduction is mainly in the channel, thus most of the charge dissipates in the substrate, NOT in the drain, therefore probability of upset is much lower



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The Real Deal About FinFETs

Designers must deal with new BSIM models, new netlist parameters, quantized “W” and “L” , NF, NFIN, etc. but no major disruption in design methodology for IP users

SRAM design techniques including body bias and various assist techniques might not work for FinFETs and require a fresh approach

Layout migration from planar is not always feasible. High device parasitics and high device performance dependency on layout call for extreme care in layout

HCI and SER are generally better than in planar due to thin body & elevated channel. NBTI is slightly worse

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