The Challenges of FinFET Design

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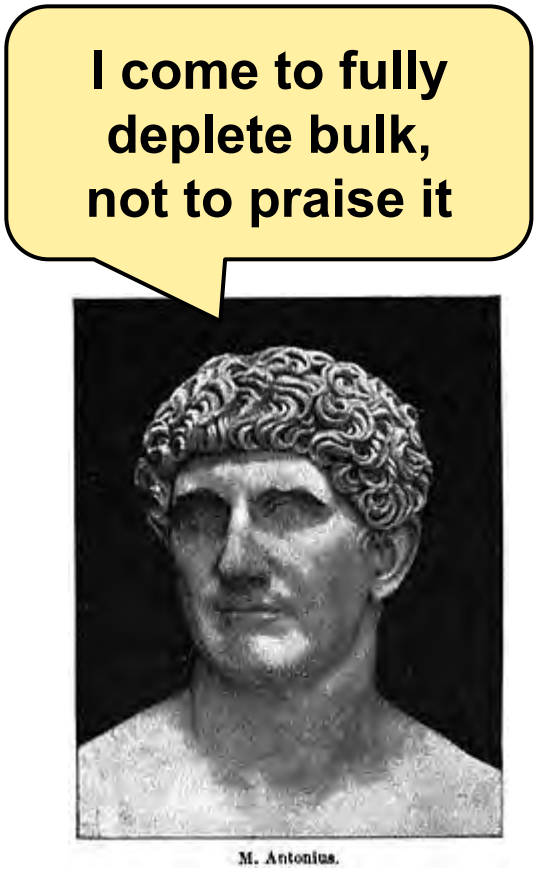
20nm: End of the Line for Bulk

- Barring something close to a miracle, 20nm will be the last bulk node
  - Conventional MOSFET limits have been reached
  - Too much leakage for too little performance gain
- Bulk replacement candidates
  - Short term:
    - Planar FDSOI or FinFET/Tri-gate/Multi-gate
  - Longer term: III-V devices, GAA, nanowires, etc.

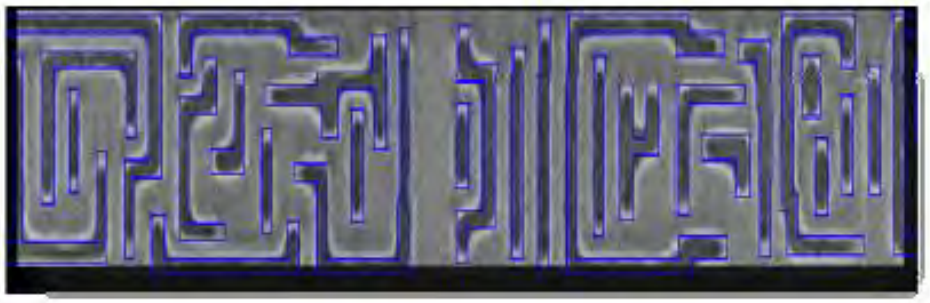


A Digression on Node Names

- Process names once referred to half metal pitch and/or gate length
  - Drawn gate length matched the node name
  - Physical gate length shrunk faster
  - Then it stopped shrinking
- Observation: There is nothing in a 20nm process that measures 20nm

Node	1X Metal Pitch
Intel 32nm	112.5nm
Foundry 28nm	90nm
Intel 22nm	80nm
Foundry 20nm	64nm

Source: IEDM, EE Times

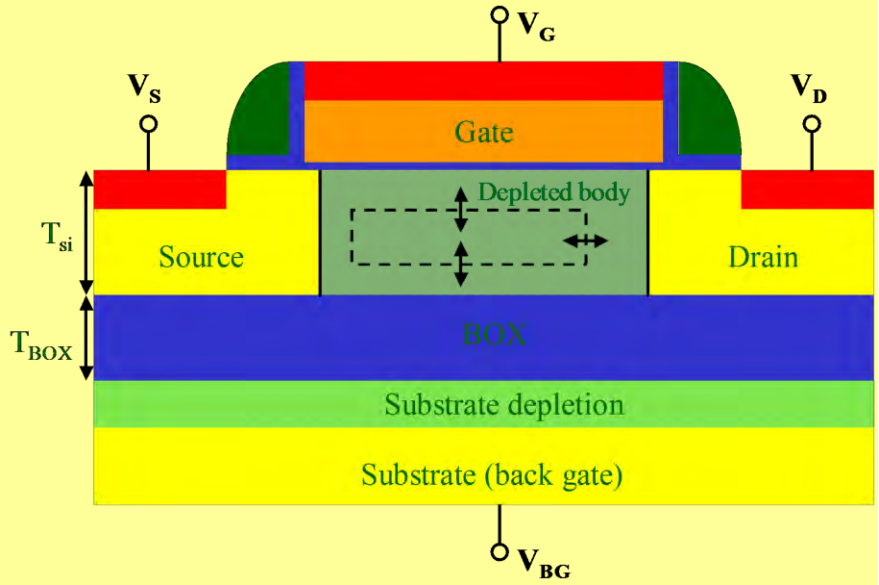


14nm node ARM M1 clip, 46nm minimum pitch, exposed on an NXE:3300B with conventional illumination

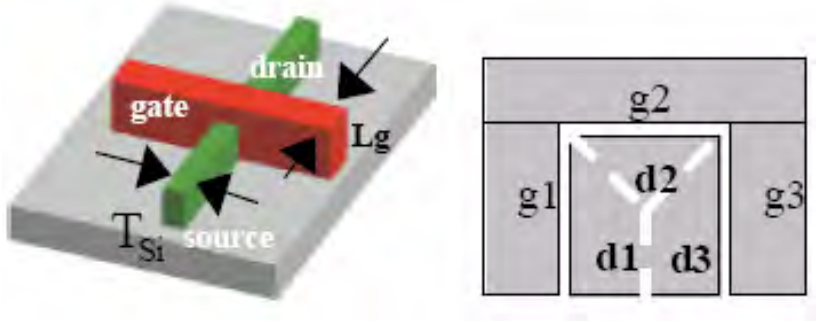
Source: ASML keynote, IEDM 12

Getting Beyond Bulk: The Contenders

- FDSOI
- Fabs: **ST**, Global, IBM
- Claim to fame: Better than bulk, easier than fins

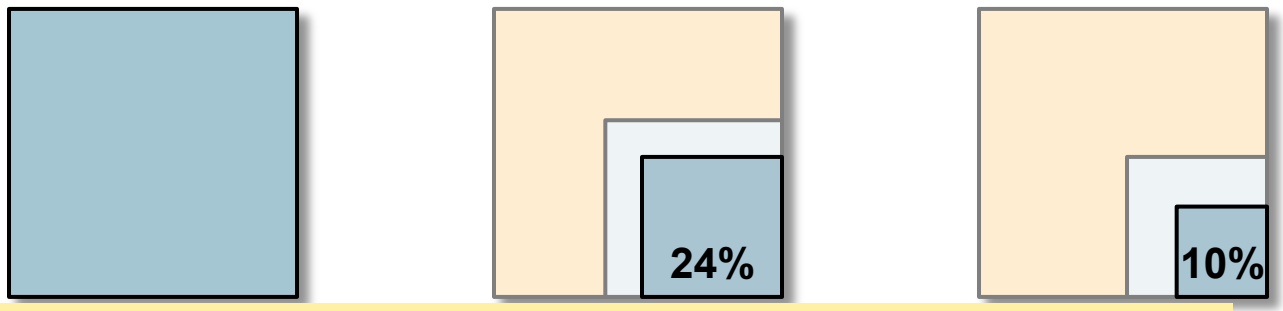


- FinFET
- Fabs: **Intel**, Global, IBM, Samsung, TSMC
- Claim to fame: 3D is the future, and the future is now



The “Dark Silicon” Problem

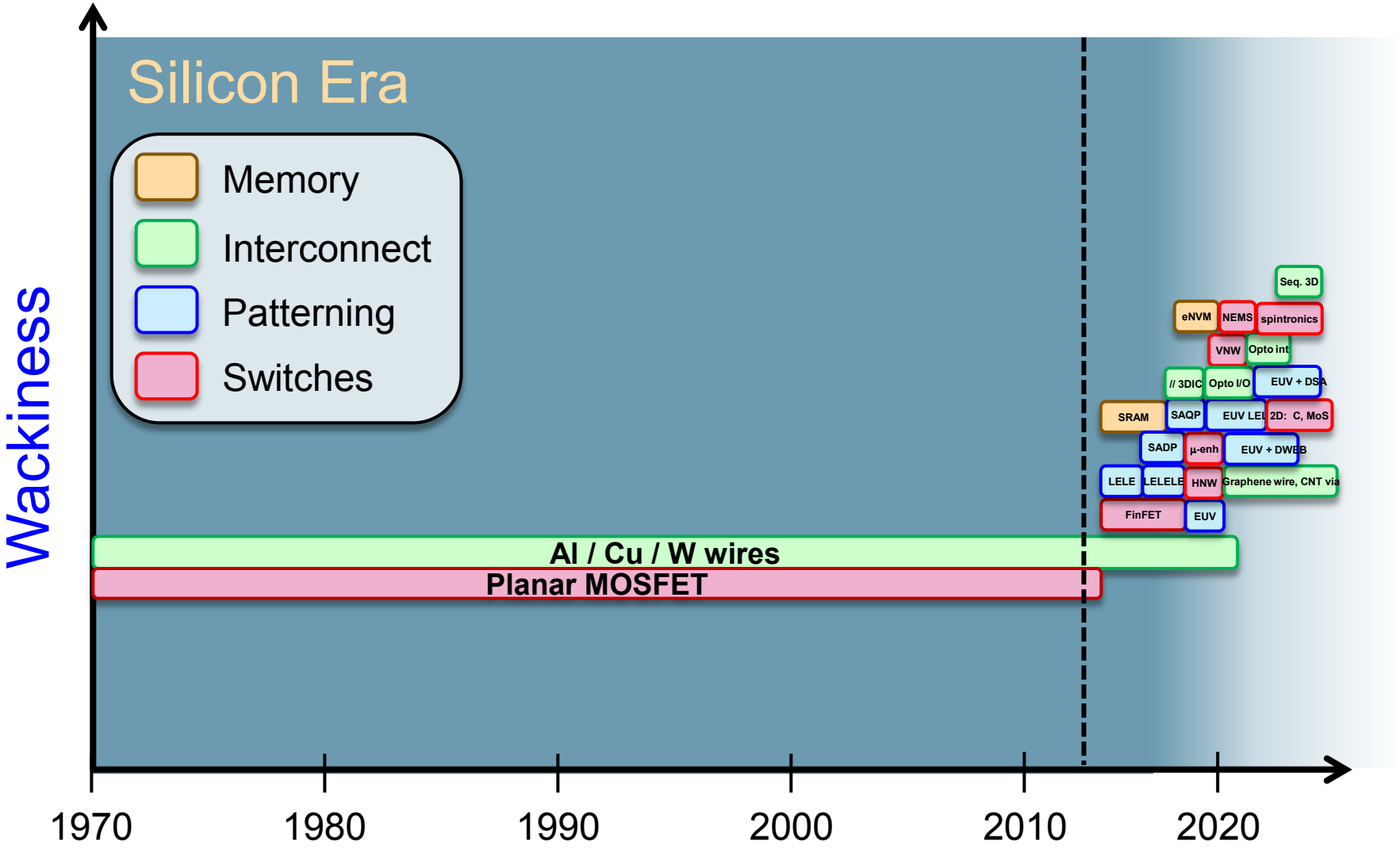
Node	45nm	20nm	10nm
Year	2009	2013	2017
Area	1	~1/4	~1/16
Peak freq	1	1.6	2.4
Power			
@ 45nm freq	1	0.6	0.3
@ peak freq	1	1	0.6



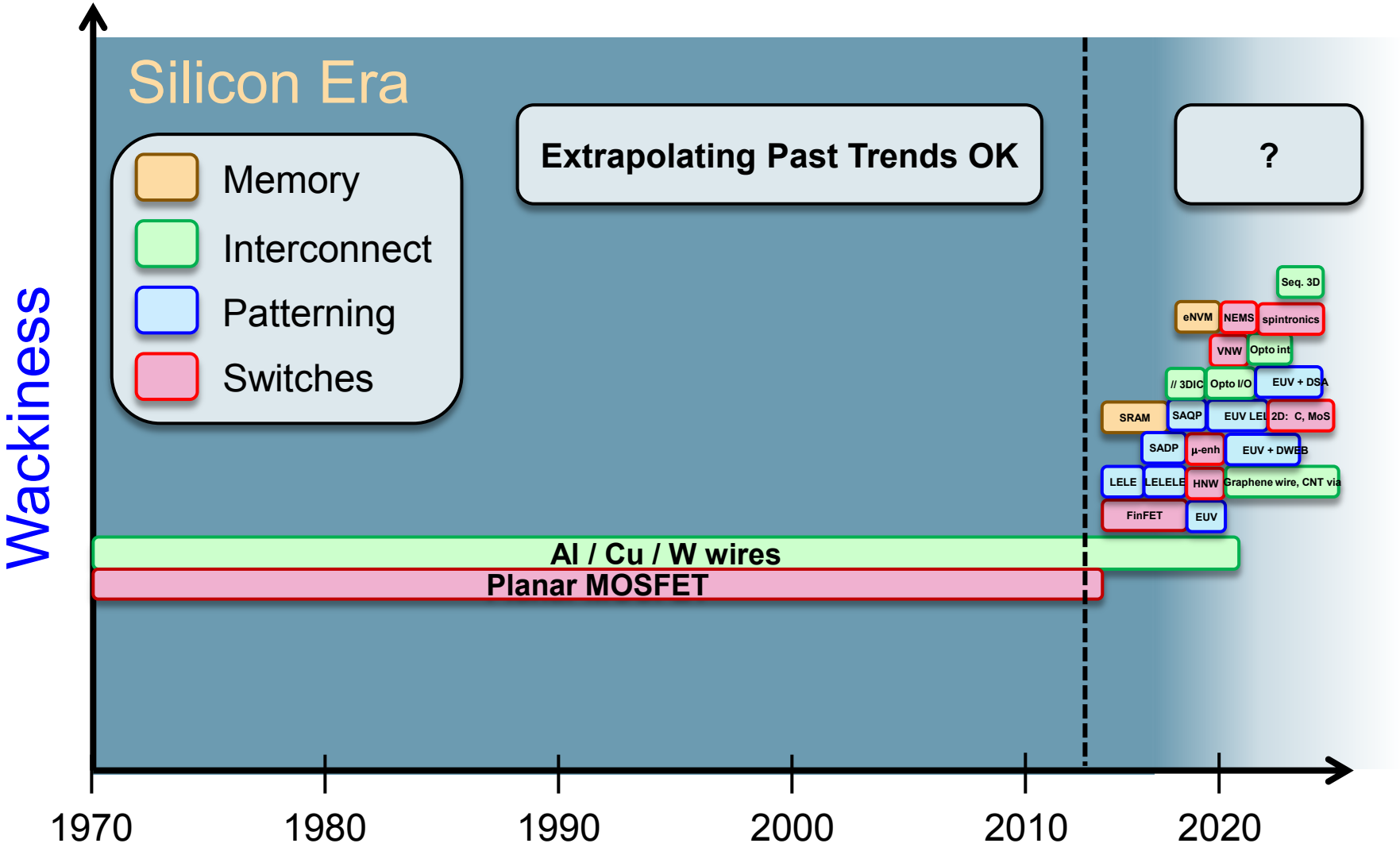
Exploitable Si
(equivalent Power)

Note: Precise scaling details don’t matter as much as the general observation

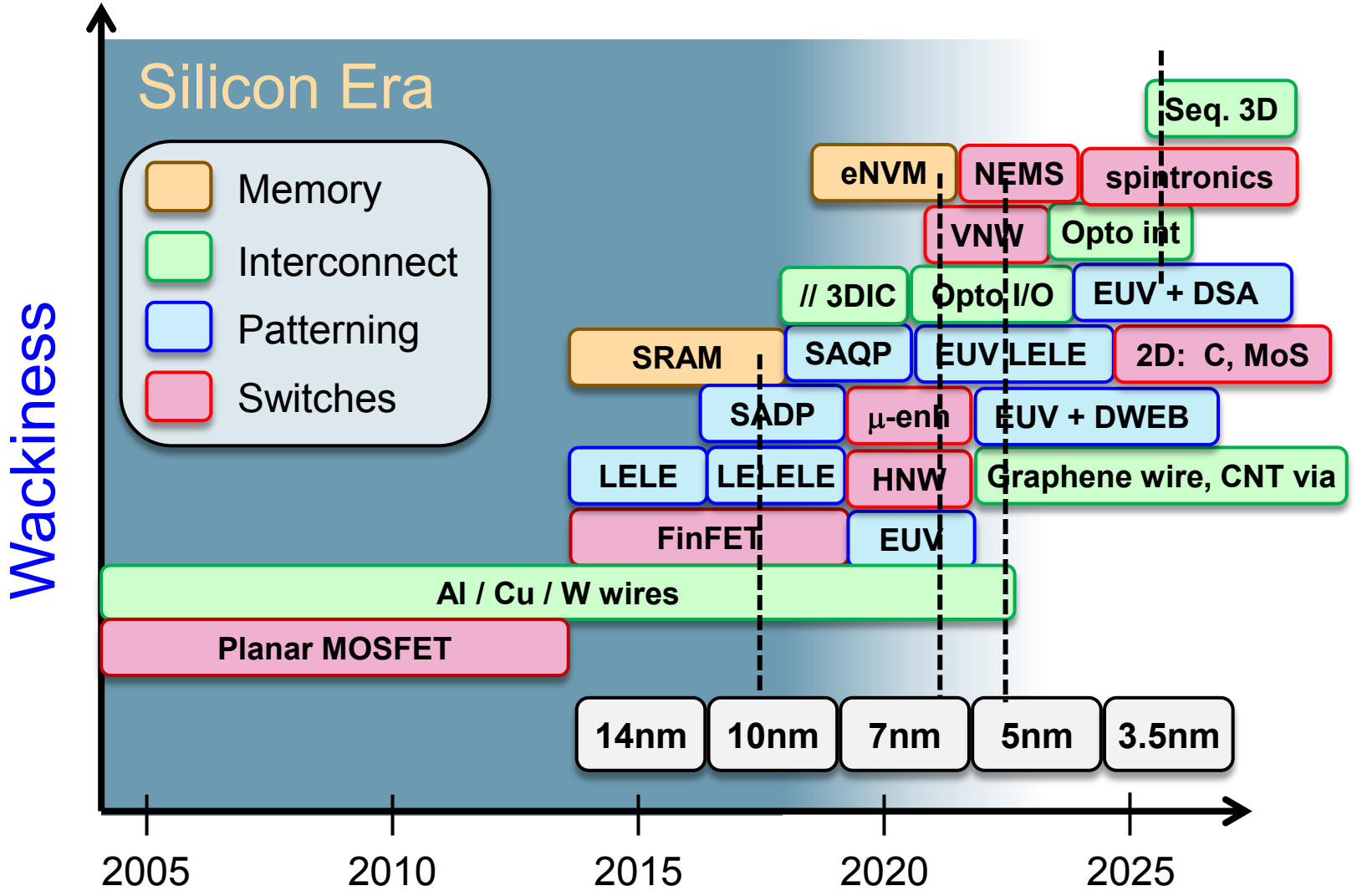
“Silicon” Device Roadmap



“Silicon” Device Roadmap



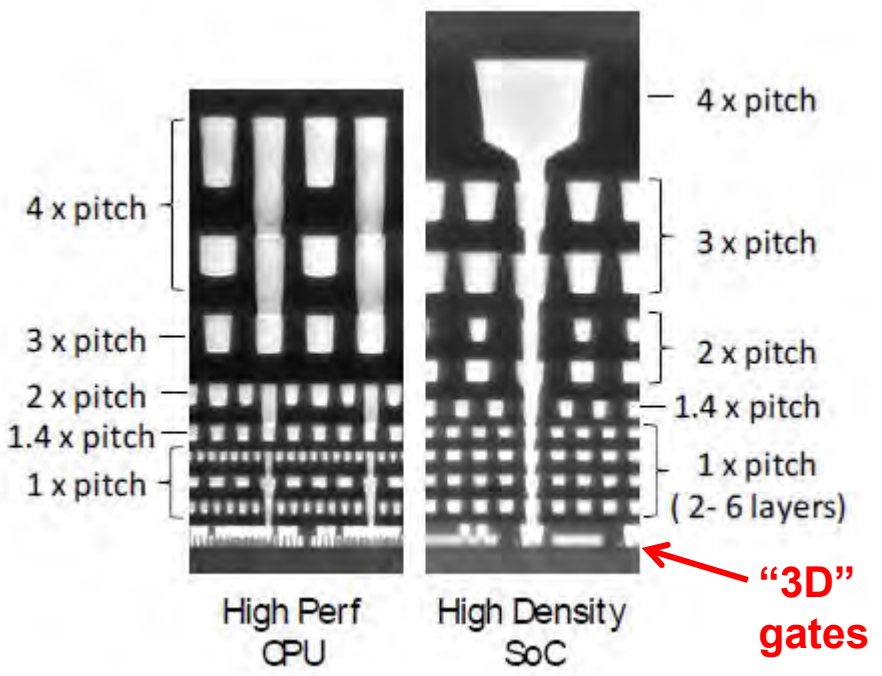
“Silicon” Device Roadmap



Sources: ITRS, IEDM, public statements, ARM speculation

Metal Stack

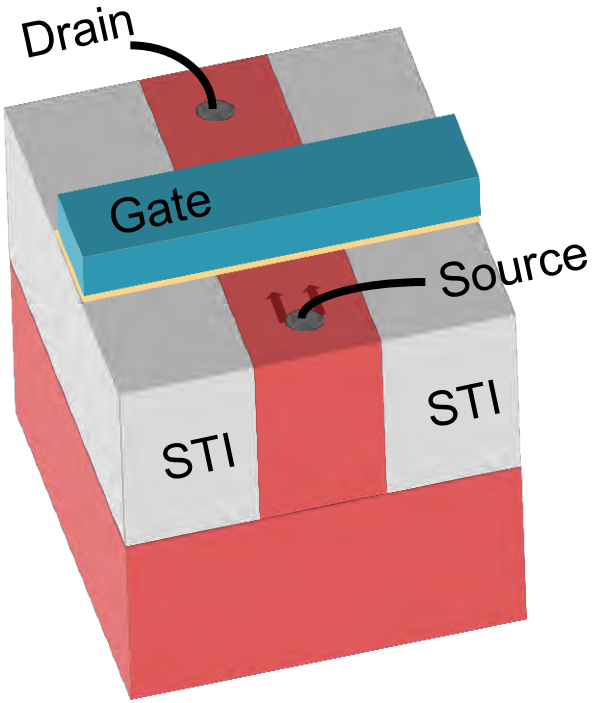
- FinFETs have significantly better current drive capability than bulk devices
  - Also higher gate capacitance
- Still a big chunk of capacitance in wiring
- RC of contacting layers also important

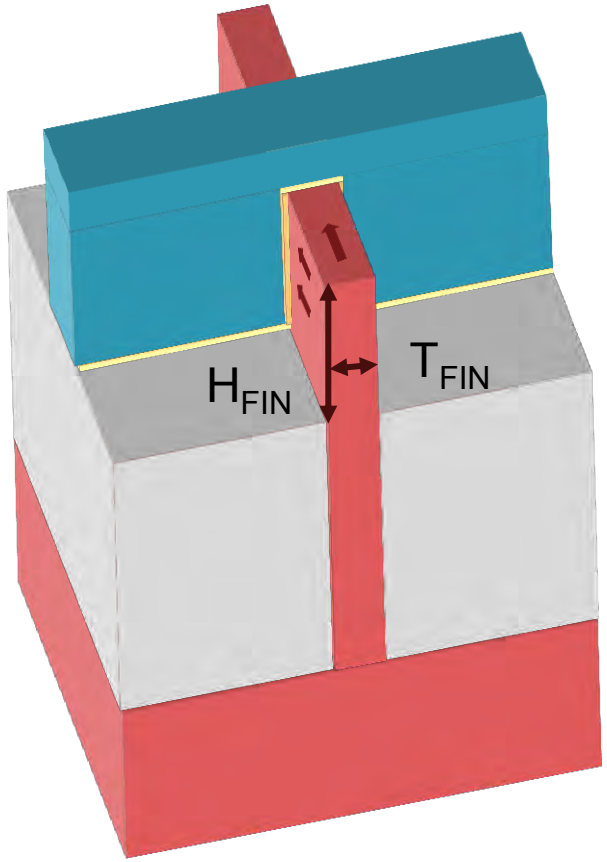


Jan et al, IEDM 12

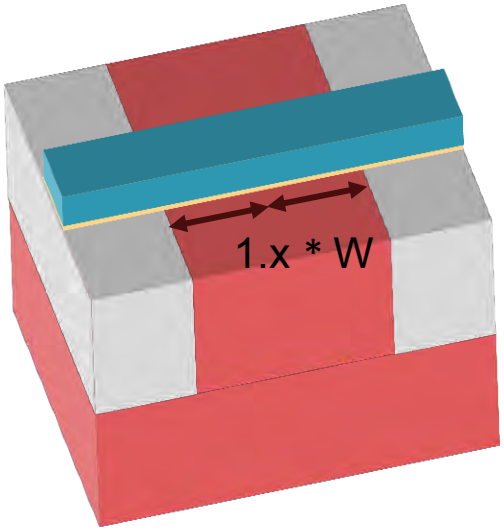
3-Sided Gate

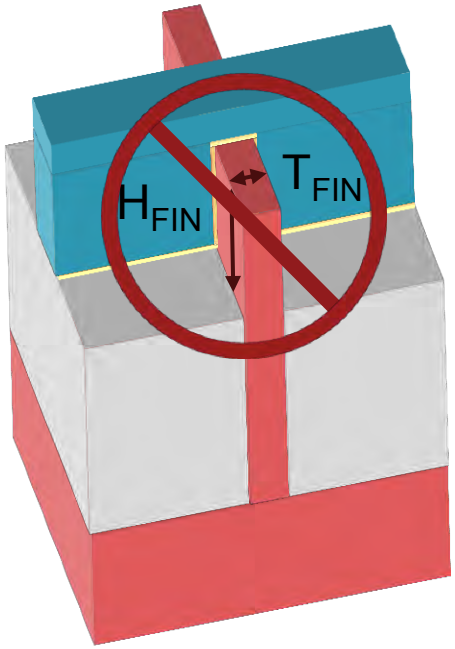
$$W_{FINFET} = 2*H_{FIN} + T_{FIN}$$





Width Quantization





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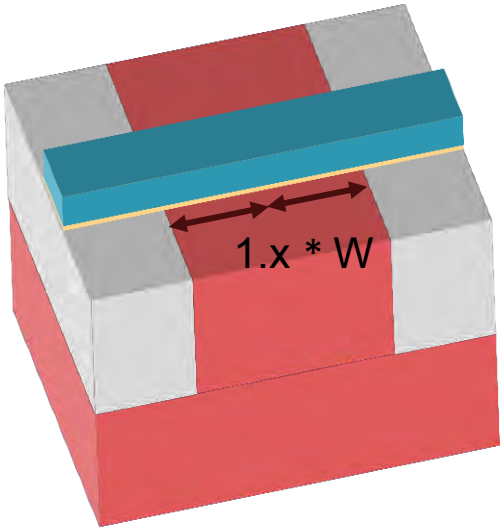
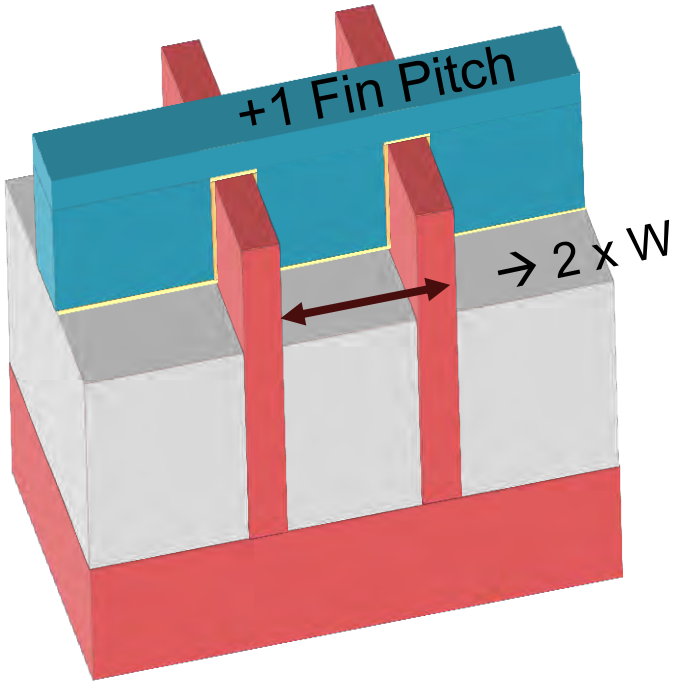
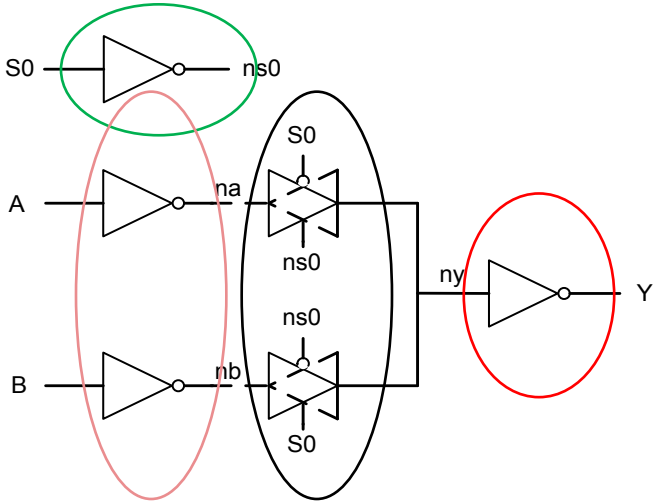
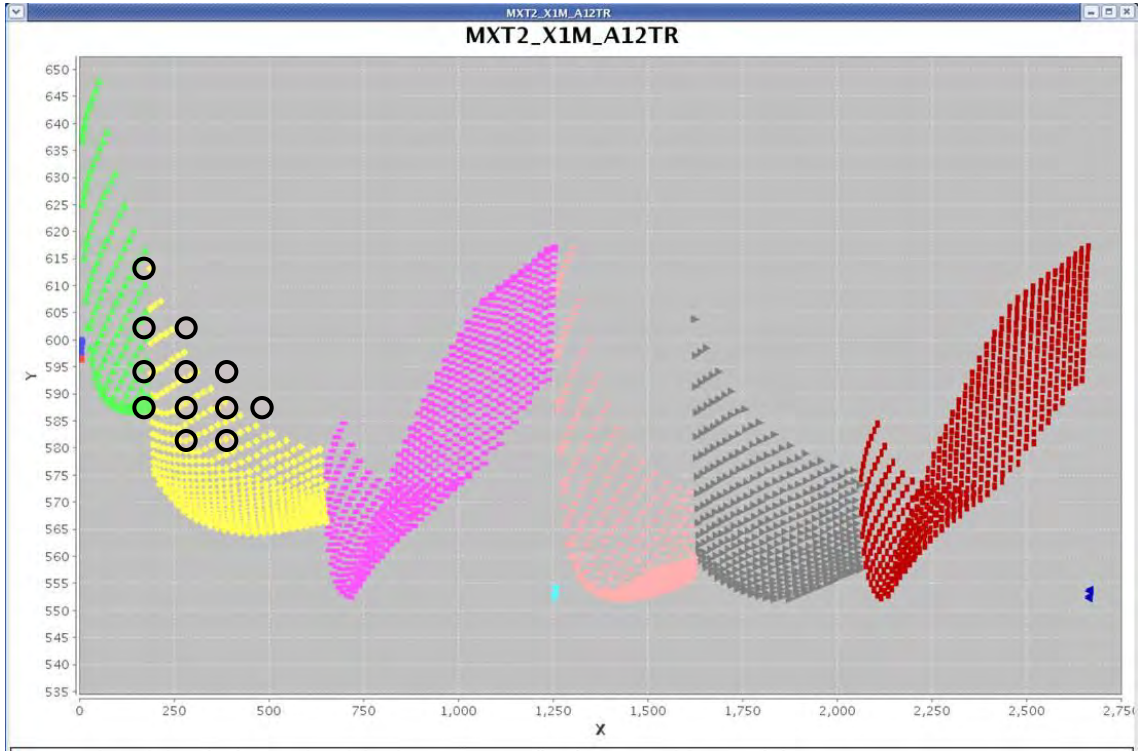




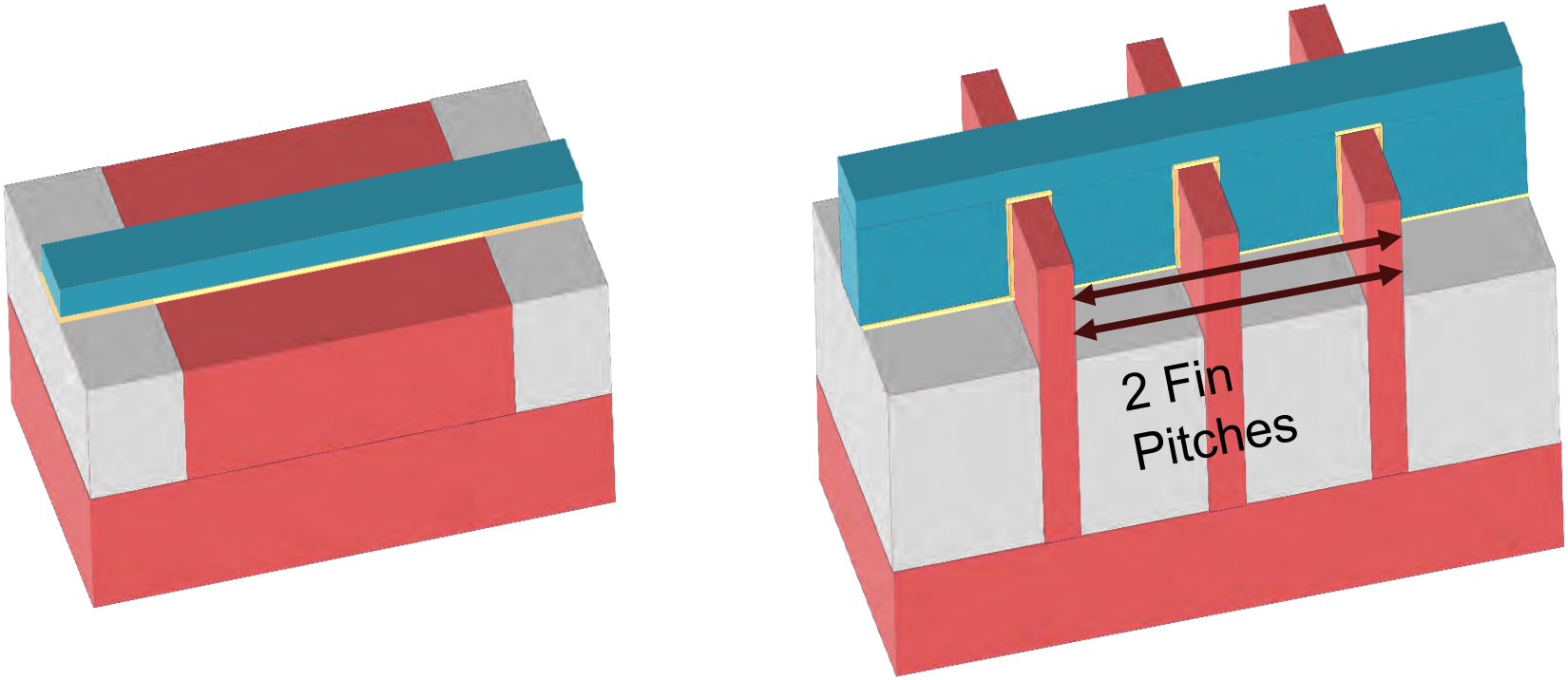
Width Quantization and Circuit Design

- Standard cell design involves complex device sizing analysis to determine the ideal balance between power and performance





3D Factor



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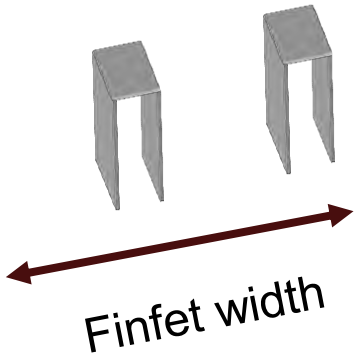
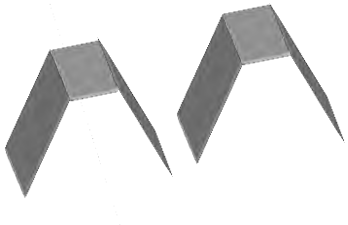


3D Factor



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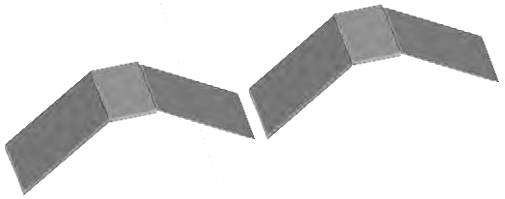
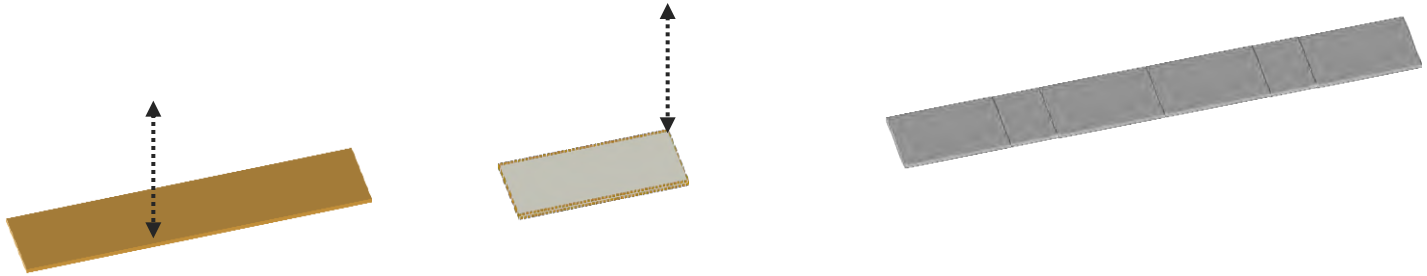
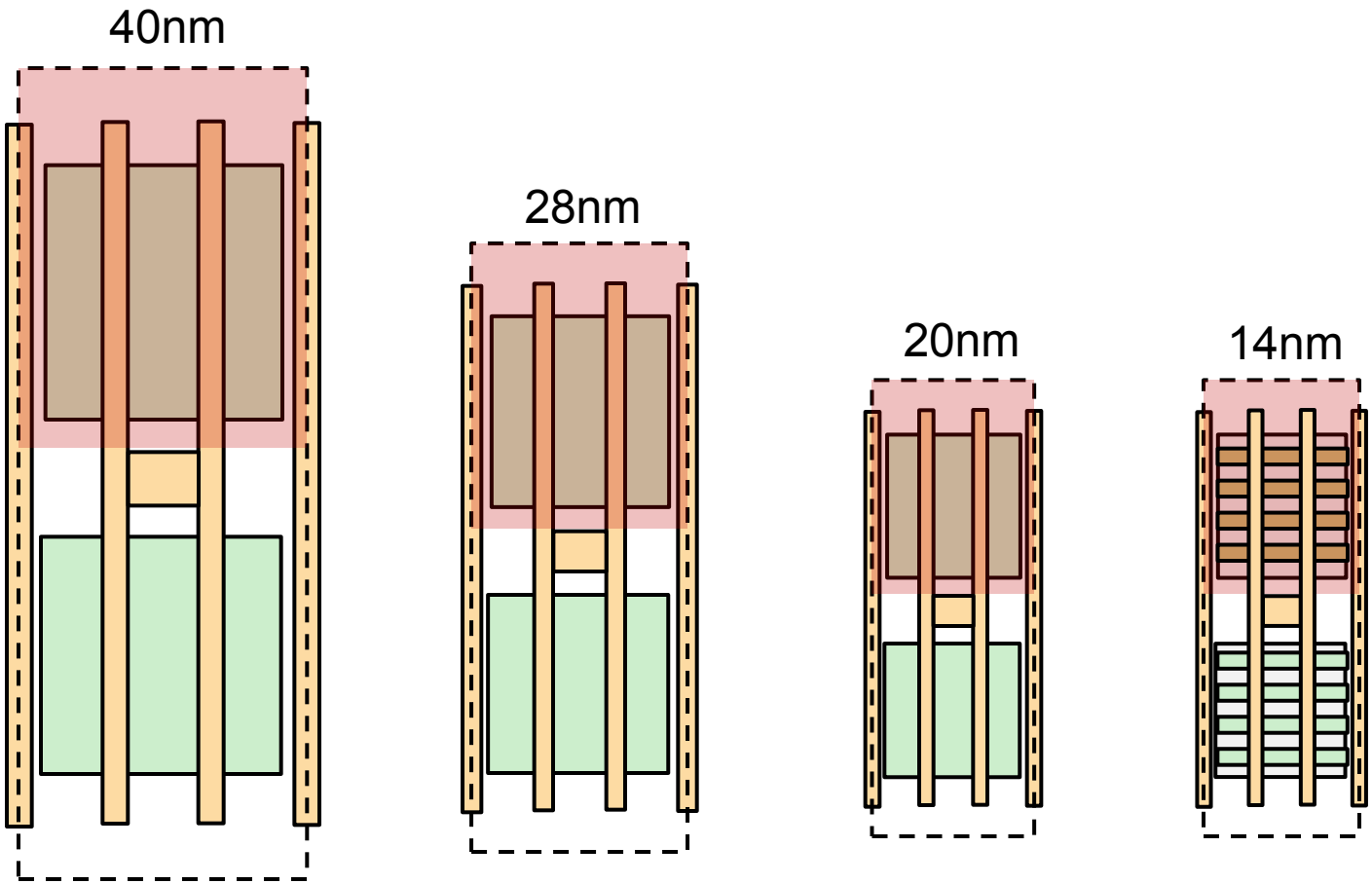


3D Factor



$$\text{3D Factor} = \frac{\text{Total width of FinFET}}{\text{Planar width used}} = \frac{2 \times H_{FIN} + T_{FIN}}{\text{Fin Pitch}}$$

Standard Cell Transistor Widths



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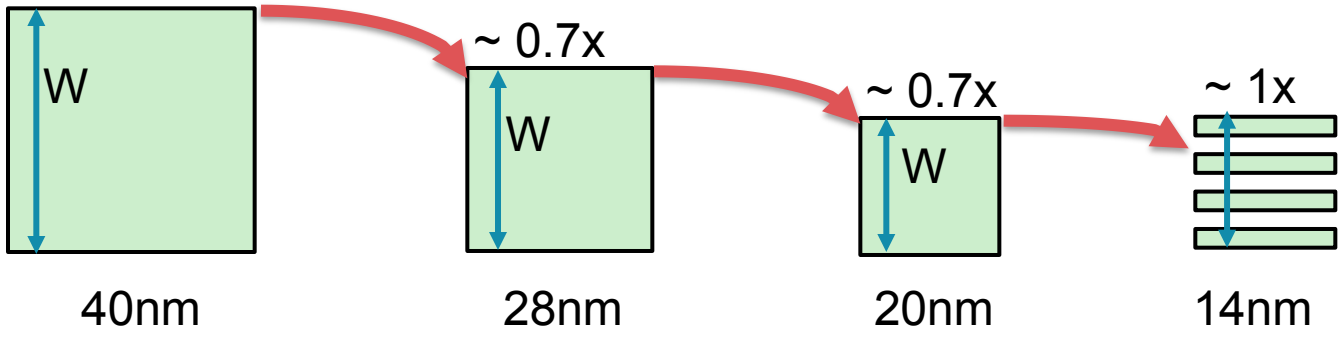

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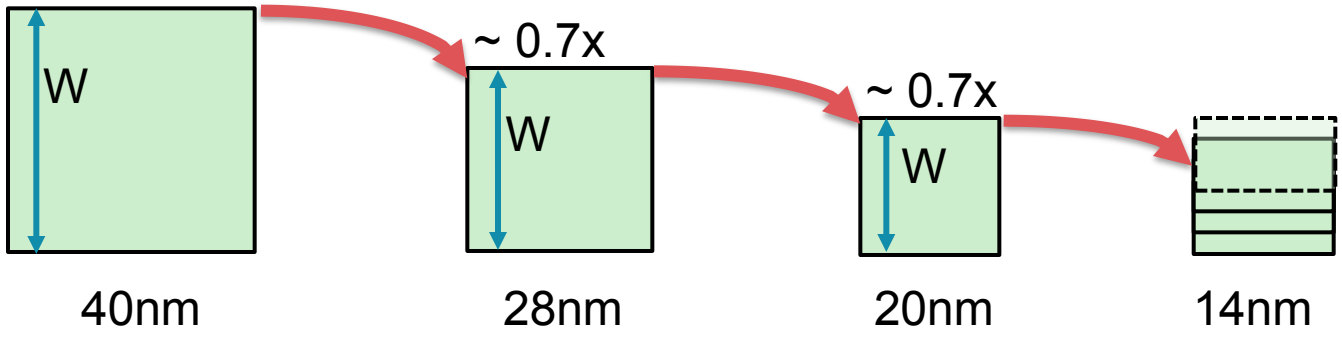

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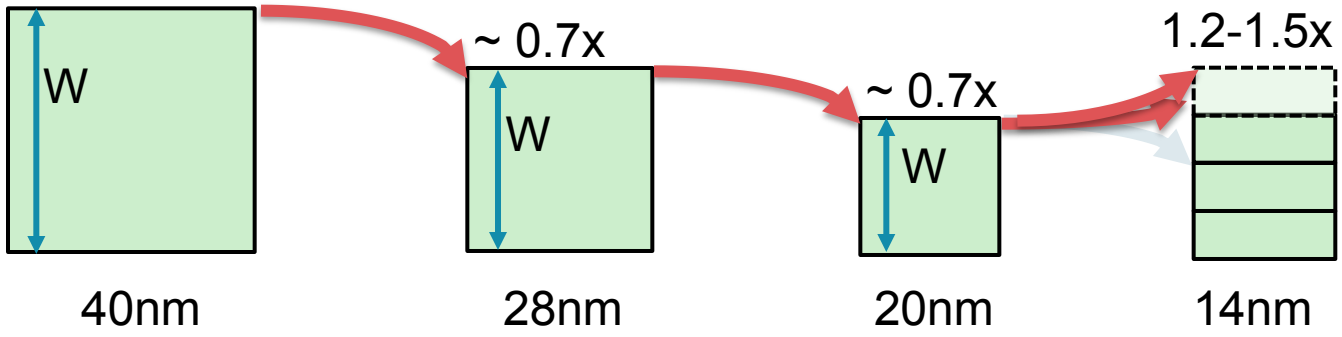
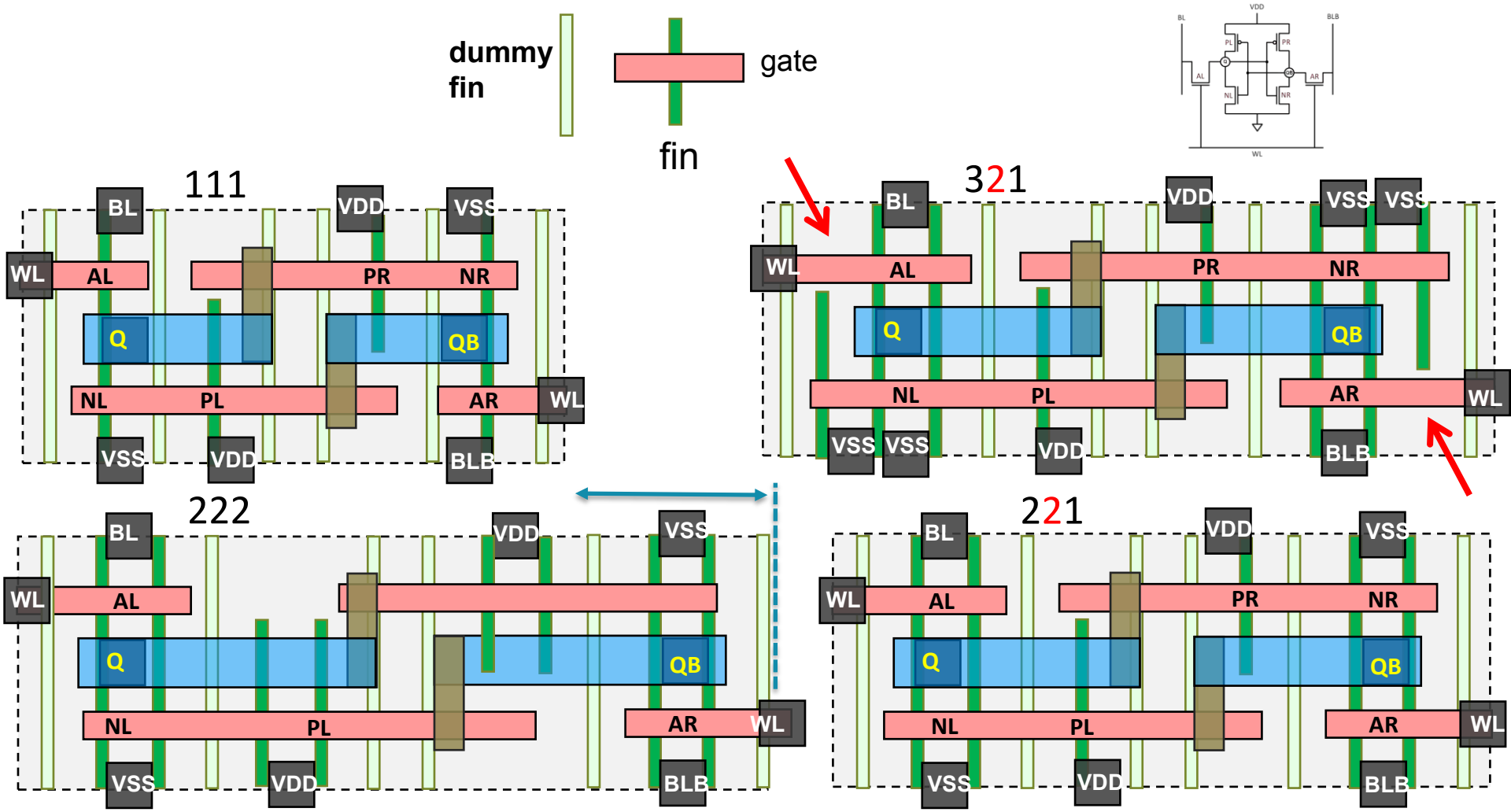


FinFET Designer's Cheat Sheet

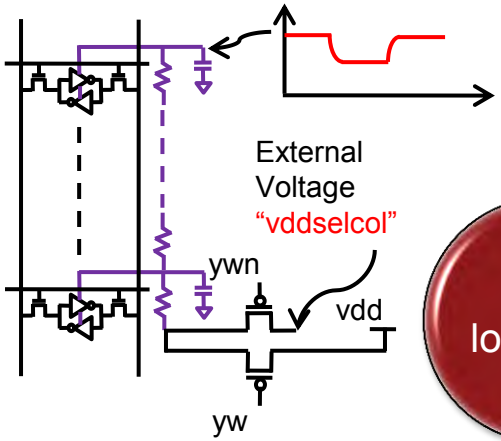
- Fewer Vt, L options
- New variation signatures
  - Some local variation will reduce
    - Local/Global balance is designer's opportunity
    - xOCV derates will need to reduce
    - Better tracking between device types
    - Reduced Inverted Temperature Dependence
- Little/no body effect
  - FinFET 4-input NAND ~ planar 3-input NAND
  - More complex cells / Higher fan-in (?)
- Paradigm shift in device strength per unit area
  - Get more done locally per clock cycle
  - Watch the FET/wire balance
  - Expect better power gates
  - Watch your PDN and EM!

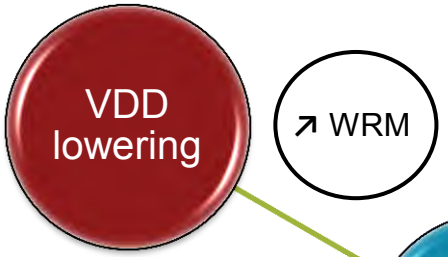
FinFET bit cells: Discrete Options



Note: Conceptual cell layout, not foundry specific

Assist Required for Most Cells





↗ WRM

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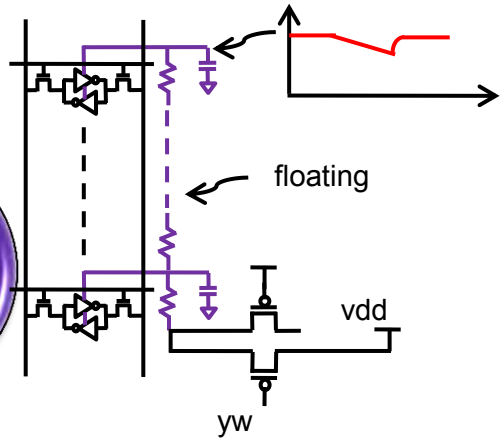
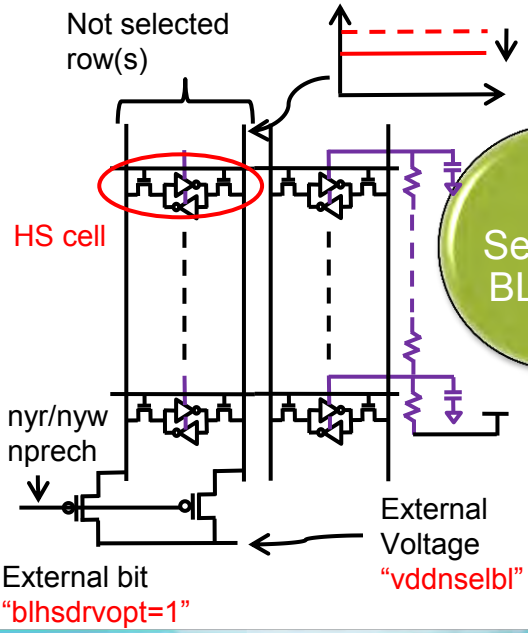


External bit
"colfloatopt=1"



External bit
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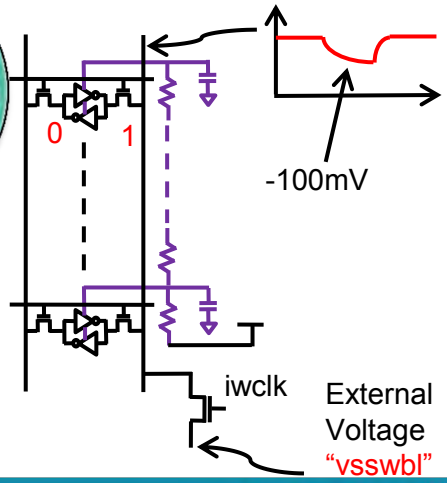
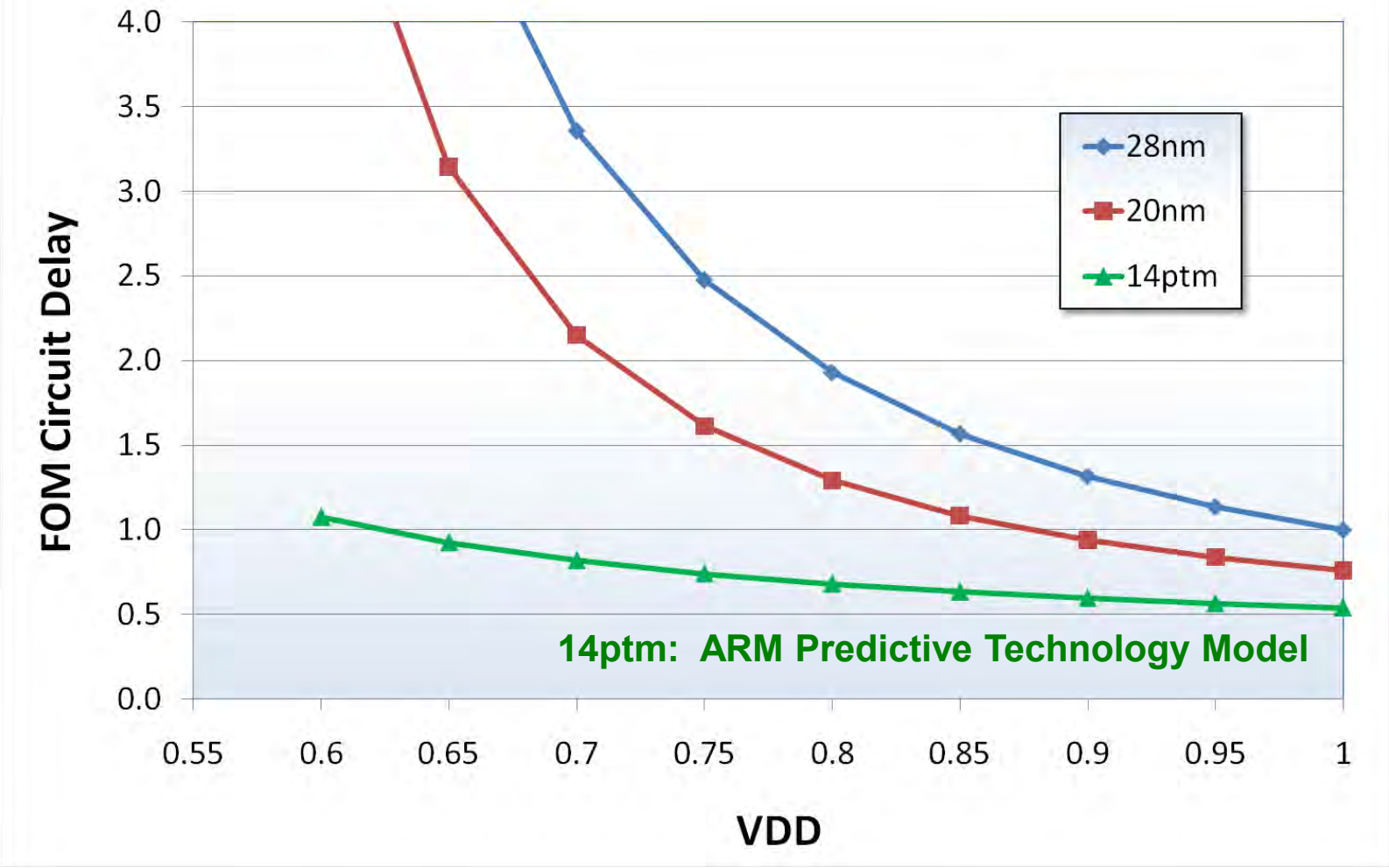
↗ ADM

↗ WRM

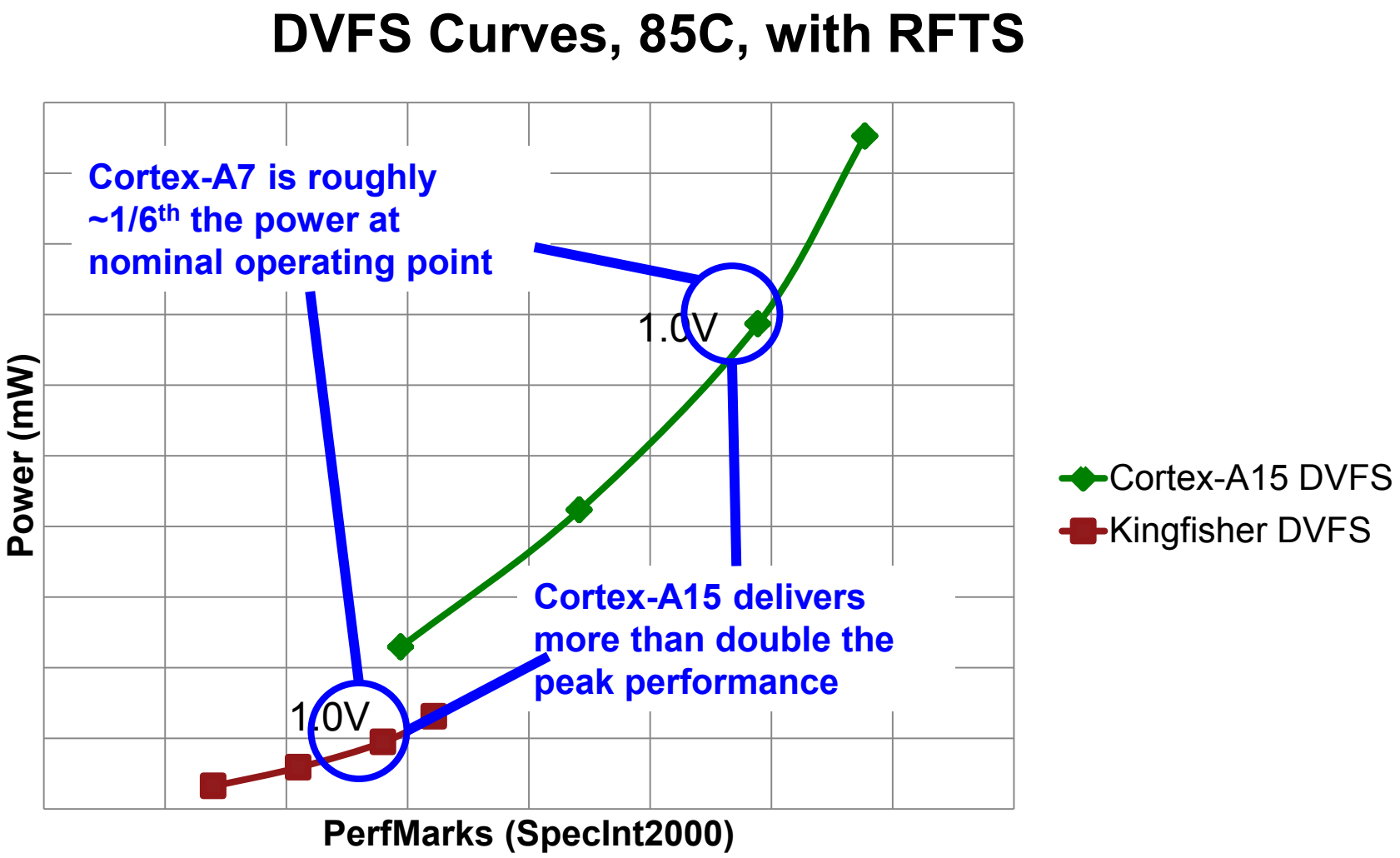


FinFET and Reduced VDD



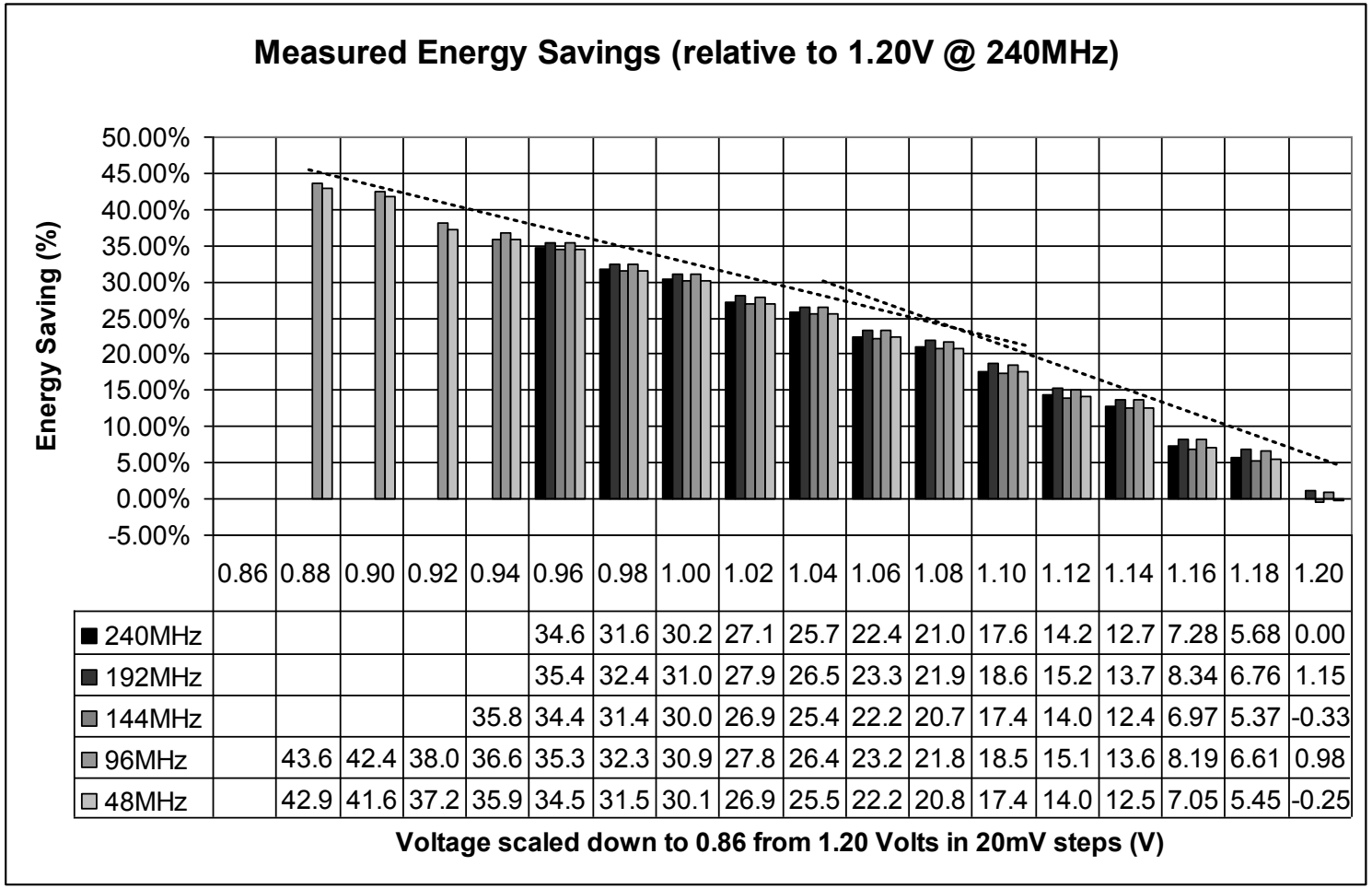
FOM ➔ “Figure of Merit” representative circuit

Big-Little Optimized Solution with DVFS



The Good Old Days of DVFS

- Measured energy savings with DVS at 65LP
  - RAM voltage headroom requires 1.08V…



	0.86	0.88	0.90	0.92	0.94	0.96	0.98	1.00	1.02	1.04	1.06	1.08	1.10	1.12	1.14	1.16	1.18	1.20
240MHz						34.6	31.6	30.2	27.1	25.7	22.4	21.0	17.6	14.2	12.7	7.28	5.68	0.00
192MHz						35.4	32.4	31.0	27.9	26.5	23.3	21.9	18.6	15.2	13.7	8.34	6.76	1.15
144MHz					35.8	34.4	31.4	30.0	26.9	25.4	22.2	20.7	17.4	14.0	12.4	6.97	5.37	-0.33
96MHz		43.6	42.4	38.0	36.6	35.3	32.3	30.9	27.8	26.4	23.2	21.8	18.5	15.1	13.6	8.19	6.61	0.98
48MHz		42.9	41.6	37.2	35.9	34.5	31.5	30.1	26.9	25.5	22.2	20.8	17.4	14.0	12.5	7.05	5.45	-0.25

Summary

- FinFETs cause substantial changes in physical IP design but their effect can mostly be hidden from higher levels
  - Especially when combined with litho needs
- Other devices will be needed in the future, their effect may be more pronounced
- Designers can best take advantage of improved performance by working at lower voltages