

FOUNDRY DAY: FINFET DESIGN ENABLEMENT

Daniel Nenni, SemiWiki

- *Introduction and FinFET Value Proposition*

Tom Dillinger, Oracle

- *FinFET Primer and Parasitics*

Rob Aitken, ARM

- *FinFET SoC Design Challenges*

Raymond Leung, Synopsys

- *FinFET SRAM Design Challenges*

Tom Quan, TSMC

- *FinFET Design Ecosystem Challenges*



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Semiconductor Power Crisis ISSCC 2011

“New transistor designs are part of the answer,” said Dr. Jack Sun. “Options include a design called FinFET, which uses multiple gates on each transistor.”

“Researchers have made great progress with FinFET, and TSMC hopes it can be used for the next generation of CMOS -- the industry's standard silicon manufacturing process.”



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SEMIWIKI TRAFFIC REPORT

FinFETs #1 Trending Term for 2012

1,283,590 people visited this site



■ **20.90% Search Traffic**
268,325 Visits

■ **50.77% Referral Traffic**
651,679 Visits

■ **28.28% Direct Traffic**
362,968 Visits

■ **0.05% Campaigns**
618 Visits



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FINFET DESIGN CHALLENGES

- Scaling layout and circuit design
- Power density per unit area increase
- New layout dependent effects
- New sources of process variation
- New analog structures required
- FinFET Bulk versus FinFET SOI
- New EDA tool challenges:
 - Extraction, EM, Thermal modeling



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FINFET ADDED COMPLEXITIES

Design Rule Manuals:

- 700 rules @ 90nm
- 800 rules @ 65nm
- 1,200 rules @ 40nm
- 1,900 rules @ 28nm
- 3,000 rules @ 20nm
- 3,400 rules @ 16nm



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FINFET ADDED COMPLEXITIES

DRC Deck Sizes:

- Just under 20,000 @ 90nm
- Just over 20,000 @ 65nm
- Just under 30,000 @ 40nm
- Just over 40,000 at 28nm
- Right on 80,000 at 20nm
- Just under 100,000 @ 16nm



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FINFET VALUE PROPOSITION VERSUS PLANAR

Performance: +10-20% @ same power

Power: -25-40% @ same performance

Area: Comparable to planar

Cost: Comparable to planar



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