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CONSULTING IN ELECTRONIC DESIGN

ITRS 2013
Silicon Platforms + Virtual Platforms = An explosion in SoC design

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ELECTRONIC DESIGN STRATEGY & MARKET ANALYSIS

The Five Design Constraints

- Frequency
- Power
- Gate Count
- Design time
- Cost of design
- Cost of the packaged SoC

What Happened to Performance ?

- The old view “Frequency = Performance”.
  - **Frequency is still a constraint but –**
- Today’s view Performance = Latency plus Power
- Customer view of Performance = Available Applications
  - **Gate count**

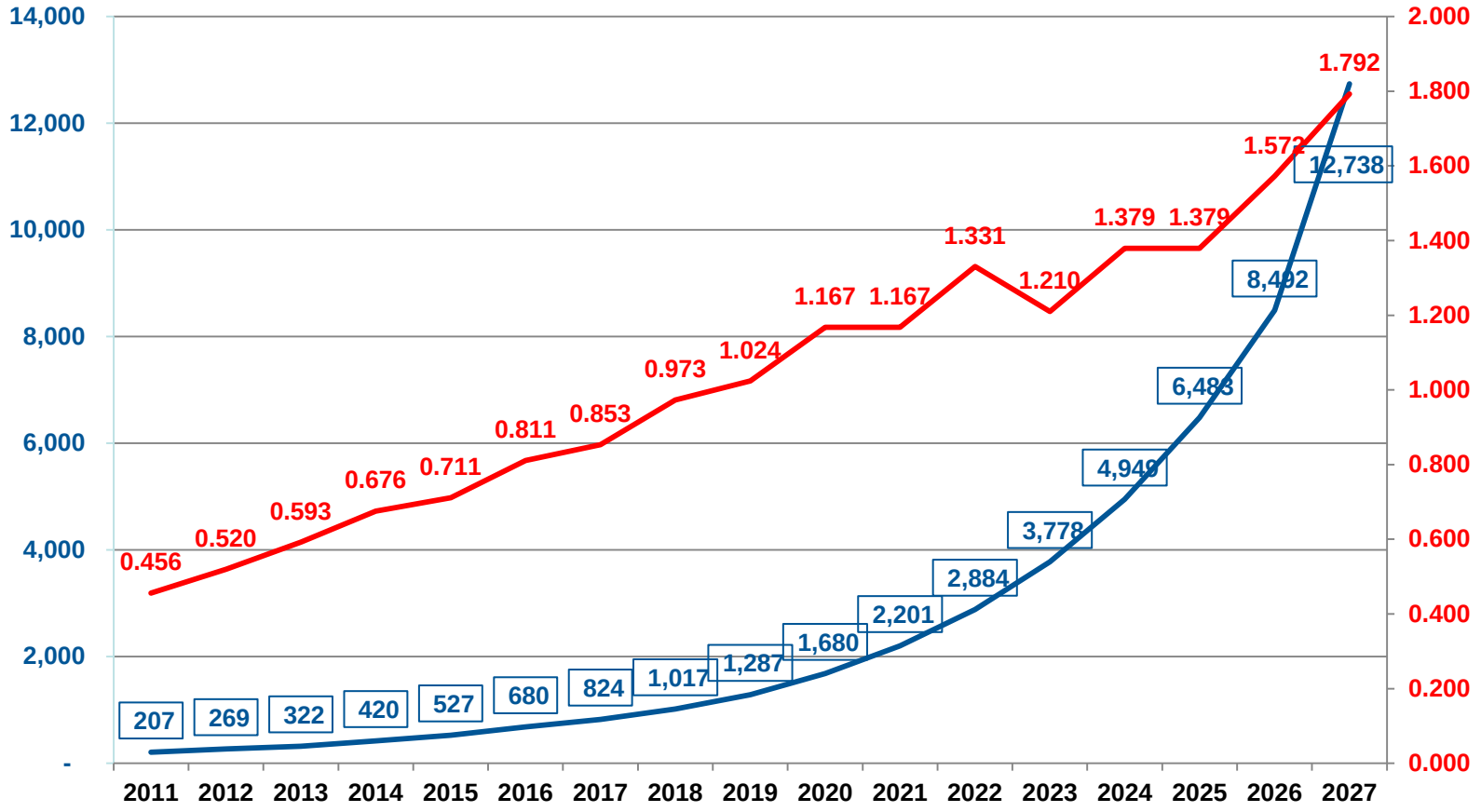
Improving Power's Impact on Design

Table DESN14 Low-Power Design Technology Improvements and Impact on Dynamic and Static Power

Software Virtual Prototype	2011	123%	120%	Virtualization tools to allow the programmer to develop software prior to silicon
Frequency Islands	2013	126%	100%	Designing blocks that operate at different frequencies
Extreme Power Gating	2015	90%	100%	Shutting down applications (Dark Silicon)
Hardware/Software Co-Partitioning	2017	118%	100%	Hardware/software partitioning at the behavioral level based on power
Heterogeneous Parallel Processing (AMP)	2019	118%	100%	Using multiple types of processors in a parallel computing architecture
Many Core Software Development Tools	2021	120%	100%	Using multiple types of processors in a parallel computing architecture
Power-Aware Software	2023	121%	100%	Developing software using power consumption as a parameter
Near-Threshold Computing	2025	123%	80%	Lowering Vdd to 400 - 500 mV
Asynchronous Design	2027	121%	100%	Total Non-clock driven design

Source: ITRS 2012

Gates & Frequency
(5 watts max)



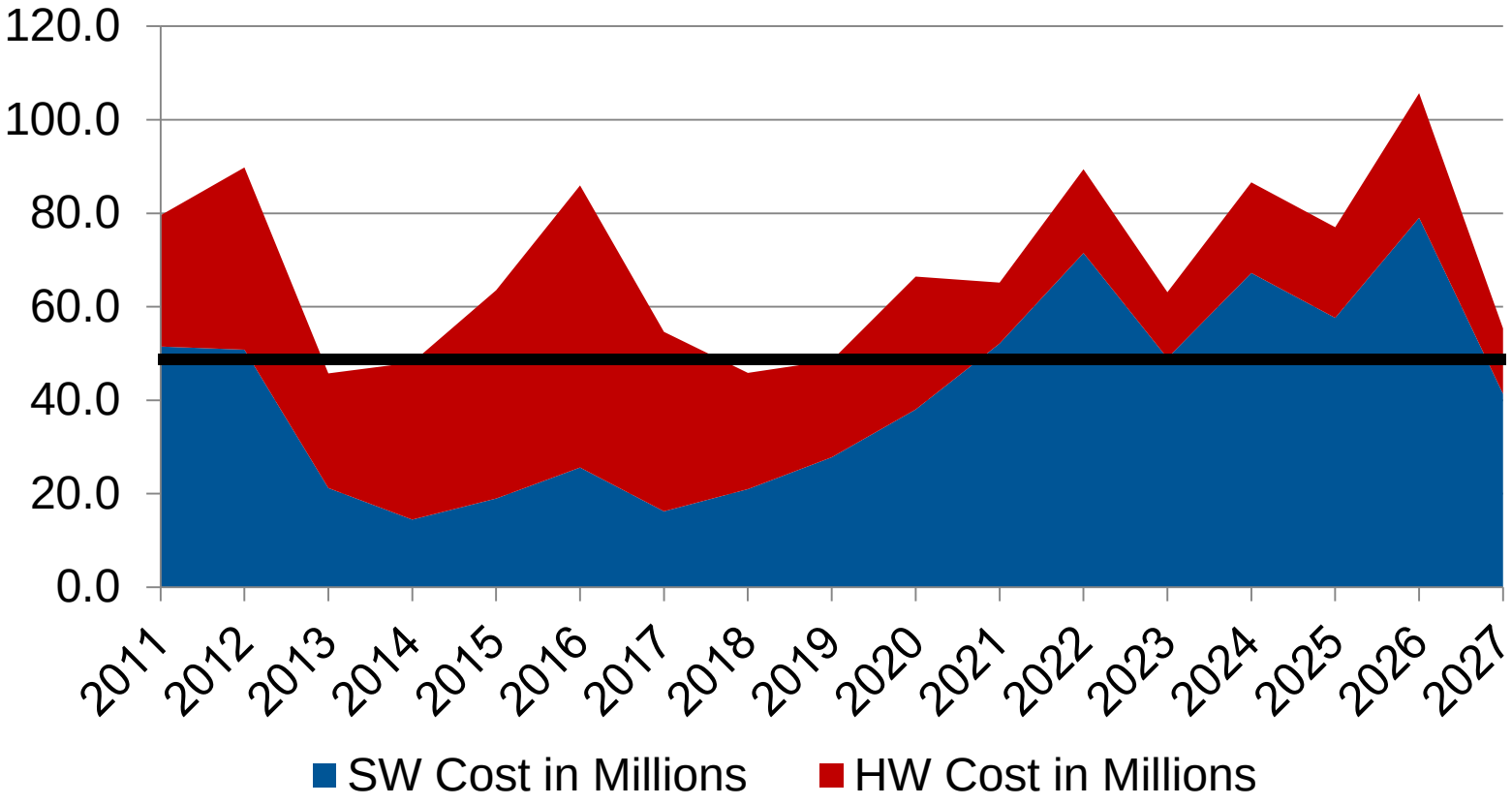
Max Usable Gates do to Power Constraints

- In 2011 we could use 39% of the available gate count.
- By 2026 we are up to 93% of the available gates, as long as we can accomplish the required improvements.
- But now we need to look at cost.

Improvements on Design Productivity

DT Improvement	*Year*	*Productivity Delta*	*Productivity (Gates/Year/Designer)*	*Cost Component Affected*	*Description of Improvement*
Software Virtual Prototype	2011	300% SW	1200K HW, 2584K SW	SW development	Virtualization tools used to allow development prior to completed silicon
Intelligent Testbench	2012	37.5% HW	1650K HW, 2584K SW	System design and verification	Like RTL verification tool suite, but also with automation of the verification partitioning step
Reusable Platform Blocks	2013	200% HW, 100% SW	4949K HW, 5168K SW	Chip/circuit/PD verification	Fully functional platforms used as a block in larger platform design (e.g., ARM in OMAP)
Silicon Virtual Prototype	2015	100% HW	9897K HW, 5168K SW	System design and verification	A hardware virtualization platform that enables an RTL handoff of a SOC
Heterogeneous (AMP) Parallel Processing	2017	100% HW, 100% SW	19794K HW, 10336K SW	SW development verification	Many specialized cores provide processing around a main processor, which allows for performance, power efficiency, and high reuse
Transactional Memory	2018	60% SW		SW Development	Automaticaly handles locks and unlocks.
Many-Core SW Development Tools	2019	60% SW	19794K HW, 16537K SW	SW development	Enables compilation and SW development in highly parallel processing SOCs
Parallel SW Language	2021	200% SW		SW development	Laguages specifically designed for parallel programing.
Suoer Computer Class Servers	2023	100% HW 75% SW		HW & SW Design and Development	Parallel computing specialised for the application and computer language.
System-Level Design Automation (SDA)	2025	60% HW, 37.5% SW	31671K HW, 45476K SW	System design and verification	Automates true system design on- and off-chip for the first time, including electronic, mechanical and other heterogeneous technologies
Executable Specification Source: ITRS 2012	2027	200% HW, 200% SW	95013K HW, 136429K SW	System design and verification	Describes the system specification in a manner that allows automated design and validation

Max Usable Gates at 5 Watts - Cost

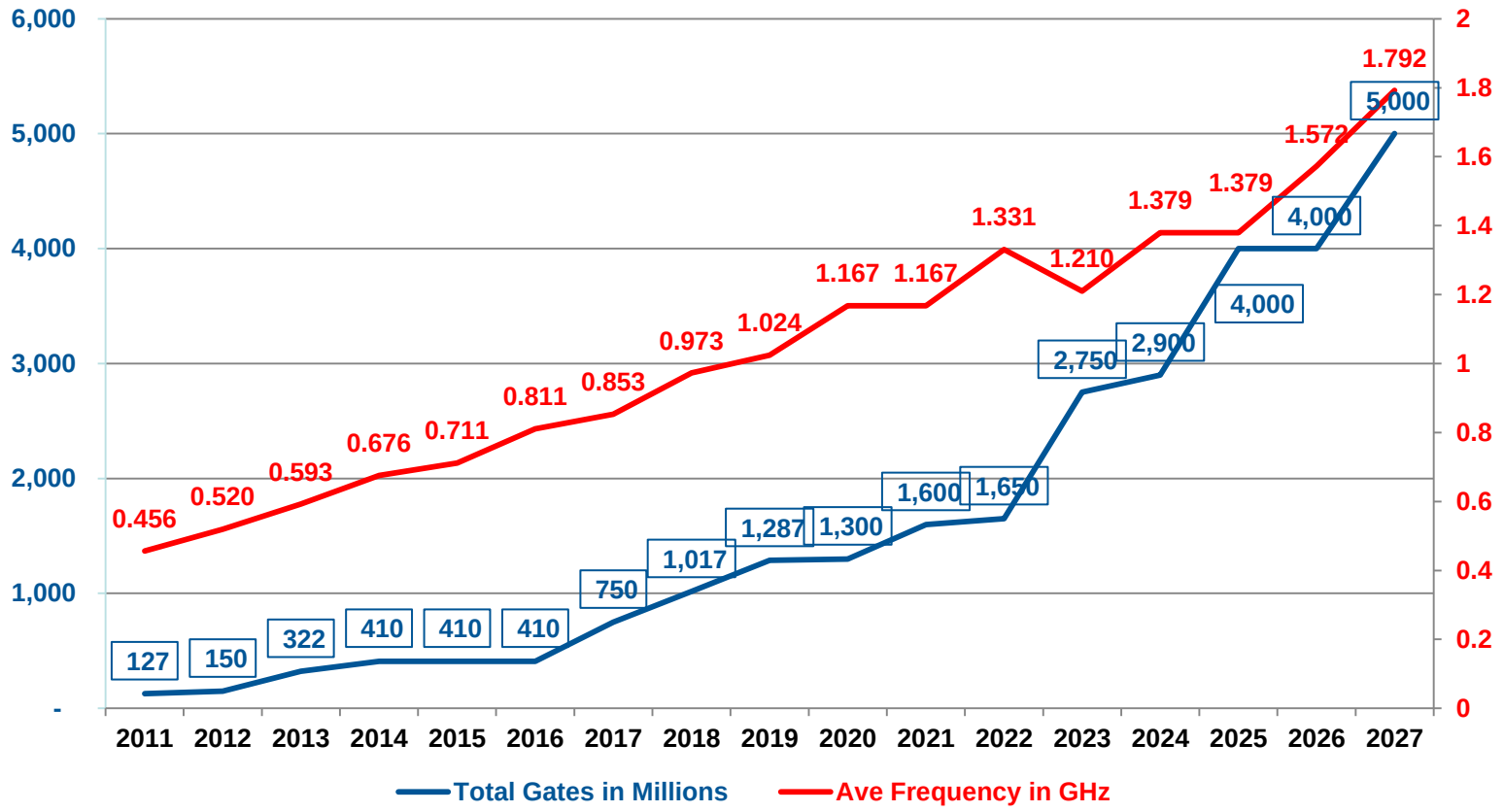


Source: ITRS 2012

Cost of a 5 watt Mobile SoC Design

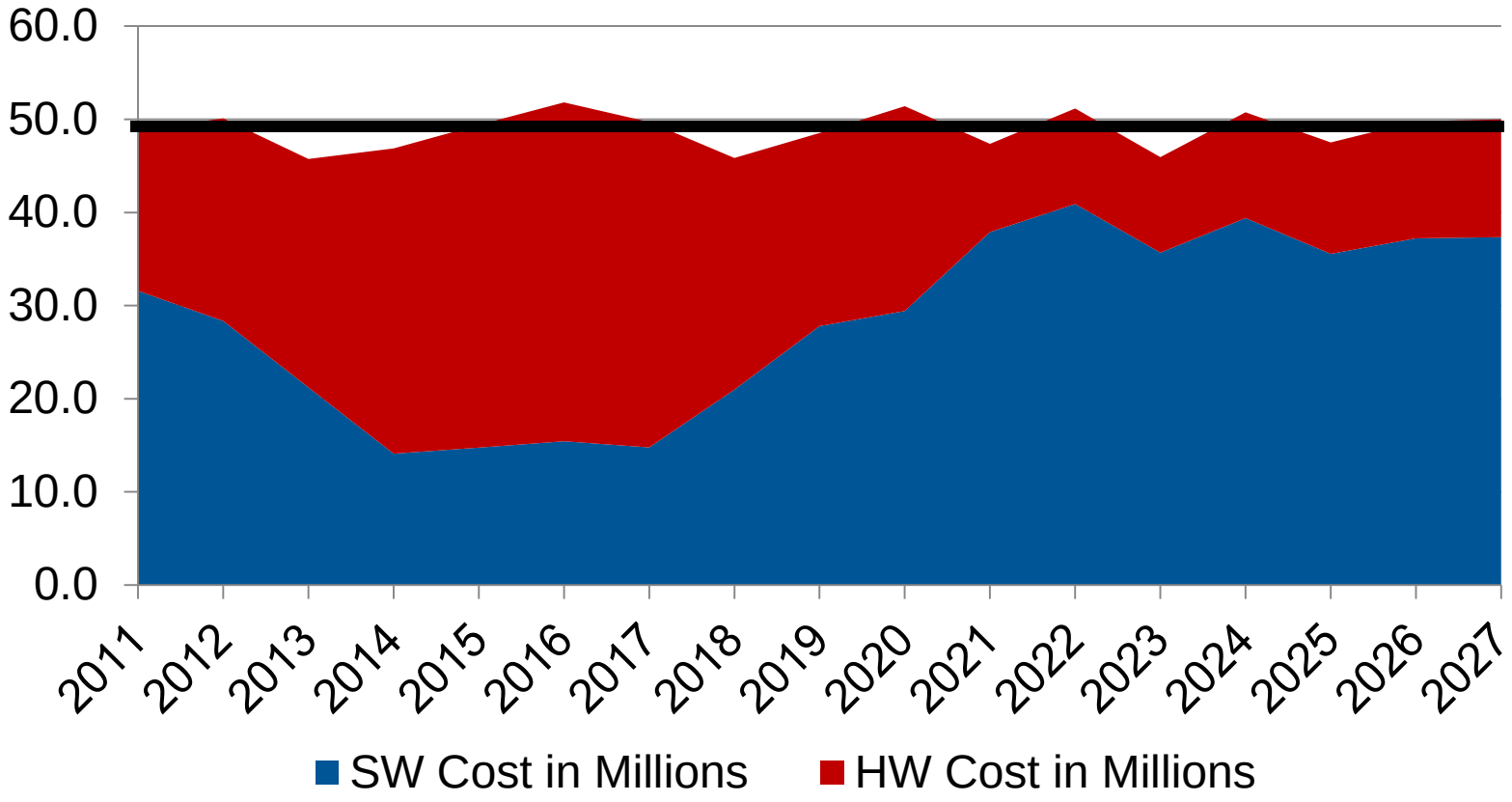
- Only four times in 17 years will we be able to meet our $50,000,000 goal for a large semiconductor company design.
- We aren't even close to meeting the $25,000,000 goal for a VC funded Start-Up design.
- So if we can't use the maximum allowable gate count, for our Power Budget, what can we do ?

Gates & Frequency @ $50m (5 watts max)



Source: ITRS/Gary Smith EDA 2012

Max Usable Gates at 5 Watts - @ $50m Cost



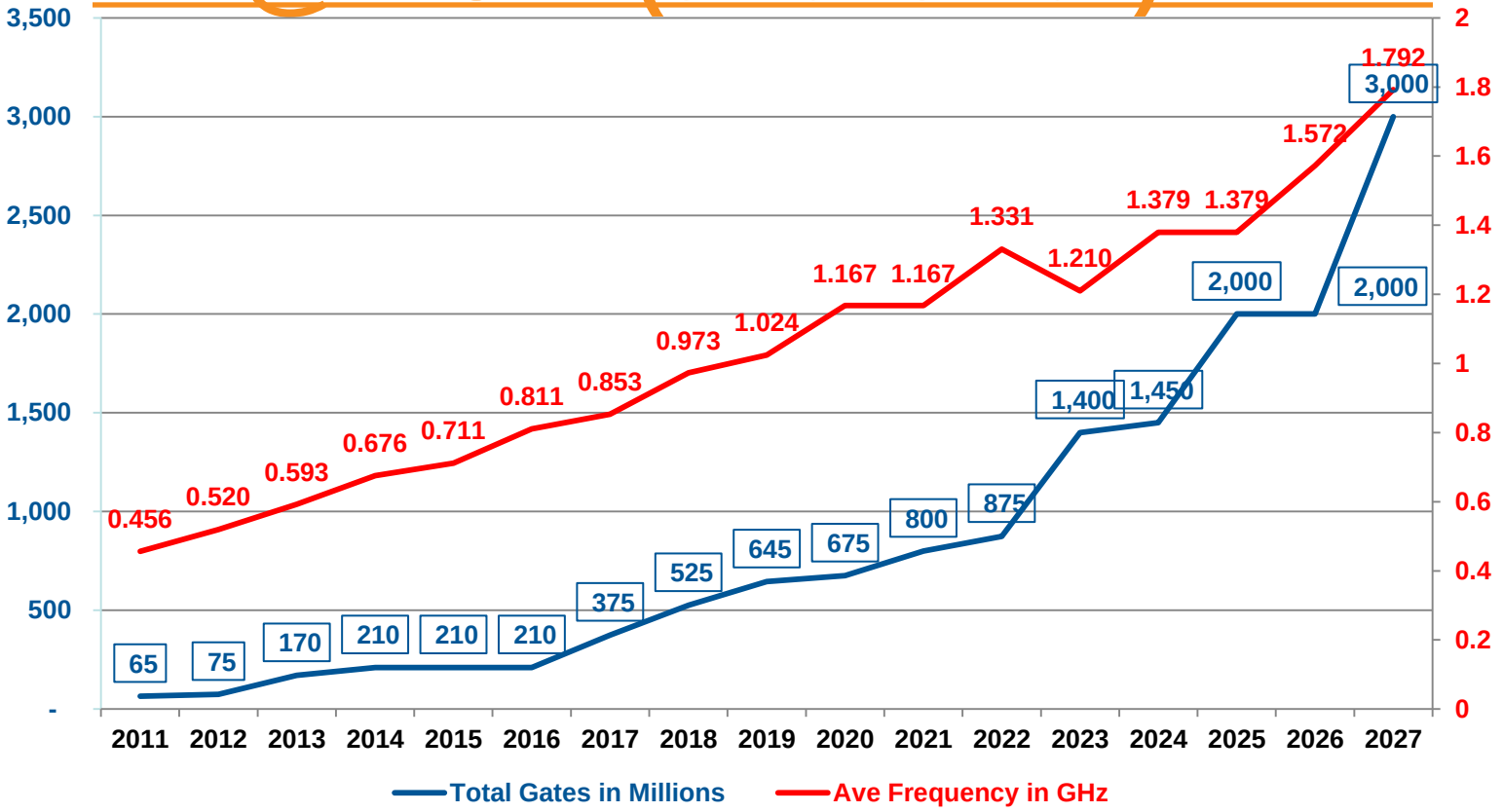
Source: ITRS/Gary Smith EDA 2012

Gate Count of a 5 watt Mobile, $50m SoC Design

- Not bad, in 2013 it's about the same gate count and by 2027 we can do 5,000,000,000 gates, vs. almost 13,000,000,000 usable gates.

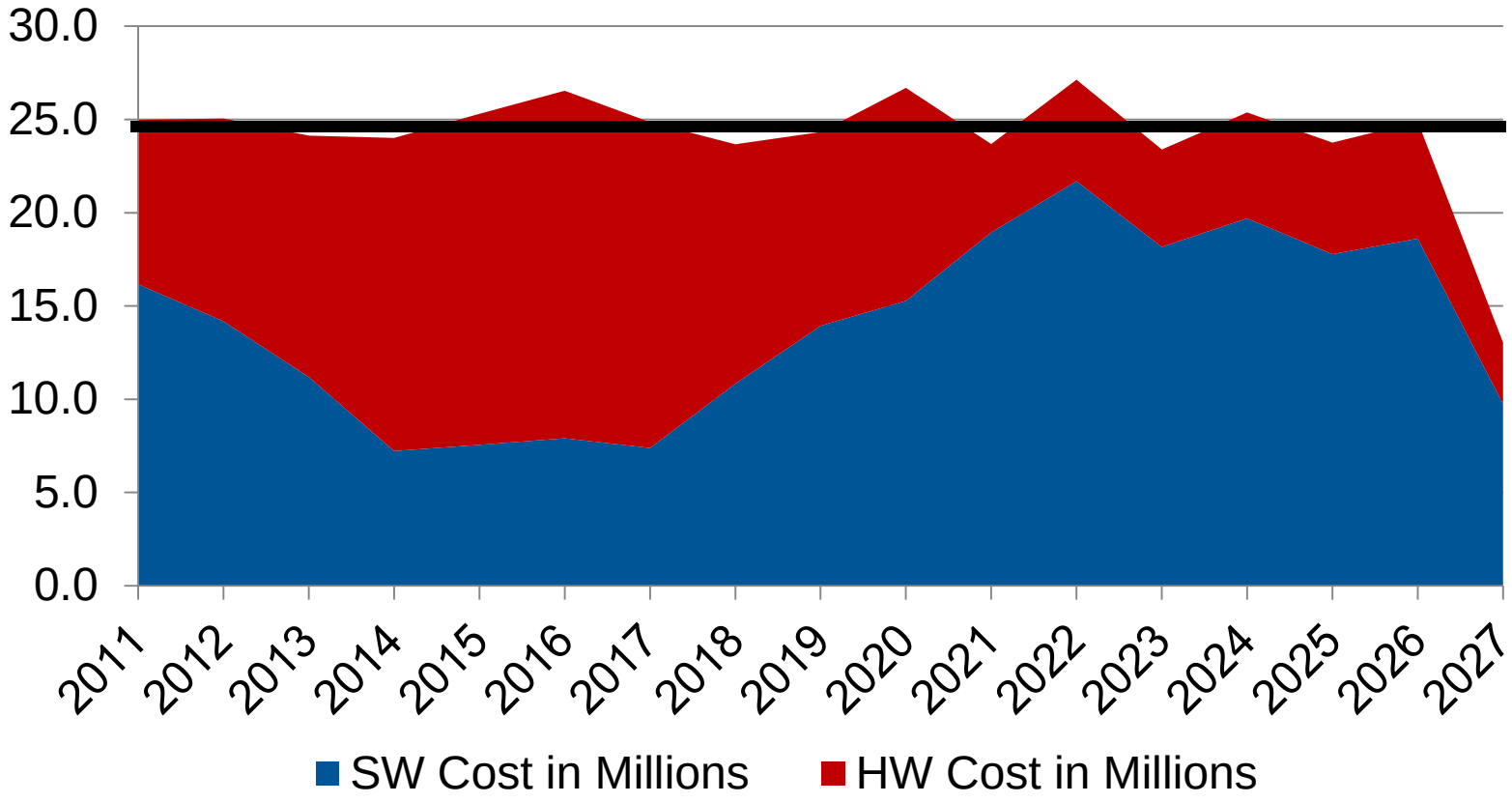
- Now let's look at what a Start-Up can do.

Gates & Frequency @ 25M (5 watts max)



Source: ITRS/Gary Smith EDA 2012

Max Usable Gates at 5 Watts - @ $25m Cost



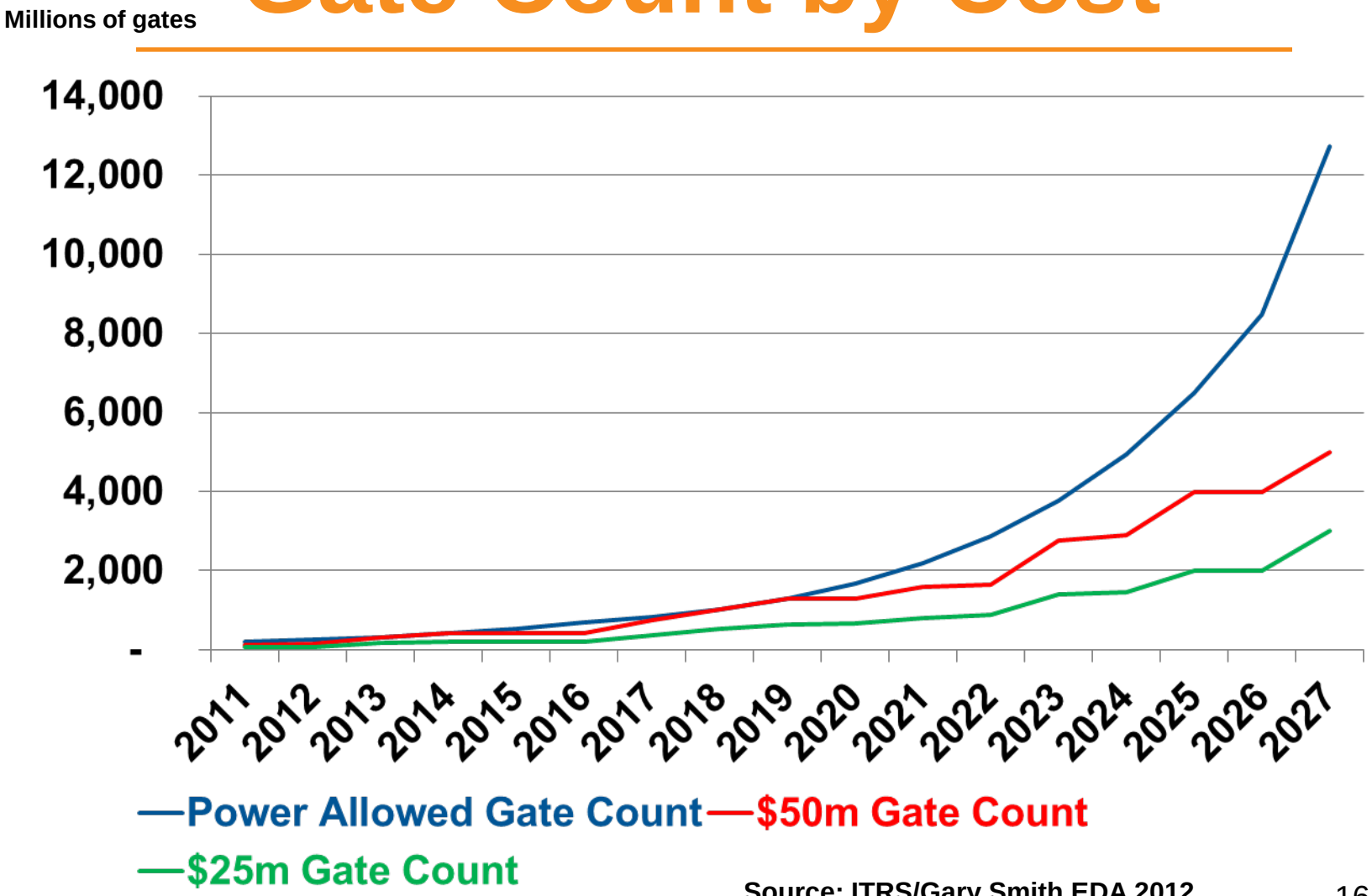
Source: ITRS/Gary Smith EDA 2012

Gate Count of a 5 watt Mobile, $25m SoC Design

- Again not bad. They can come within both their Power Budget and their Cost Budget and design up to 3,000,000,000 gates.

- Now what does that mean to the marketing team.

Gate Count by Cost



Source: ITRS/Gary Smith EDA 2012

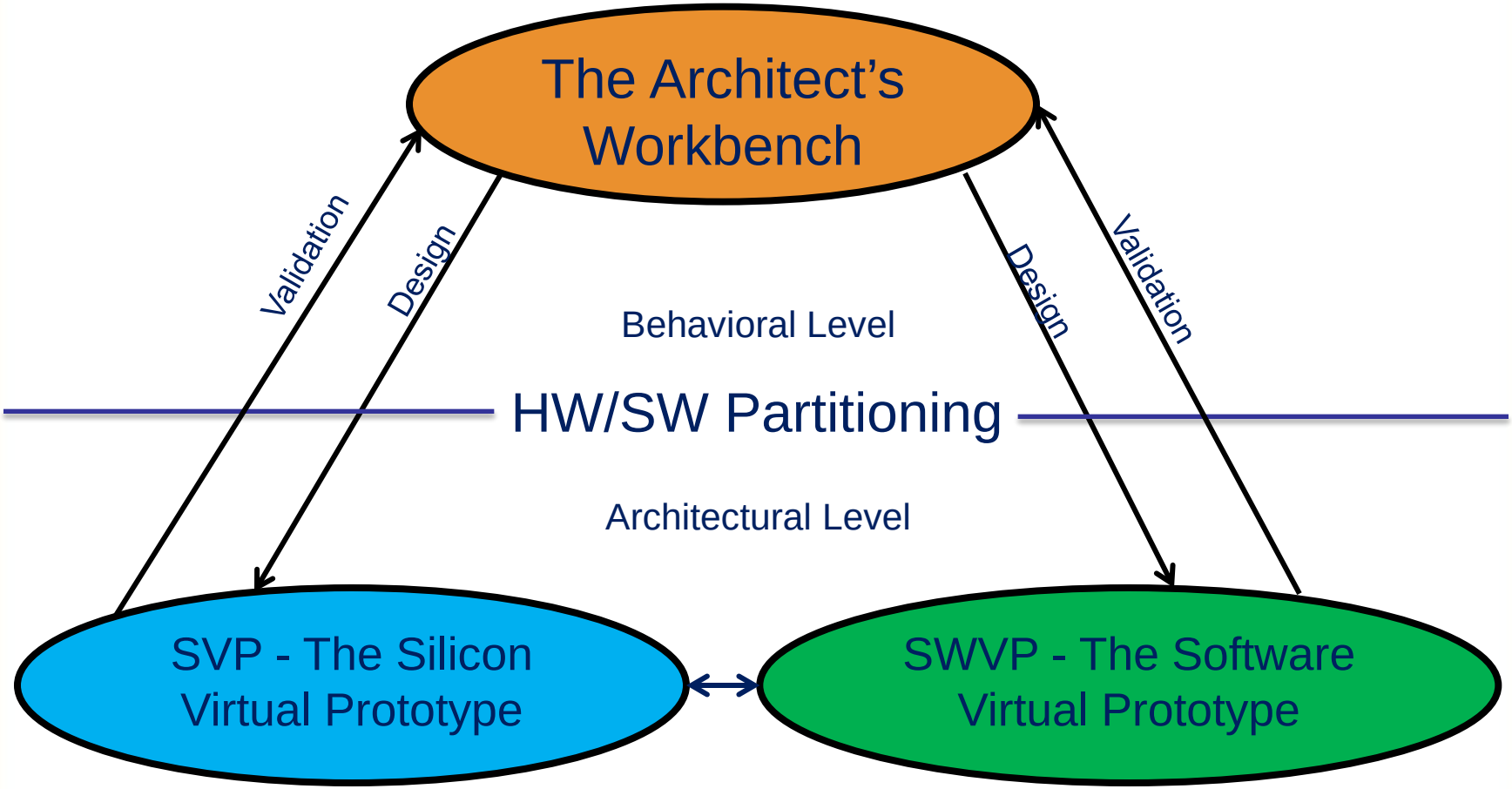
The Competitive Edge

- So the more Apps you have on your phone the better chance you'll have a competitive edge.
- Still they have to be the right Apps.
- And let's face it 3 billion gates is a LOT of gates.
- And how you use those gates is often more important that how many you use.

Bottom Line

- There are predictions being passed around that designs will cost $150 m.
- That's just wrong. You don't know the cost until you pick a gate count.
- Truth is that is that if a Start-Up picks their product carefully, and does a "smart" design, they can compete.

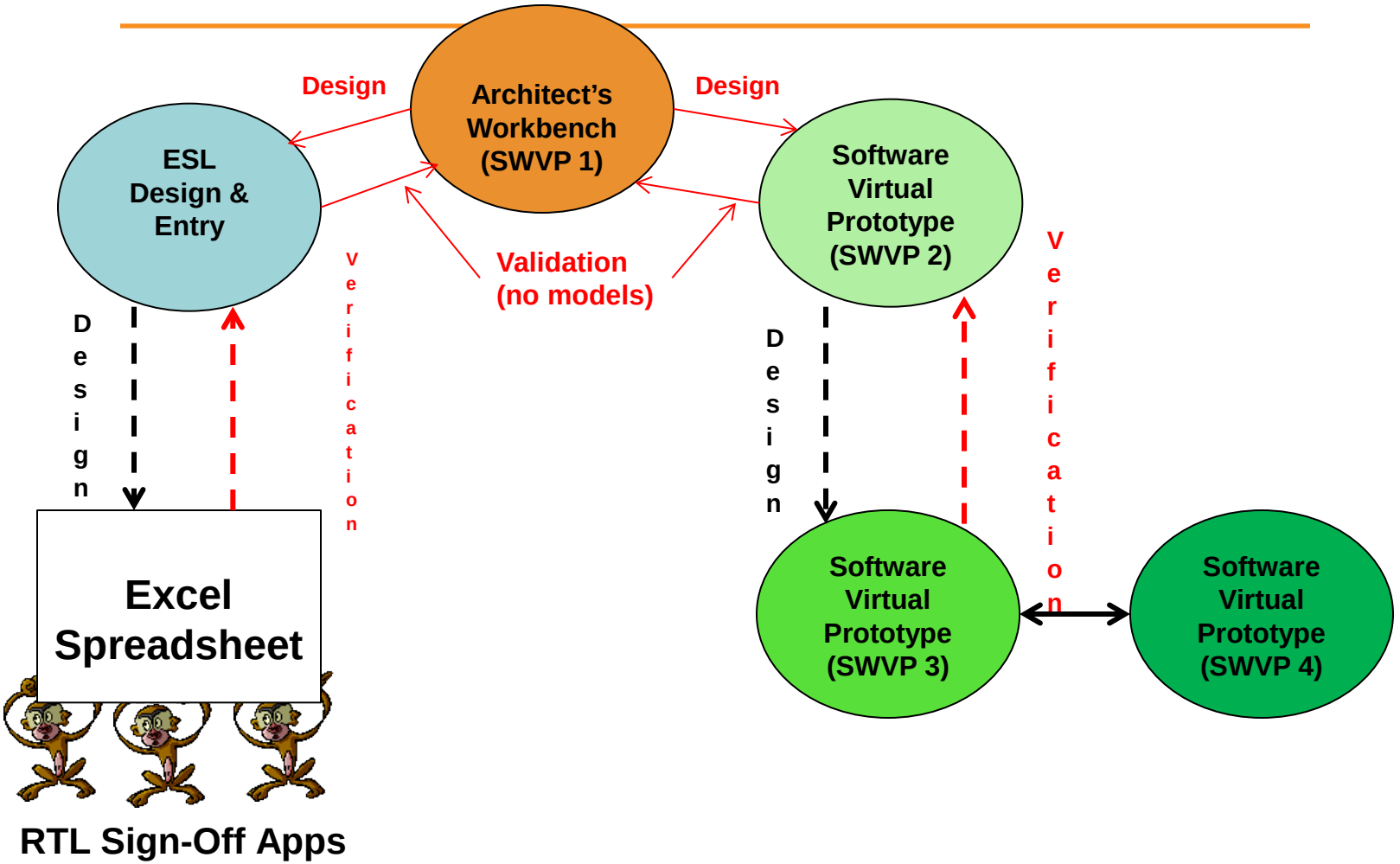
ESL
The Three Virtual Prototypes



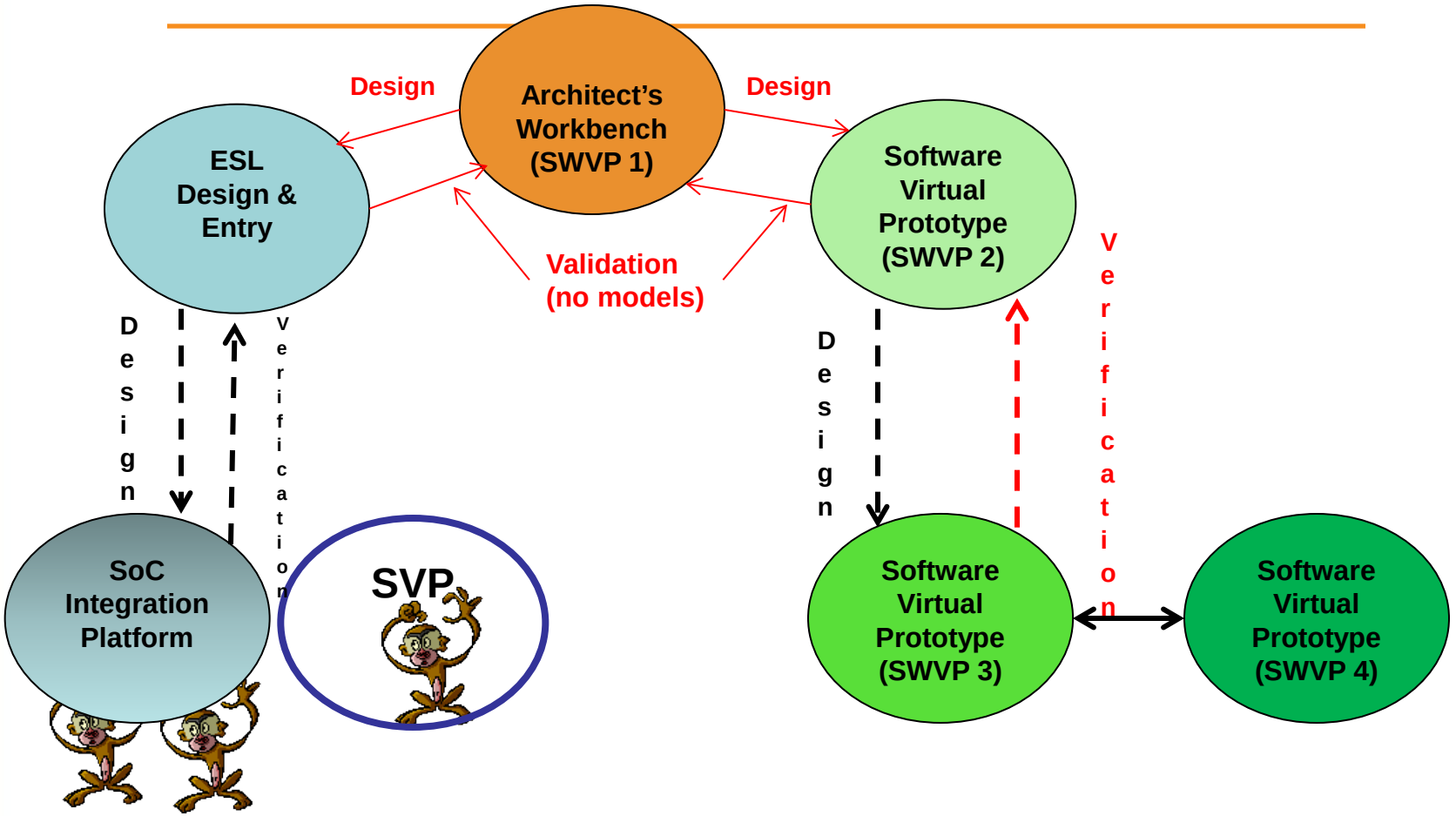
The Silicon Virtual Prototypes

- **SVP 1**, the design starts, hardware accelerators added, Transactional Modeling developed. In-House Platforms designed.
- **SVP 2**, existing RTL blocks inserted, System C blocks synthesized, design completed, design verified, Golden Netlist is the output.
- Could be the same team.

The ESL Flow 2011



The ESL Flow 2012



The Software Virtual Prototypes

- **SWVP 1**, the Architect's Workbench, used by the Architectural Team for design formation and exploration, usually modeled in C/C++ or M (Mathwork's Language).

  Microprocessors selected, Foundation Platform selected, some Applications Platforms selected.

The Software Virtual Prototypes

- **SWVP 2**, Applications code written. Applications code is run on the SVP checking for latency and power.
- **SWVP 3**, Firmware & Middleware written. Applications code is run on the SVP checking for final latency and power.
- **SWVP 4**, Used by product marketing and sales to check out the design with prospective customers for possible modifications.

The Software Virtual Prototypes

- The four different SWVPs serve four different functions, therefore there are:
  - **four different users,**
  - **four different specifications,**
  - **and four different price points!**

The ESL Flow 2013 Numbers