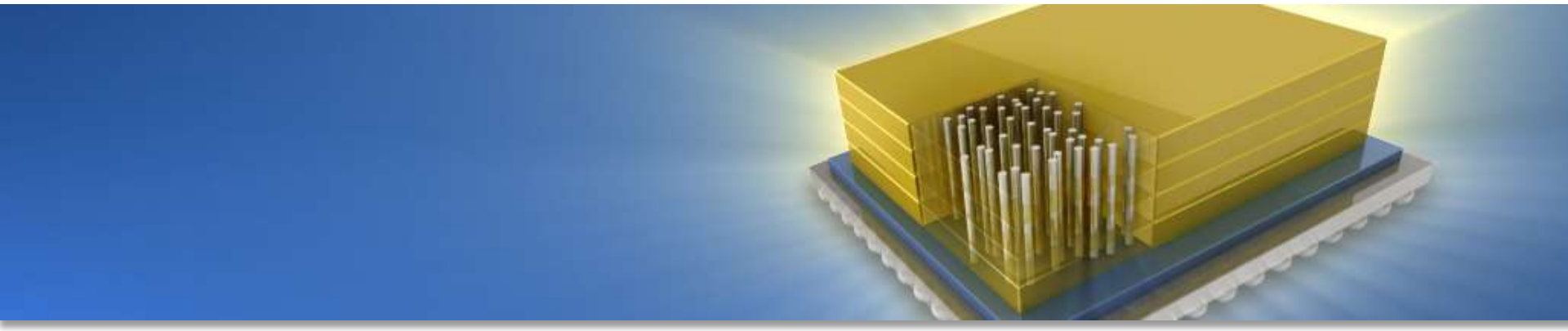


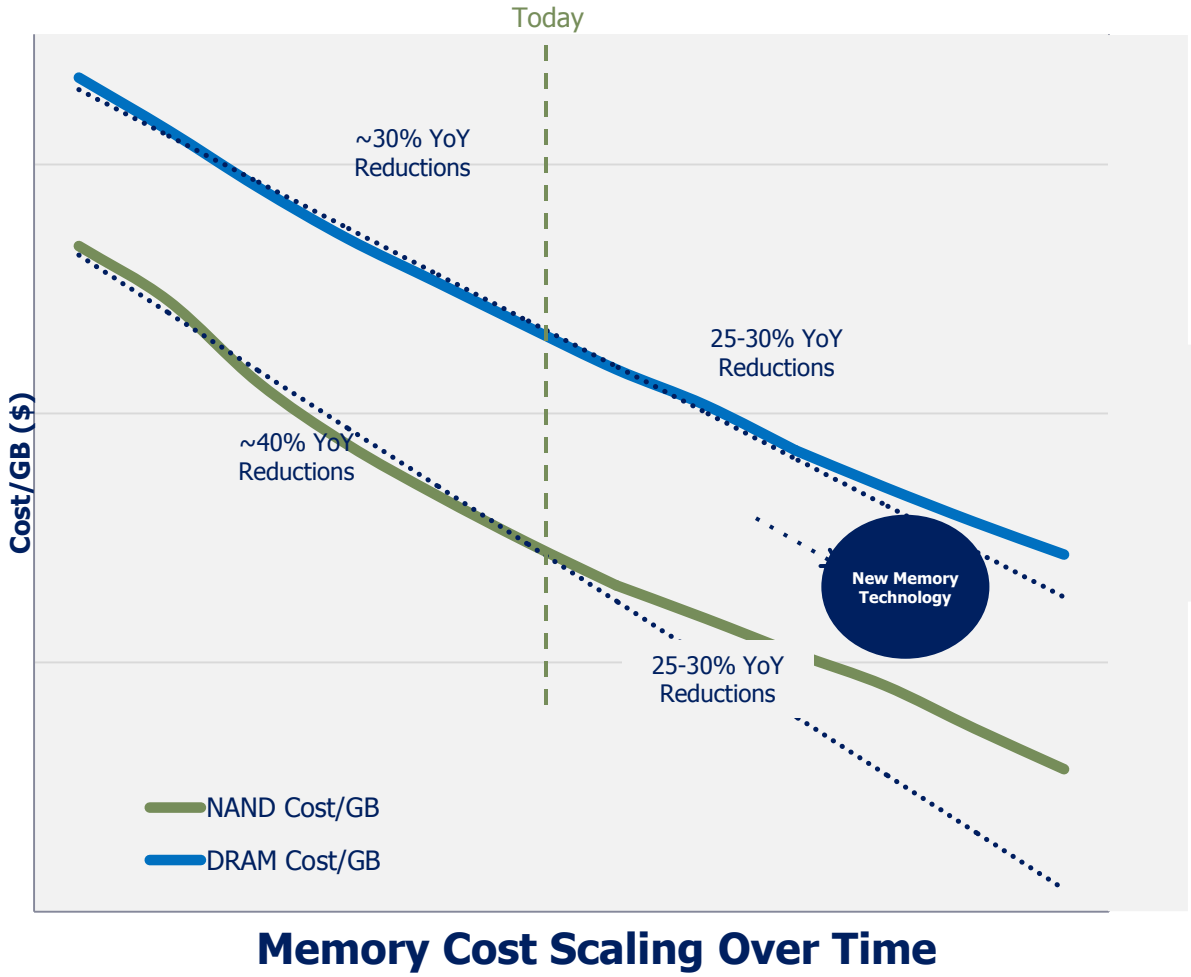
Hybrid Memory Cube

Mike Black

The Situation

- Continued global demand for mobility
- Device proliferation
- Impact of the Cloud
- Big data analytics challenge

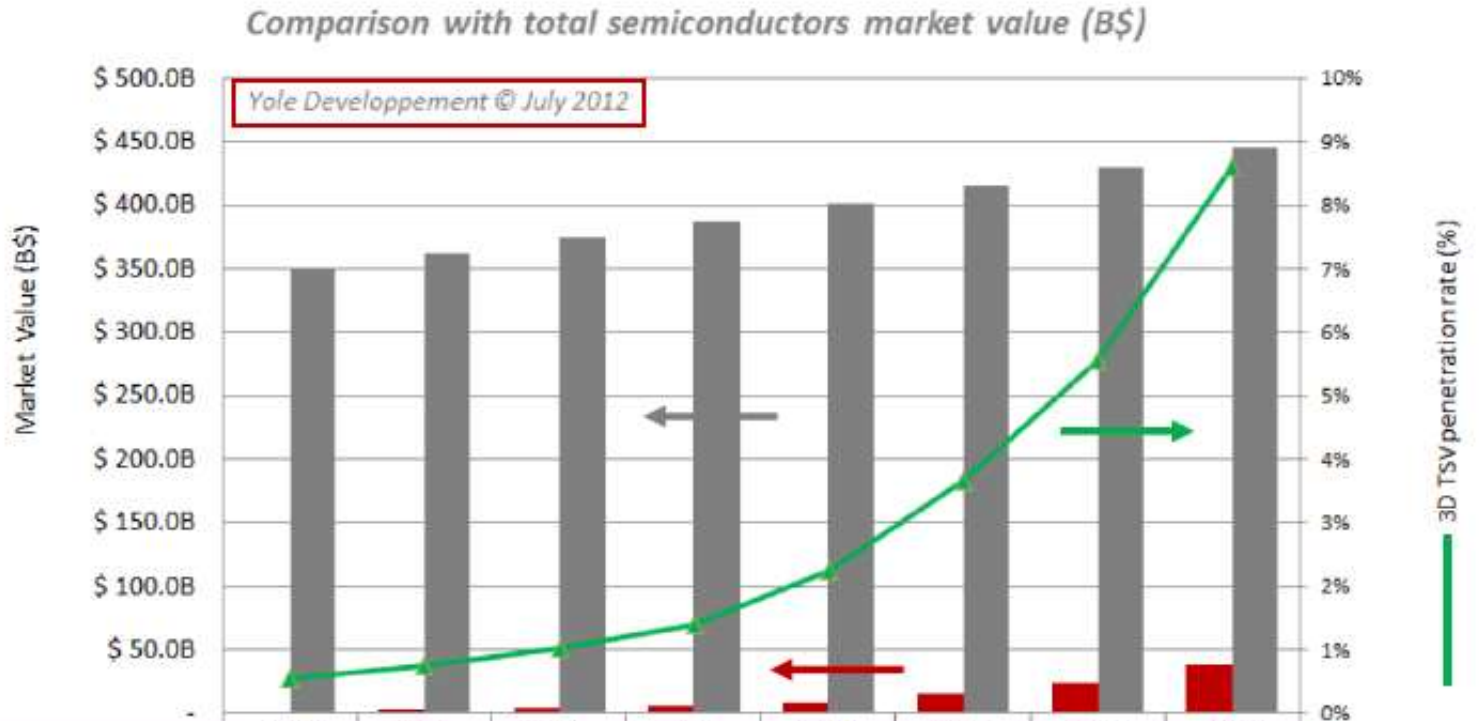
The Roadmap



Memory Cost Scaling Over Time

- **Physical and Electrical Materials Limitations**
- **Equipment Capability**
- **Cost and Complexity**

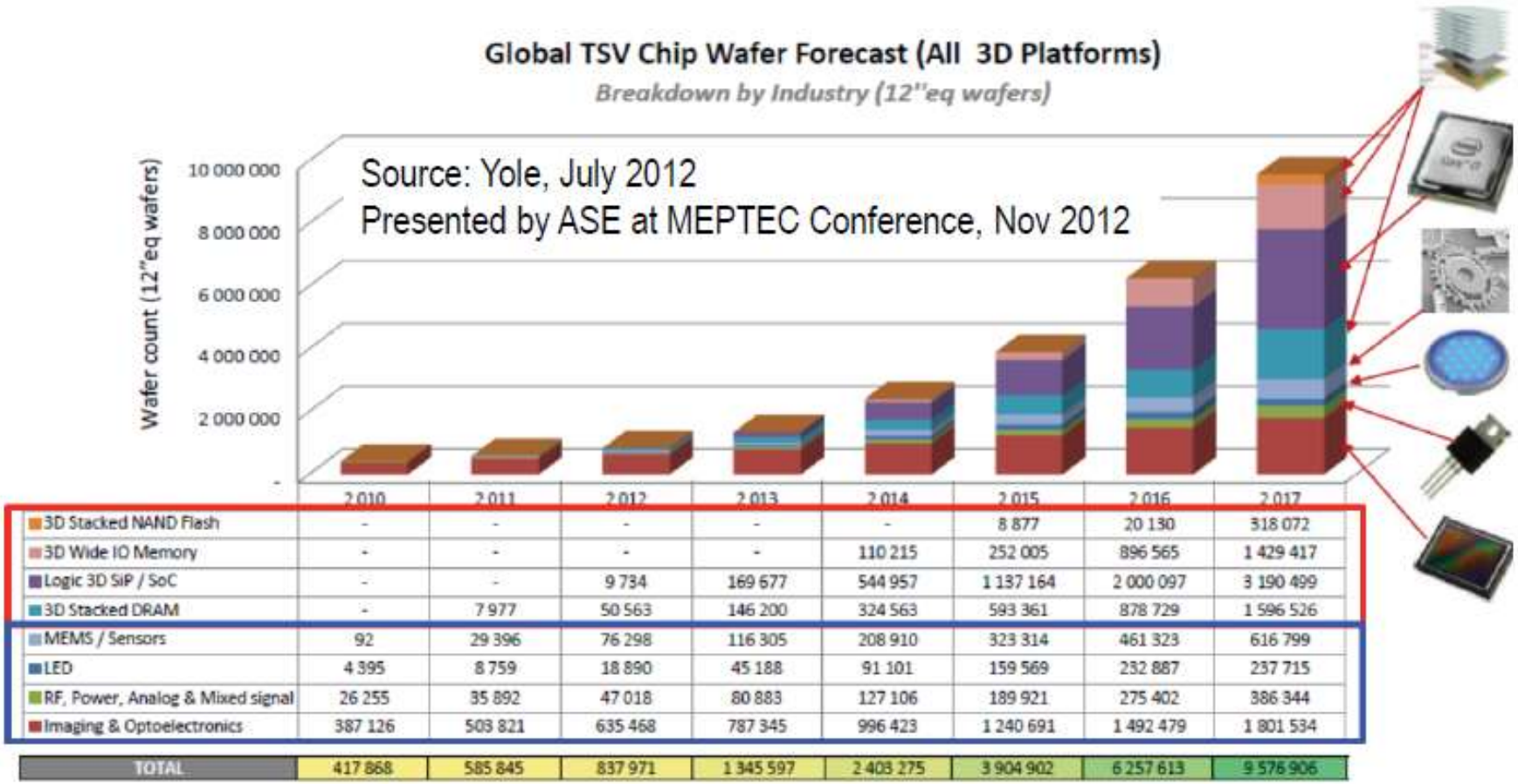
Global Revenue Forecast
3D TSV Devices



	2010	2011	2012	2013	2014	2015	2016	2017
TOT 3D TSV Devices (B$)	$ 1.9B	$ 2.7B	$ 3.9B	$ 5.5B	$ 9.0B	$ 15.2B	$ 23.9B	$ 38.4B
TOT Semi value (B$)	$ 350.0B	$ 362.3B	$ 374.9B	$ 388.1B	$ 401.6B	$ 415.7B	$ 430.2B	$ 445.3B
3D TSV Penetration rate	1%	1%	1%	1%	2%	4%	6%	9%

* : Excluding Interposer Revenues !

Global Forecast
TSV Chip Wafers



	2010	2011	2012	2013	2014	2015	2016	2017
3D Stacked NAND Flash	-	-	-	-	-	8 877	20 130	318 072
3D Wide IO Memory	-	-	-	-	110 215	252 005	896 565	1 429 417
Logic 3D SiP / SoC	-	-	9 734	169 677	544 957	1 137 164	2 000 097	3 190 499
3D Stacked DRAM	-	7 977	50 563	146 200	324 563	593 361	878 729	1 596 526
MEMS / Sensors	92	29 396	76 298	116 305	208 910	323 314	461 323	616 799
LED	4 395	8 759	18 890	45 188	91 101	159 569	232 887	237 715
RF, Power, Analog & Mixed signal	26 255	35 892	47 018	80 883	127 106	189 921	275 402	386 344
Imaging & Optoelectronics	387 126	503 821	635 468	787 345	996 423	1 240 691	1 492 479	1 801 534
TOTAL	417 868	585 845	837 971	1 345 597	2 403 275	3 904 902	6 257 613	9 576 906

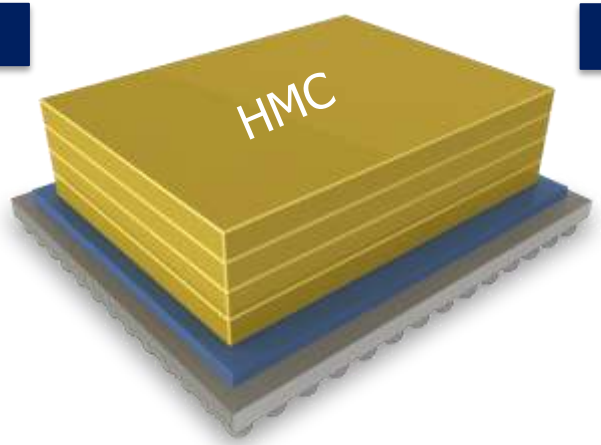
The Innovation: **HMC**

Revolutionary Approach to Break Through the "Memory Wall"

- Evolutionary DRAM roadmaps hit limitations of bandwidth and power efficiency
- Micron introduces a new class of memory: Hybrid Memory Cube
- Unique combination of DRAMs on Logic

Key Features

- Micron-designed logic controller
- High speed link to CPU
- Massively parallel "Through Silicon Via" connection to DRAM



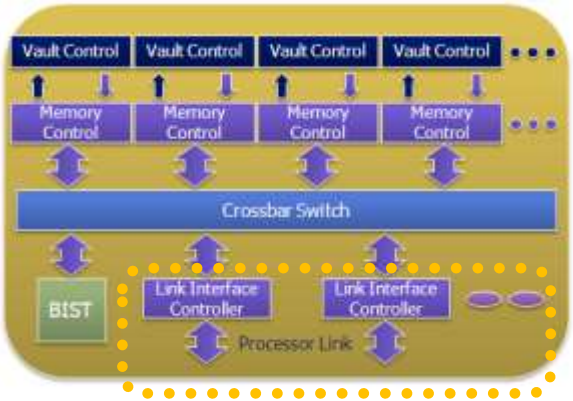
Unparalleled performance

- Up to 15X the bandwidth of a DDR3 module
- 70% less energy usage per bit than existing technologies
- Occupying nearly 90% less space than today's RDIMMs

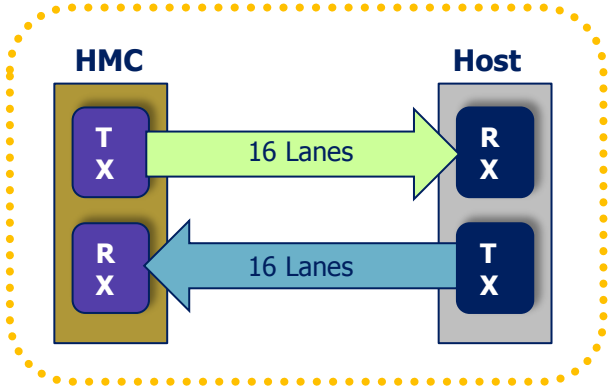
Full silicon prototypes in silicon
TODAY

Targeting high performance computing and networking, eventually migrating into computing and consumer

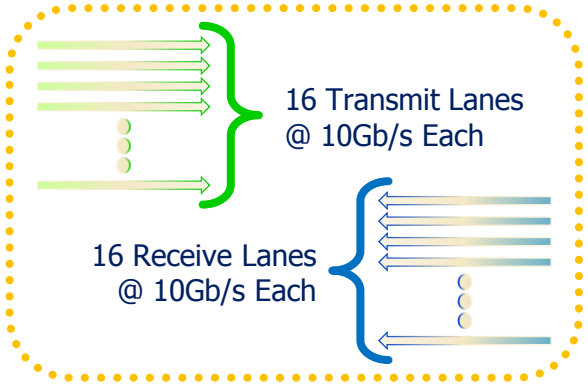
Link Controller Interface



HMC (Gen2) has Four Links



Each Link has 32 differential Lanes



(*) HMC-SR supports up to 15Gbps SERDES options

Designed with Off-the-Shelf, High Speed SerDes Interface

Link Interface Examples

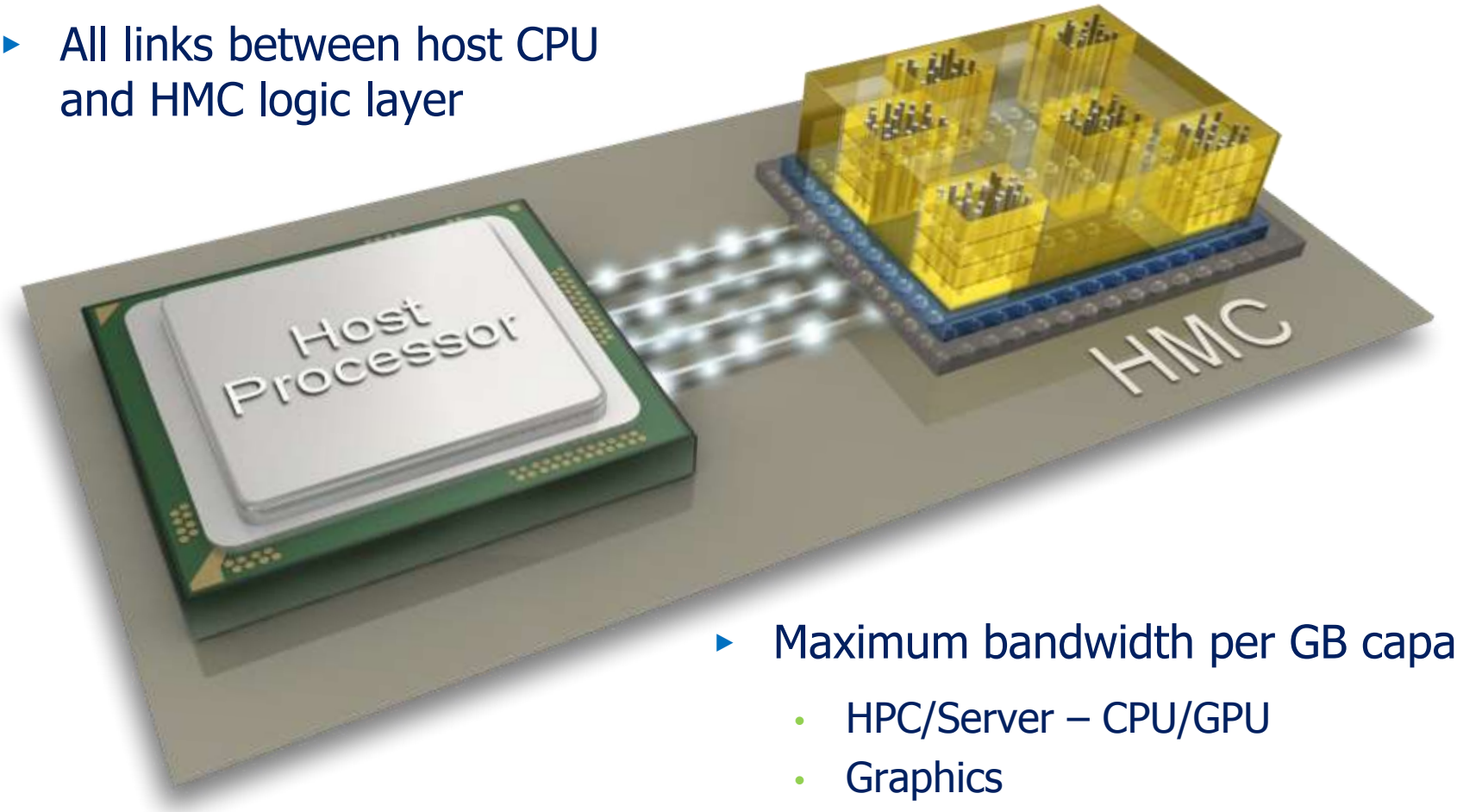
4 Link Example (160GB/s)

- 10Gb/s per lane
- 32 lanes per link (320Gb/s = 40GB/s)
  - 16 TX and 16 RX
- 4 Links (40GB/s x 4) = **160GB/s**

(*) Aggregate DRAM peak bandwidth remains 160GB/s

HMC Near Memory

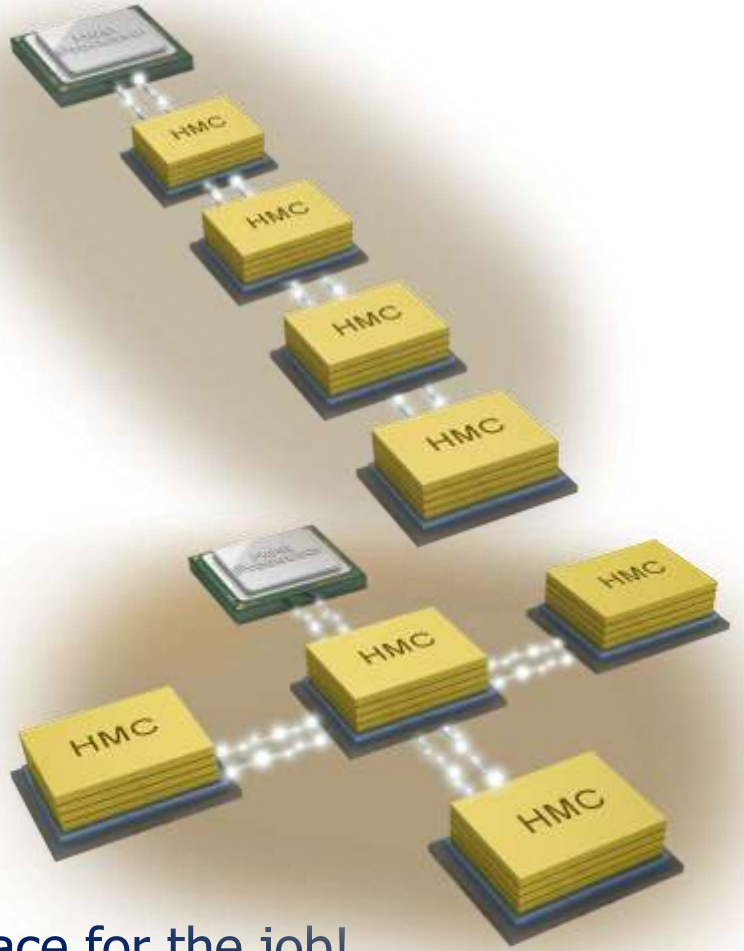
- All links between host CPU and HMC logic layer



- Maximum bandwidth per GB capacity
  - HPC/Server – CPU/GPU
  - Graphics
  - Networking systems
  - Test equipment

HMC "Far" Memory

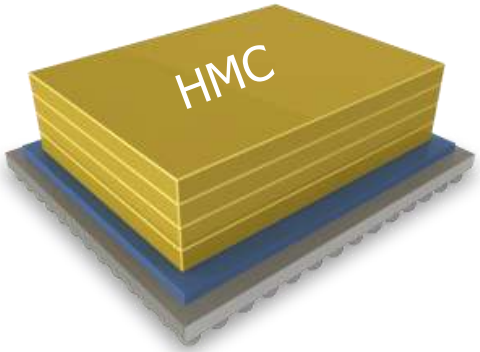
- Far memory:
  - Some HMC links connect to host, some to other cubes
  - Scalable to meet system requirements
  - Can be in module form or soldered-down
- Future interfaces may include:
  - Higher speed electrical (SERDES)
  - Optical
  - Whatever the most appropriate interface for the job!

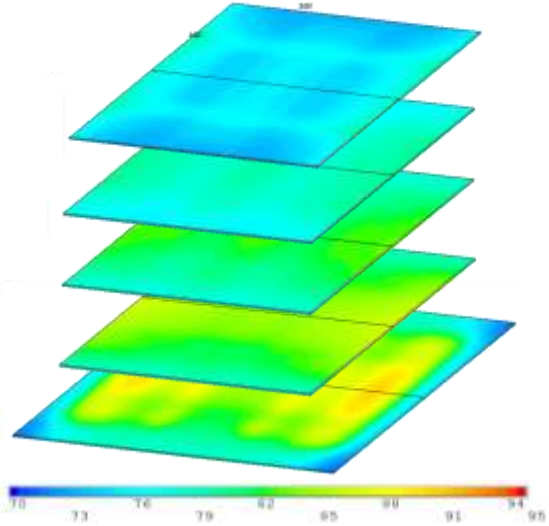


The Requirements

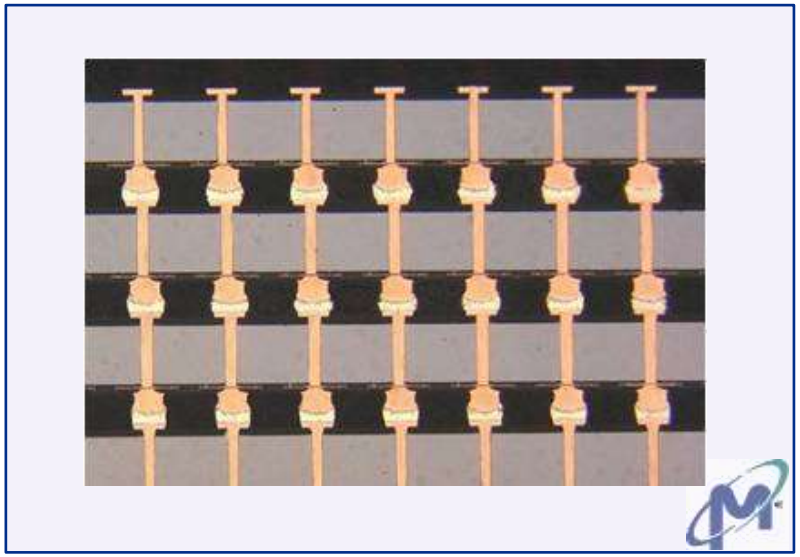
- Major industry transitions demand innovative business models:
  - Joint R &D efforts
  - Agreed-upon design standards
  - Cross-industry coordination
  - Customer education and hands-on training

Internal Support





- Micron design and verification tools
- Memory and logic design
- Interconnect modeling
- Thermal modeling



HMC Design Environment Examples

Design of Memory Cells and Array Matrix

Design Step	Challenges	EDA Solution	Status
Core Cells Optimization	Area, Speed, Power	HSPICE, FineSim, Verilog	✓
Drivers and Sense Amps	Speed, Noise	HSPICE, FineSim, Verilog	✓

Design of Logic Die

Design Step	Challenges	EDA Solution	Status
Core Logic Optimization	Area, Speed, Power	Cadence RC, EDI, EPS, ETS	✓
I/O Drivers and Package	Speed, Noise, EM,	Cadence ADE, Spectre, VPS	✓

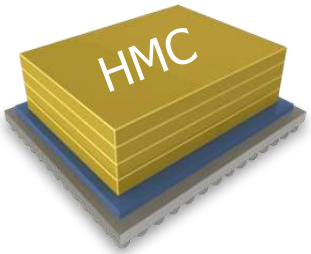
Integration into a Printed Circuit Board

Design Step	Challenges	EDA Solution	Status
DC & AC Models for I/Os	Accuracy vs runtime	Nimbic-Apex, Ansoft-Q3D, TPA, HFSS	✓
Power & Temp. Analysis	For Die, Pkg, Board	Icepack, FloTHERM	✓

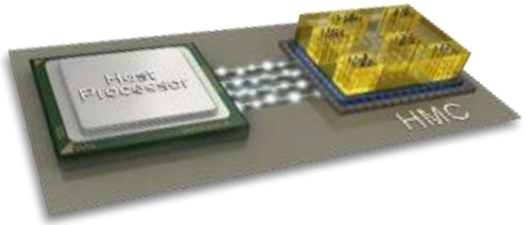
System-level Integration

Design Step	Challenges	EDA Solution	Status
HMC Functional Model(s)	Comply with Standard	To be determined	**By Q2**
HMC Timing Model(s)	Language a, b, c	To be determined	**By Q2**

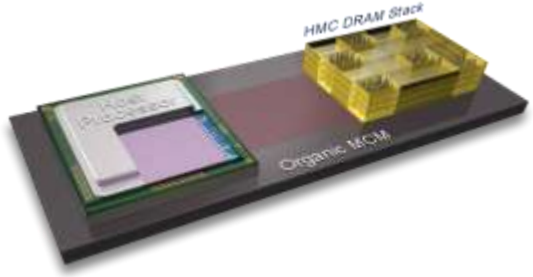
External Support



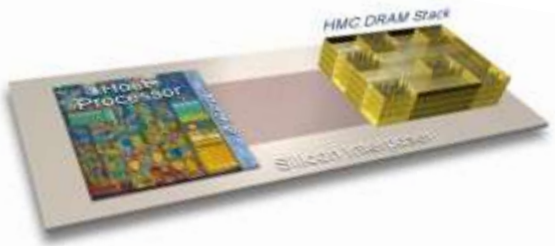
Traditional PCB



Advanced MCM 3D/2.5D



Si Interposer 3D/2.5D



Broad Industry Adoption

HMCC Mission

Promote widespread adoption and acceptance of an industry standard serial interface and protocol for Hybrid Memory Cube

ALTERA. ARM IBM Micron Open-Silicon SAMSUNG SK hynix XILINX

Hybrid Memory Cube CONSORTIUM

http://www.hybridmemorycube.org/

HMC Consortium Update

- HMCC specification final and available!
- Visit hybridmemorycube.org for more information.

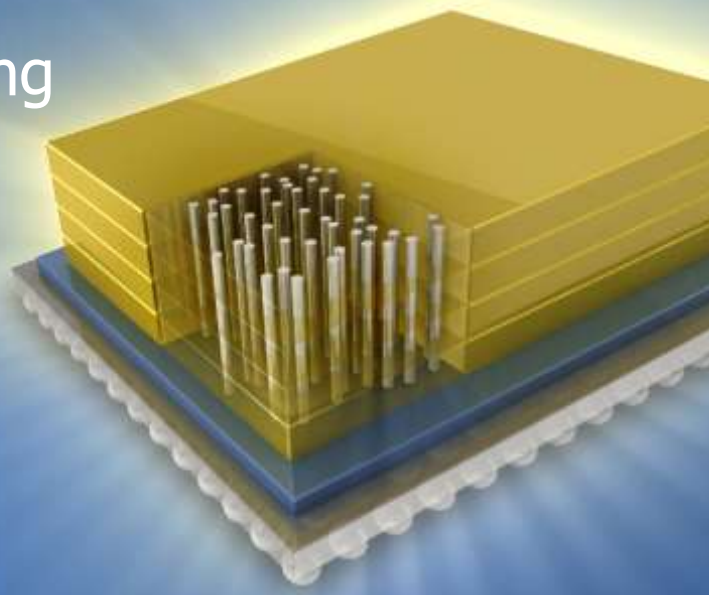
- Developers working on next speed grade for SR and USR PHY:
  - SR speed bump to 28Gb/s
  - USR speed bump to 15Gb/s

Over 100 Adopters to date!			
Accel, Ltd	Fujitsu Limited	Luxtera Inc.	Pico Computing
ADATA Technology Co., LTD	Galaxy Computer System Co., Ltd.	Marvell	Renesas Electronics Corporation
AIRBUS	GDA Technologies	Mattozetta Technologies	Science & Technology Innovations
Altior	GLOBALFOUNDRIES	Maxeler Technologies Ltd.	SEAKR Engineering
APIC Corporation	GraphStream Incorporated	MediaTek	ST Microelectronics
Arira Design	HGST, a Western Digital Company	Memoir Systems Inc.	Suitcase TV Ltd
Arnold&Richter Cine Technik	HiSilicon Technologies Co., Ltd	Mentor Graphics	Tabula
Atria Logic, Inc.	HOY Technologies	Miranda	Tech-Trek
BroadPak	Huawei Technologies	Mobiveil, Inc.	Teradyne, Inc
Cadence Design Systems, Inc.	Infinera Corporation	Montage Technology, Inc.	The Regents of the University of California
Convey Computer Corporation	Information Sciences Institute USC	Napatech A/S	Tilera Corporation
Cray Inc.	Inphi	National Instruments	Tongji University
DAVE Srl	ISI/Nallatech	NEC corpration	T-Platforms
Design Magnitude Inc.	Israel Institute of Technology	Netronome	TU Kaiserslautern
Dream Chip Technologies GmbH	Juniper Networks	New Global Technology	UC, Irvine
Engineering Physics Center of MSU	Kool Chip	Northwest Logic	UMC
eSilicon Corporation	Korea Advanced Institute of Science	Obsidian Research	University of Heidelberg ZITI
Exablade Corporation	Lawrence Livermore National Laboratory	OmniPhy	University of Rochester
Ezchip Semiconductor	LeCroy Corporation	Oregon Synthesis	Winbond Electronics Corporation
FormFactor Inc.	LogicLink Design, Inc.	Perfcraft	Woodward McCoach, Inc.
			ZTE Corporation

Ecosystem

The Future

- Memory ecosystem changing
- High performance signaling and routing opening doors for EDA growth
- HMC is coming - THIS YEAR
- Tool and IP support needed now

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