A Holistic Approach for 3D/2.5D Realization

Brandon Wang
Cadence Design Systems

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Outline

- Semiconductor Challenges – More Moore or beyond Moore?
- 3D/2.5D Challenges
- A holistic methodology for 2.5D/3D Realization
- Summary

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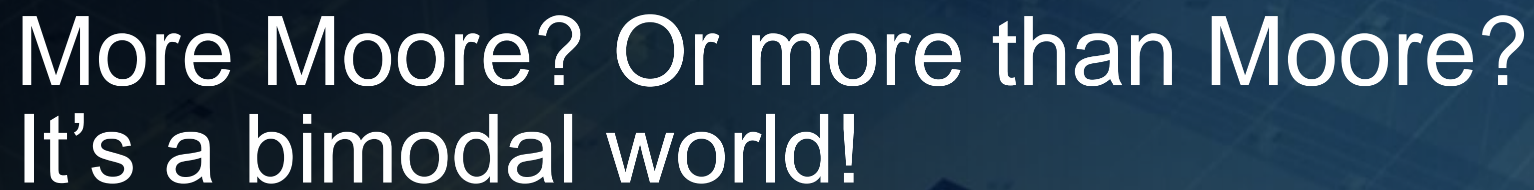

More Moore? Or more than Moore? It's a bimodal world!

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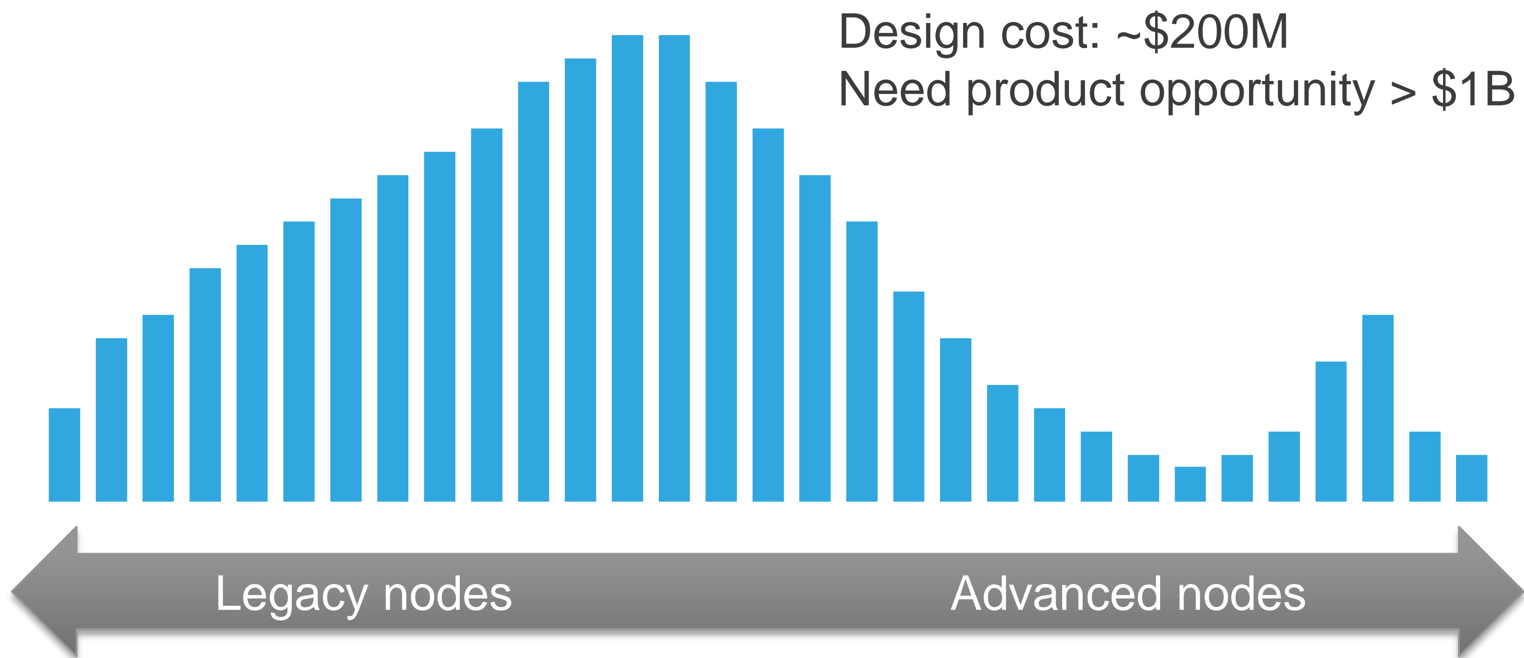
Cost of advanced-node designs

Source: IBS, May 2011	32 / 28nm node	22 / 20nm node
Fab construction	$3B	$4B – 7B
Process R&D	$1.2B	$2.1B – 3B
Design cost	$50M – 90M	$120M – 500M
Mask set	$2M – 3M	$5M – 8M
EDA enablement	$400M – 500M	$800M – 1.2B



Source: IBS 2012

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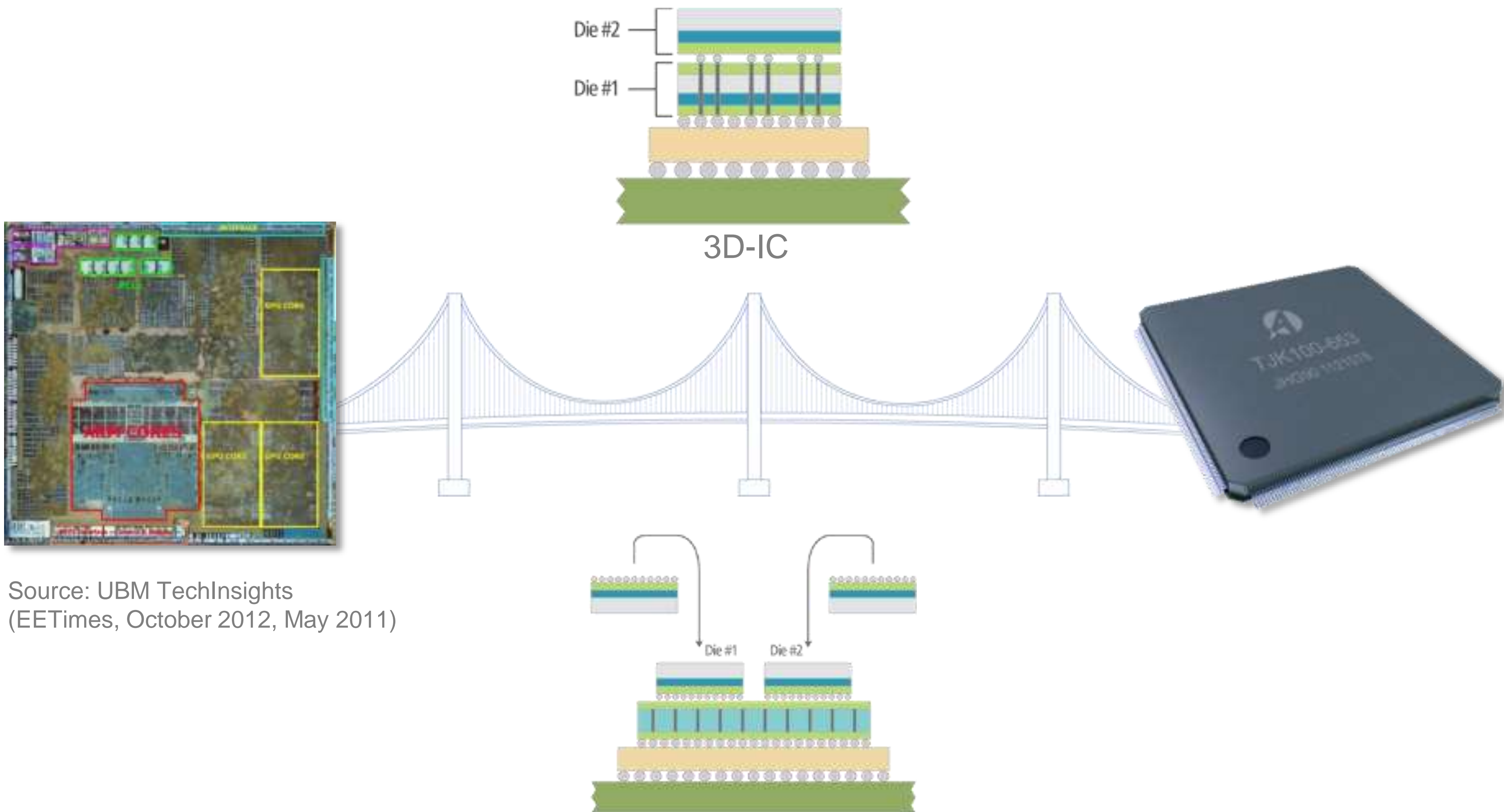
3D-IC is a bridge for “More Than Moore” solutions



Source: UBM TechInsights
(EETimes, October 2012, May 2011)

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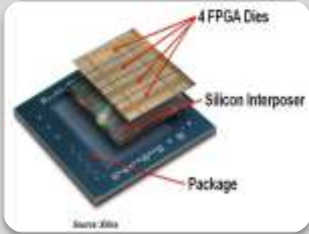
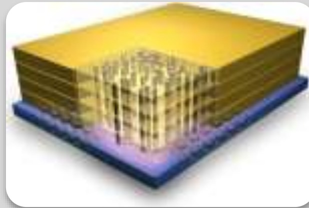
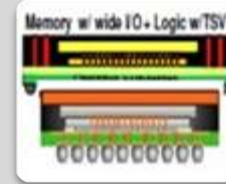
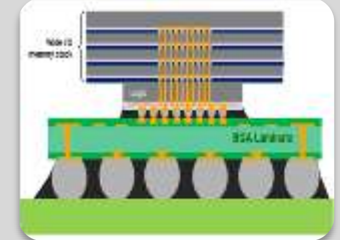
Short-, medium-, and long-term path to 3D-IC

EDA work starts at least 3-4 years earlier









Si Partitioning with TSV Interposer

- Market : FPGA
- Xilinx in 2010
- **2011-2012**

Memory Cube with TSVs

- MARKET : Server and computing
- IBM and Micron
- **2012-2013**

Logic + memory w/ 2.5D TSV Interposer

- MARKET : GPU, gaming console
- ST testchip in 2010
- **2013-2014**

Wide IO + Logic with TSVs

- MARKET : Mobile, tablet, gaming processors
- ST-E /LETI WIOMING in 2011
- **2014-2015**

High-performance computing

- MARKET : CPU, MCMs etc
- ST-E /LETI WIOMING in 2011
- **~ 2015**

SHORT → MEDIUM → LONG

Standards, ecosystem, cost

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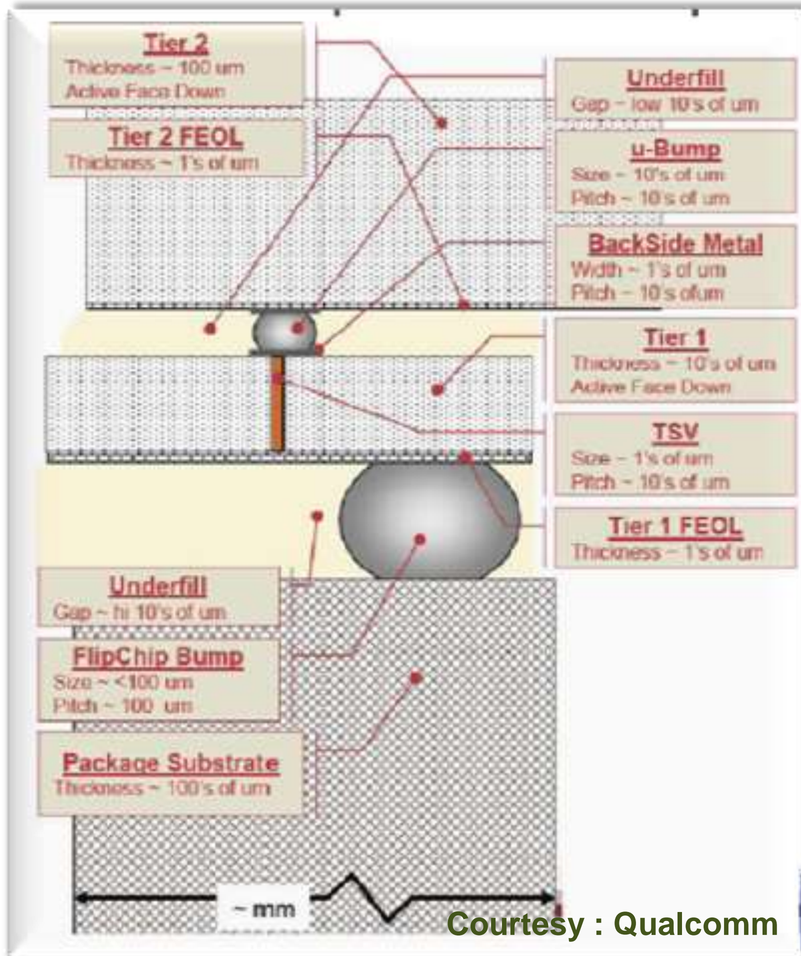
So what changes with 3D-IC in EDA world?

Revamped EDA requirements



- Package silicon co-design
- New layout layers (e.g. alignments)
- New layout layer (e.g. Back-side RDL)
- New extraction features (e.g. TSV)
- Inter-processes DRC/LVS
- Cross-die, power and signal integrity
- Cross-die timing closure
- Thermal analysis and mechanical constraints
- Manufacture test

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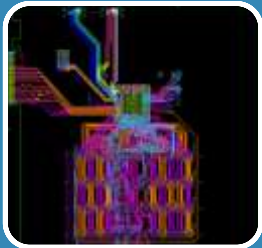
Cadence 3D-IC Integrated Solution

Complete Implementation Platforms for flexible Entry Point and Seamless Co-design

Using OpenAccess, EDI, Virtuoso each has dedicated 3DIC functions that work together, plus co-design with Cadence SiP tools for complete End to End implementation including early stage system exploration and feasibility



Full Spectrum Analysis Capability

RC/ET DFT and ATPG for 3DIC

EPS/ETS/QRC Digital Analysis Tool

Virtuoso Based Full Spice Simulation Capacity

SiP/Sigrity based Extraction, SI, and PI System/Package Analysis

PowerDC Thermal Analysis

Ecosystem partnership and Real Experiences/Proof Points

Cadence has been working with ecosystem partners since 2007 on 3DIC

8 test chips completed and 1 production chip done

Several projects ongoing

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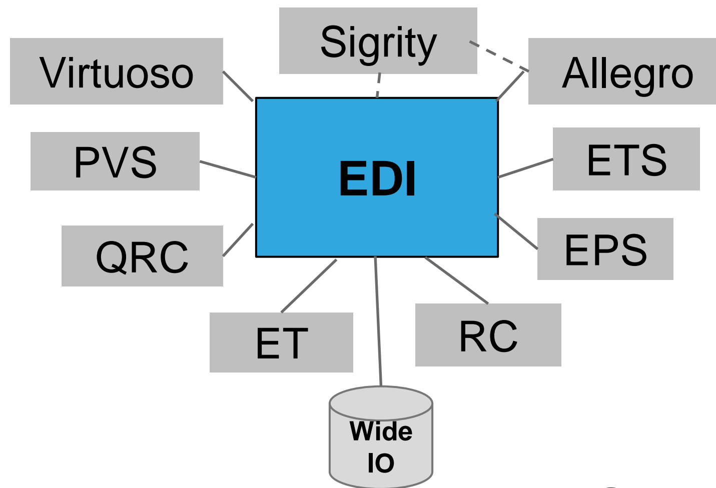
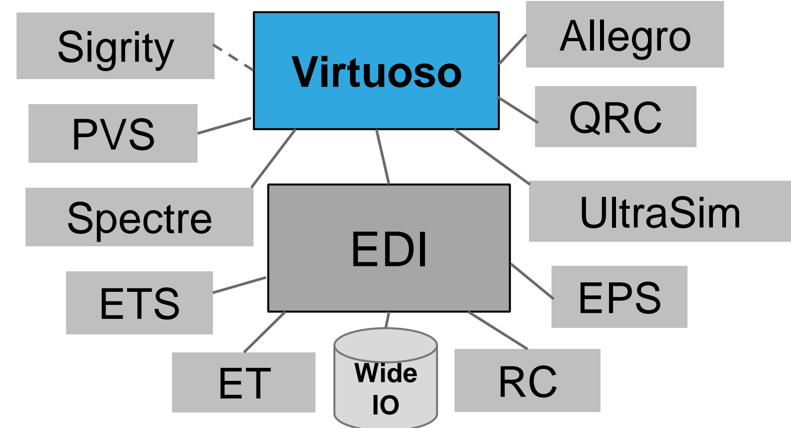
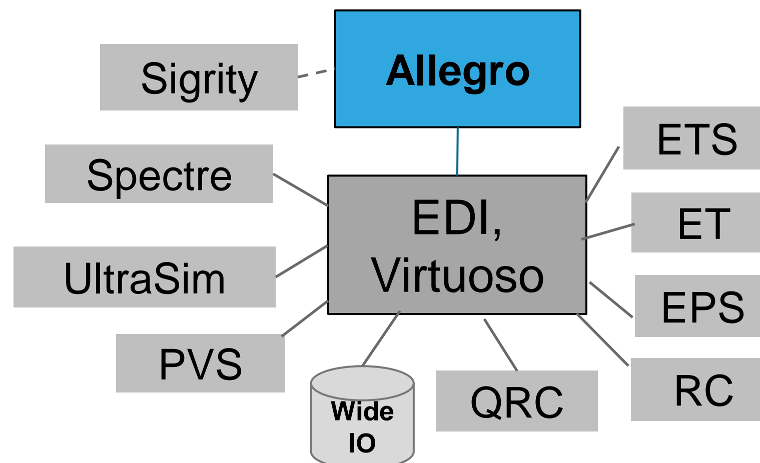
3D/2.5D Solutions with flexible Implementation Cockpits







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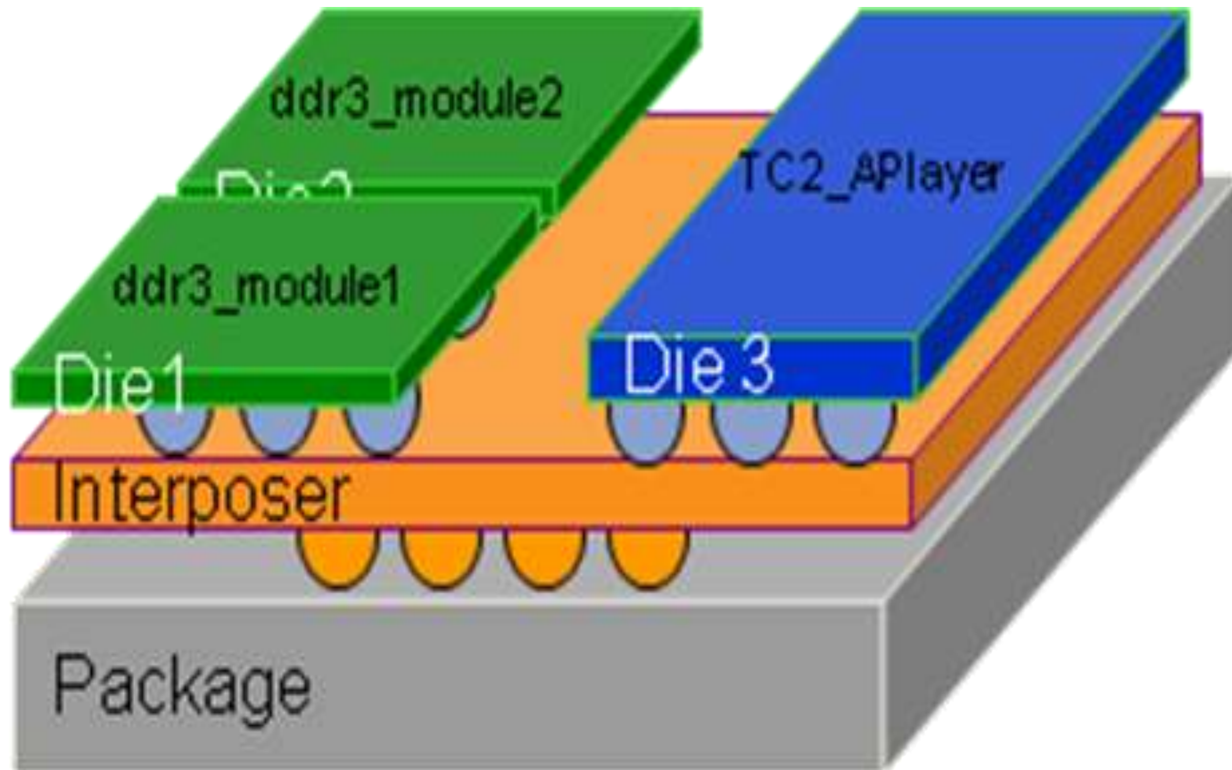
Example: 2.5D Silicon Interposer

Die3, TC2 –Logic Die. Die 1,2: Memory Dies;



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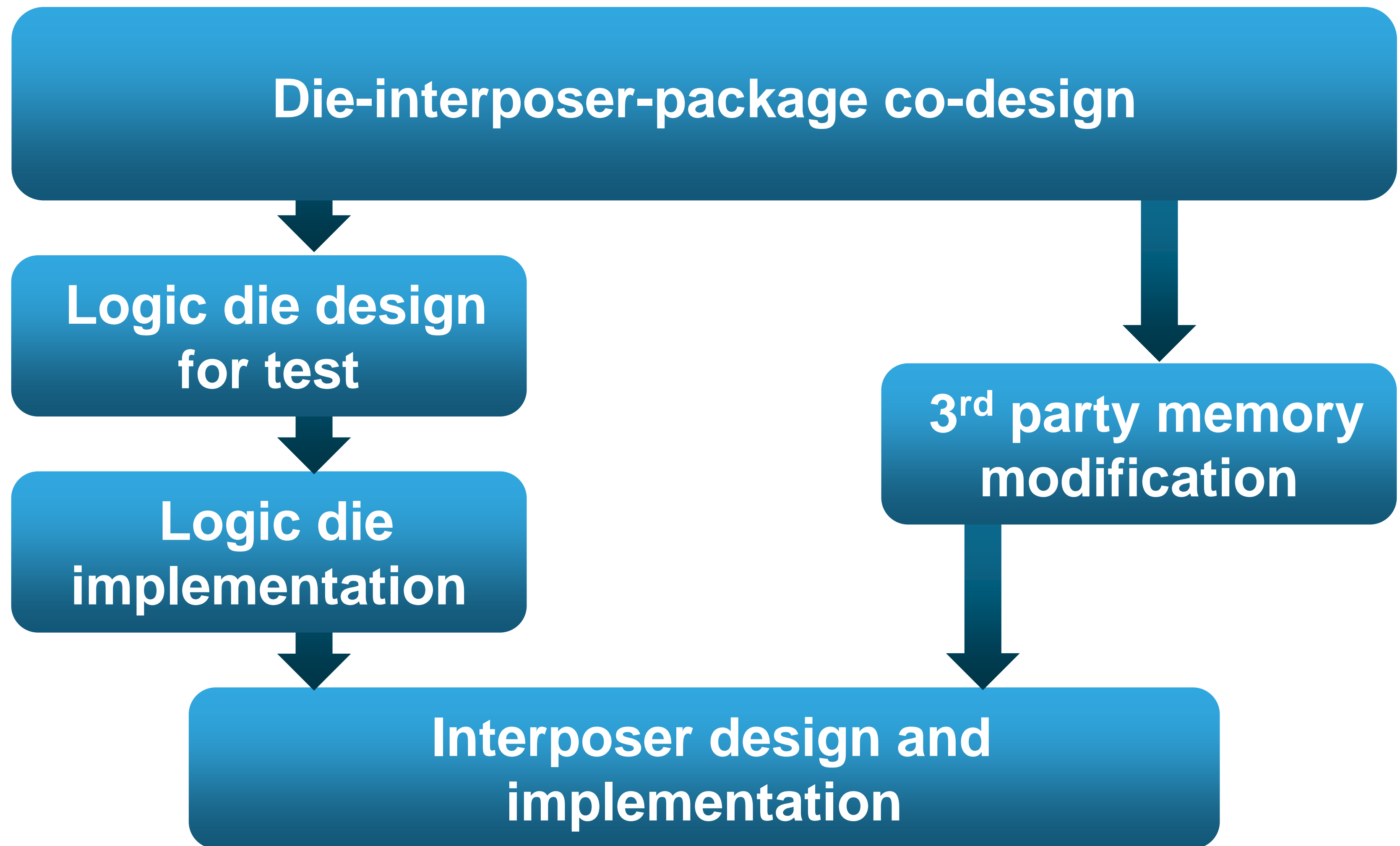
Example Design and implementation flow



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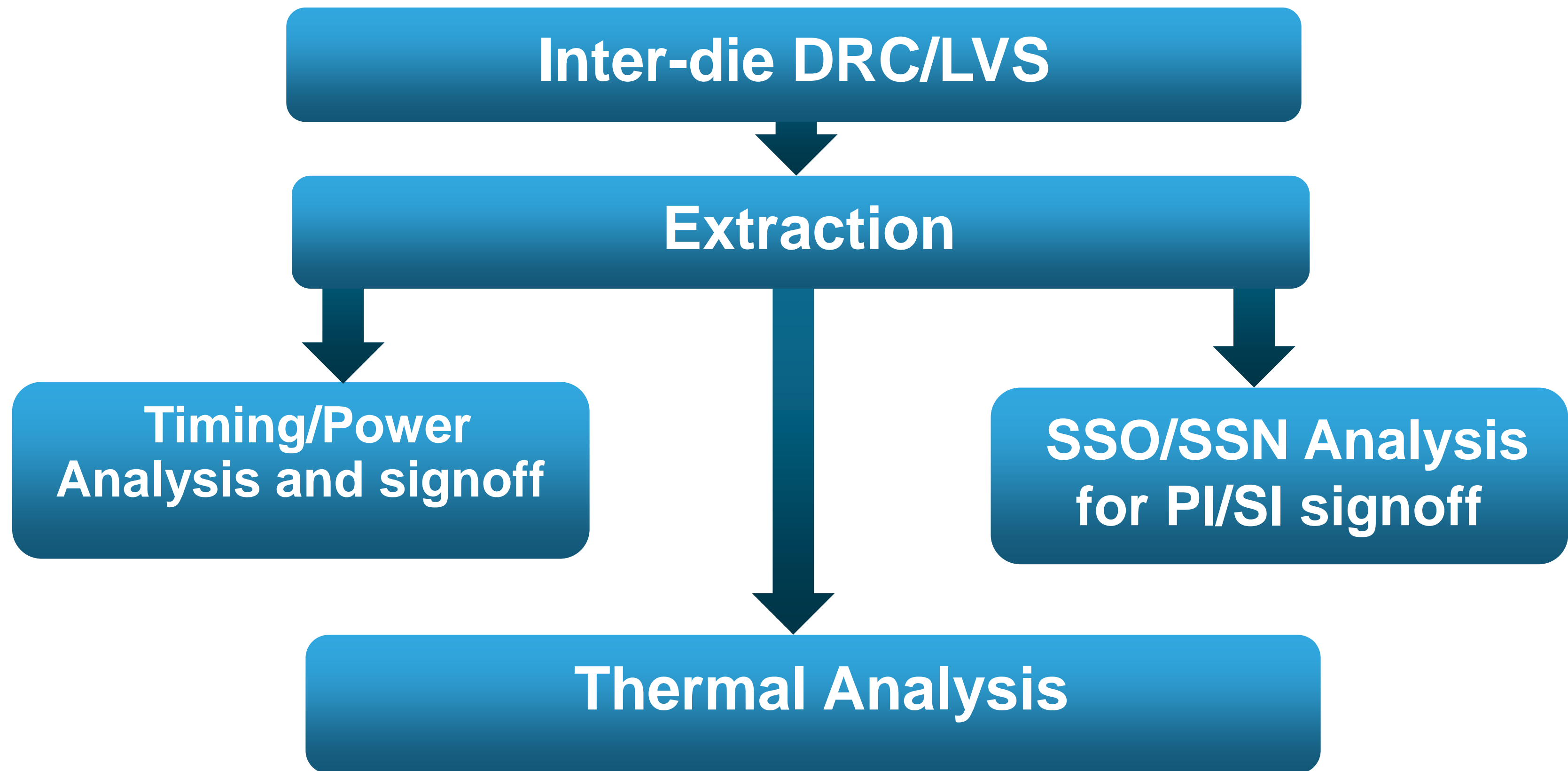
Example Analysis and signoff flow



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Summary

- 3D/2.5D can become an cost effective alternative to process scaling;

- 3D/2.5D realization involves entire design cycle with multiple 3D featured tools working together:
  - Planning,
  - Implementation,
  - Electrical and Thermal Analysis, Signoff
  - Manufacture Test;

- 3D/2.5D Implementation requires flexible platforms for design applications; An integrated flow will provide the holistic solution to 3D/2.5D Realization.

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