Verification and Extraction Solutions for 3D Stacks

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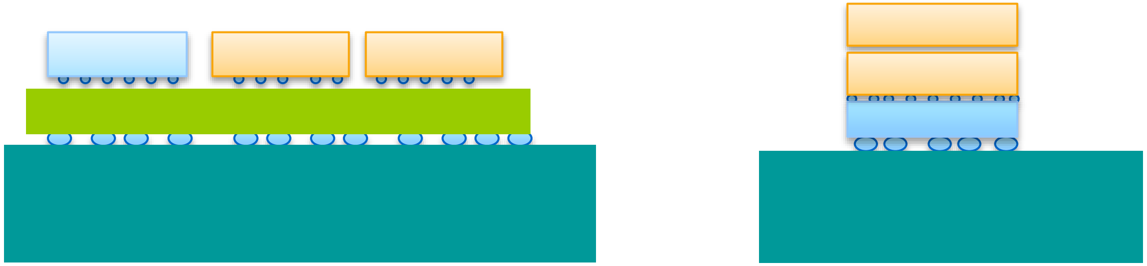
Outline

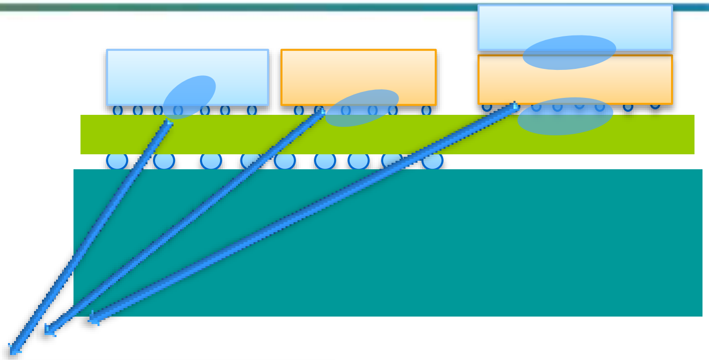
- Verification and extraction solutions
- Issues in TSV modeling
- TSV modeling approaches
- Fast Field Solver Based TSV Extraction
- Inter-die extraction

3D Stack Verification Solution

- Minimal disruption to existing verification flows
- Maintain standard DRC, LVS, PEX verification processes
  - Verify independent die/interposer
- Introduce 3D interface verification solution
  - Verify physical: offset, rotation, scaling, etc.
  - Trace connectivity of interposer, or die, to die
- Good for 2.D (interposer based) and full 3D configurations, analog and digital flows

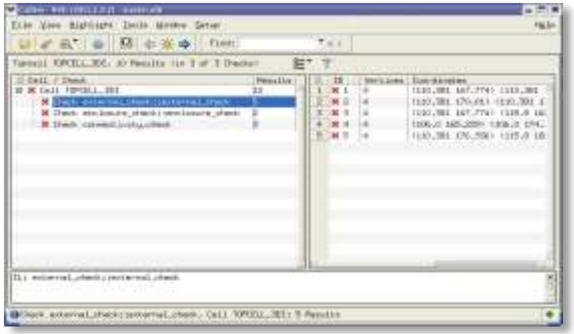


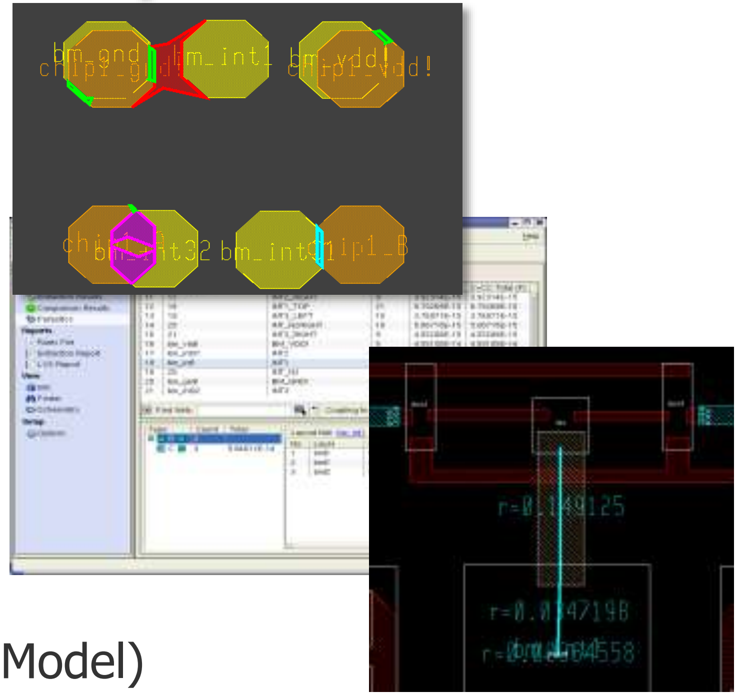
MG Stack Verification Flow



Calibre 3DSTACK

- Verify with micro-bumps are physically aligned
- Verify proper electrical connectivity through die2die and die2interposer interfaces





Calibre xRC/xACT3D

- Extract parasitics of Dies and Interposer interconnect
- Insert provided TSV circuit (Stand Alone TSV Model) into integrated parasitics/TSV netlists, or extract TSV

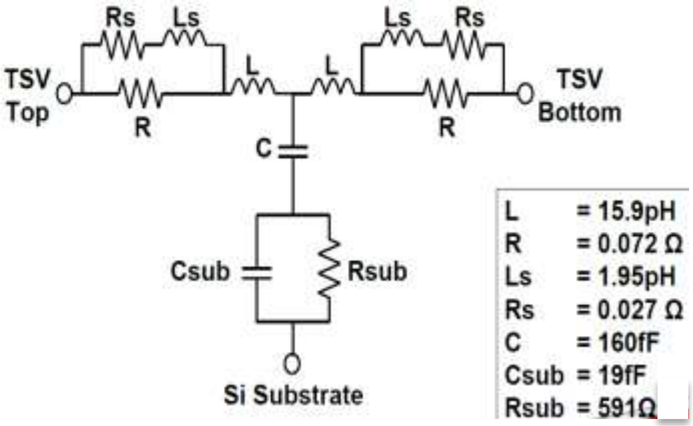
3DIC Flows and models for Analog and Digital

Analog flow

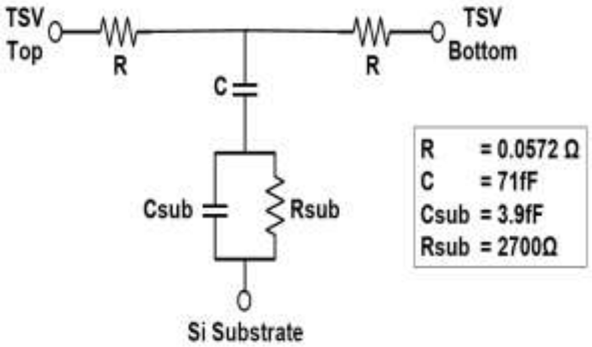
- Requires more accurate TSV model
- Treat TSV as a LVS device
- LVS device described by Spice subcircuit
- Spice simulation

Digital flow

- Lower accuracy requirements
- Treat TSV as a via
- Extraction tool generates R(C) model
  Can be replaced by provided model
- Static timing analysis



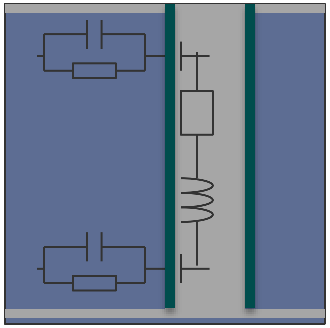
L = 15.9pH
R = 0.072 Ω
Ls = 1.95pH
Rs = 0.027 Ω
C = 160fF
Csub = 19fF
Rsub = 591Ω



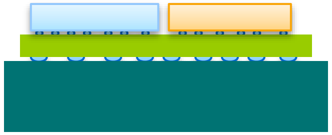
R = 0.0572 Ω
C = 71fF
Csub = 3.9fF
Rsub = 2700Ω

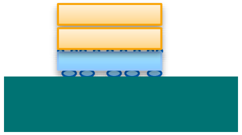
- Simpler RC model
- Inductors are ignored in digital flow

Issues in Stand Alone TSV Model Based Solution



- **Solutions based on provided TSV model**
  - TSV as LVS device or as a VIA
  - Circuit for TSV provided
    - Typically obtained by S-parameter measurements and circuit parameter extraction
  - Model of arbitrary complexity supported for TSV in analog simulation
  - Double-sided die front and back metal parasitic extraction
  - Sufficiently good for some applications (regular layout, no RDL, low density TSVs)

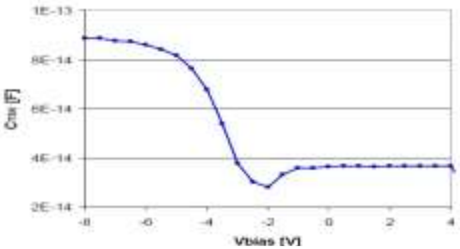


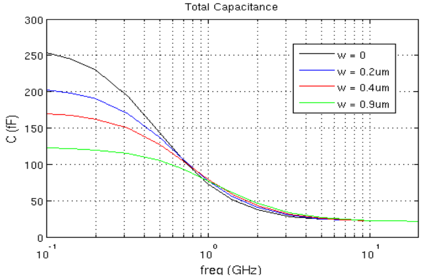


- **Problems with the stand alone TSV model solutions**
  - Not adequate for high density, high frequency applications
  - Problem with non-uniform environment around the TSVs
  - Does not account for TSV interactions with other TSVs, interconnect, devices

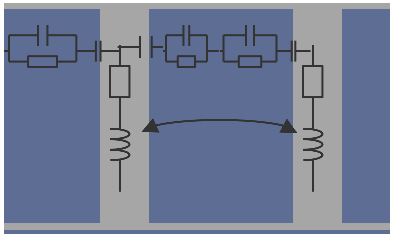
Issues in TSV Modeling

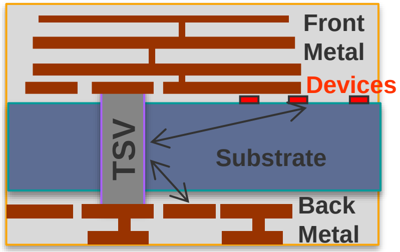
- Depletion region effects
  - TSD or TSV
    - Nonlinear behavior ; Capacitance vs. voltage across TSV
  - Frequency dependence
    - Strong non-linear frequency dependence





- Interactions between the TSVs
  - Capacitive and Inductive couplings
- Interaction between TSV and interconnect
  - Interactions with RDL and metal lines
- Impact of TSVs on device performance
  - Proper substrate description and modeling is needed



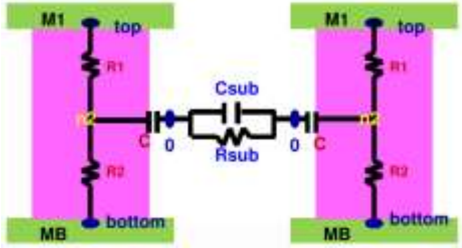


Alternative Modeling Approaches

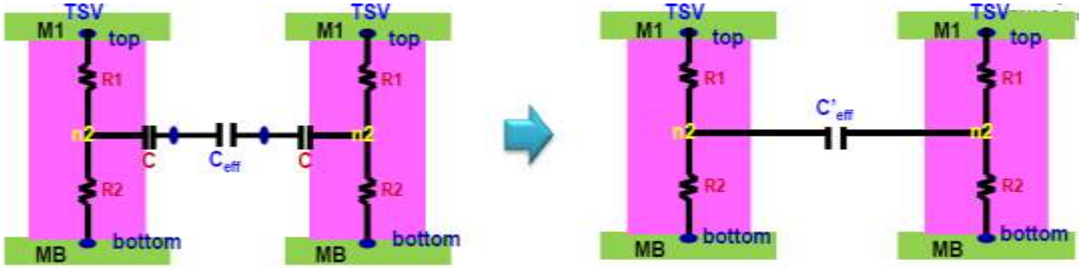
- **Single TSV models**
  - Advantage
    - Easy to integrate into a flow ; Sufficient for present needs
  - Challenges
    - Not adequate for high density, high frequency applications
- **Compact parametrized models**
  - Advantage
    - Can account for some interactions; Faster than FS
  - Challenges
    - Hard to account for all situations, to parameterize for all important variables
- **Field solver approach**
  - Advantage
    - Most accurate
  - Challenges
    - Performance; Integration

Compact Models, Examples

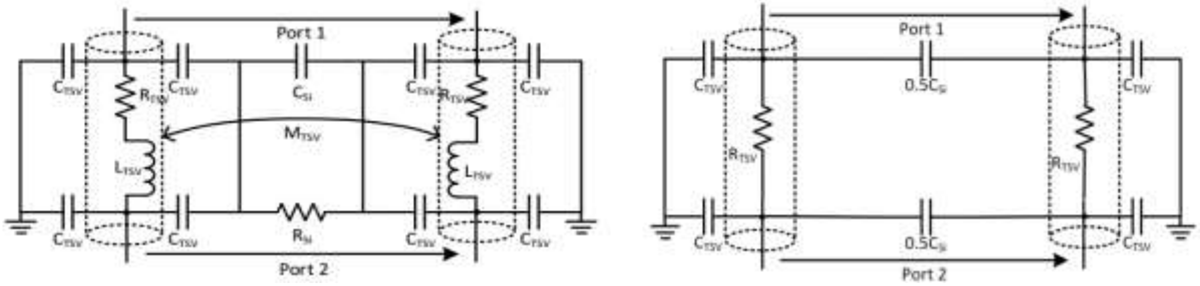
Model - foundry



- Stand alone TSV models provided for typical geometry and material properties
- Coupling parasitics dependent on spacing and frequency
- Ceff needed for STA



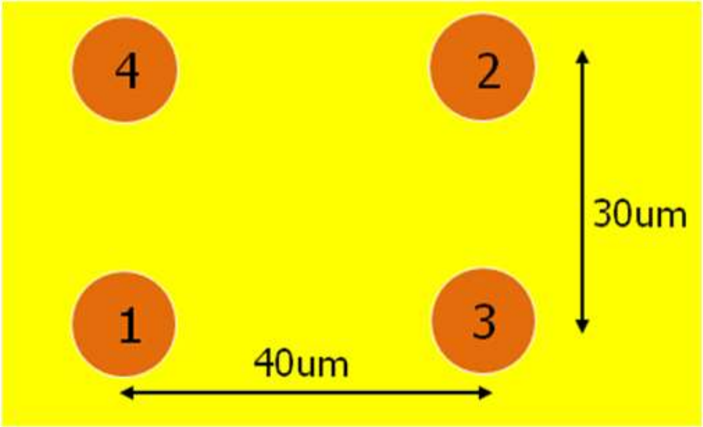
Model- academia

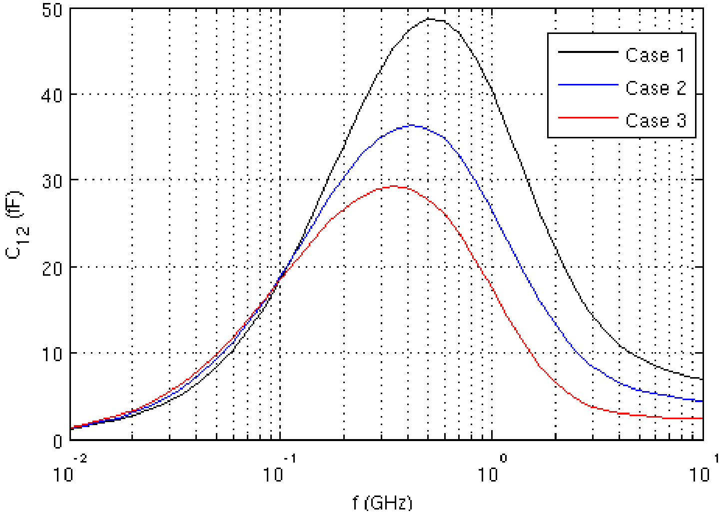


- Parametrizes TSV parasitics and Cap and Ind couplings
- Takes into account environment

Limitations of Compact models

- Calculated the mutual capacitance between TSV 1 and TSV 2:
  - Case 1: TSV 3 and TSV 4 are not present in layout
  - Case 2: TSV 4 is not present in layout
  - Case 3: All 4 of the TSV’s are present



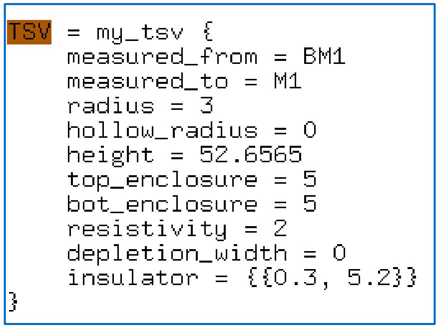


- Very strong dependence of capacitance on the environment

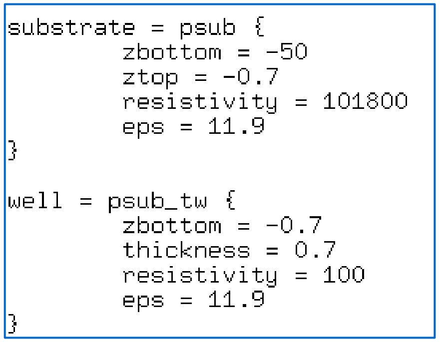
Attributes of MG FS-based TSV Extraction

- Field Solver Based Solution
  - Ensures accuracy
- Quasi-Static Capacitance Solver
  - Frequency Dependent Capacitance/Conductance
- Quasi-static Inductance Solver
  - Frequency Dependent Resistance/Inductance
- Integration to circuit verification flow
  - Minimum Changes to the Input Side
  - Output: Spice Netlist of frequency independent elements
- High accuracy
- Capability of Almost Linear Complexity of the field solver

MG Solution For 3D-IC Extraction (Engine)

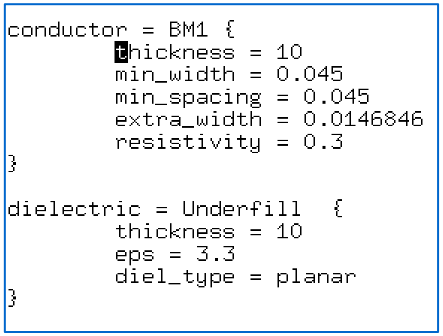


```
TSV = my_tsv {
    measured_from = BM1
    measured_to = M1
    radius = 3
    hollow_radius = 0
    height = 52.6565
    top_enclosure = 5
    bot_enclosure = 5
    resistivity = 2
    depletion_width = 0
    insulator = {{0.3, 5.2}}
}
```



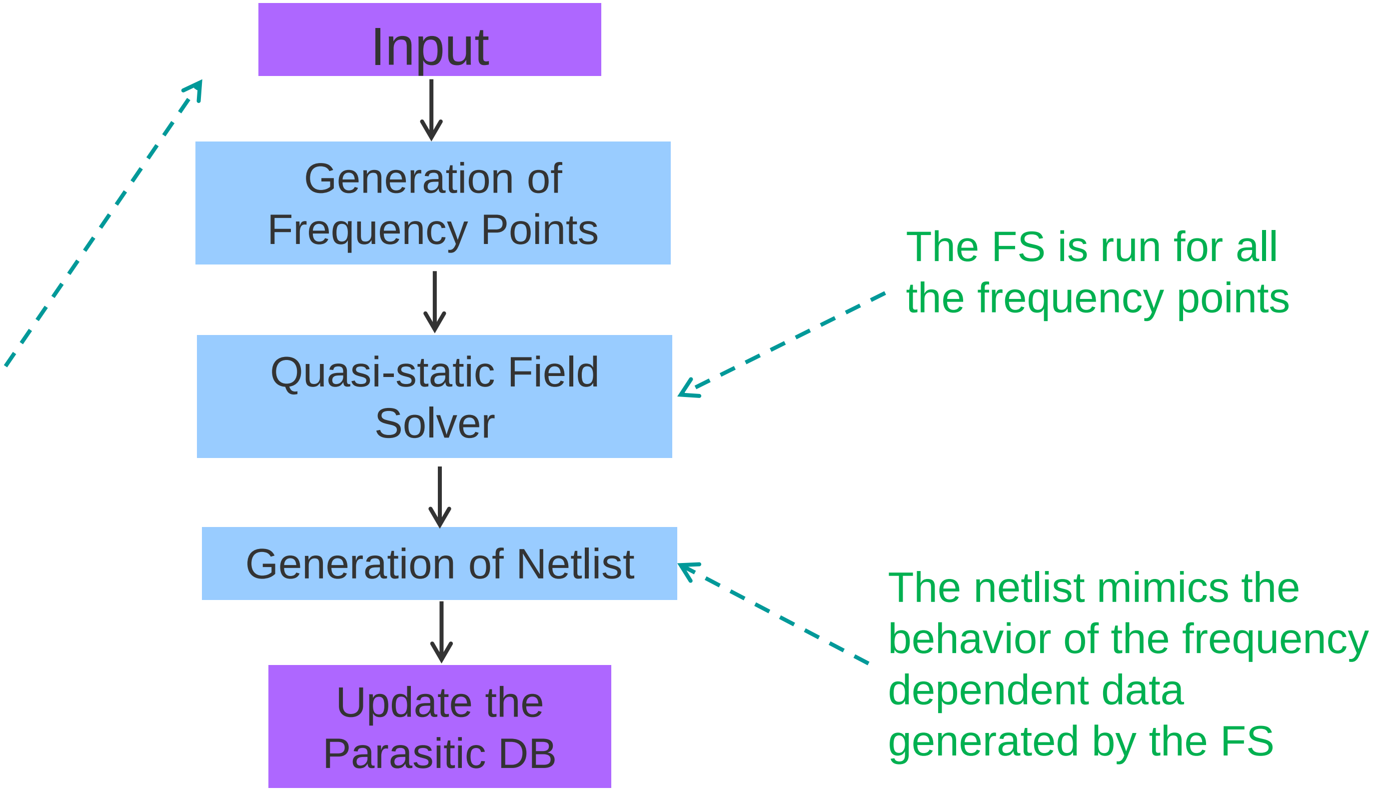
```
substrate = psub {
        zbottom = -50
        ztop = -0.7
        resistivity = 101800
        eps = 11.9
}

well = psub_tw {
        zbottom = -0.7
        thickness = 0.7
        resistivity = 100
        eps = 11.9
}
```



```
conductor = BM1 {
        thickness = 10
        min_width = 0.045
        min_spacing = 0.045
        extra_width = 0.0146846
        resistivity = 0.3
}

dielectric = Underfill  {
        thickness = 10
        eps = 3.3
        diel_type = planar
}
```



Input

Generation of Frequency Points

Quasi-static Field Solver

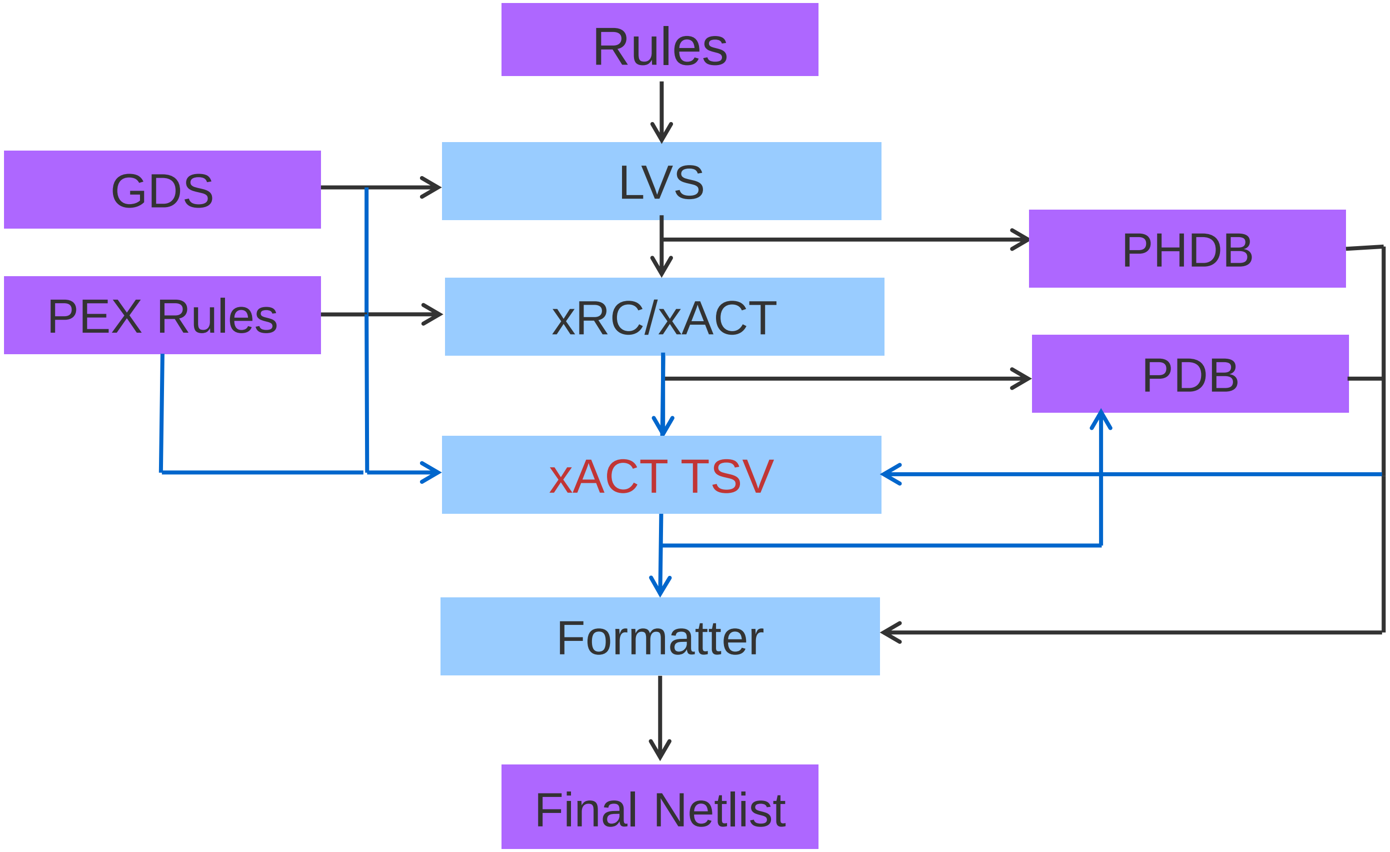
Generation of Netlist

Update the Parasitic DB

The FS is run for all the frequency points

The netlist mimics the behavior of the frequency dependent data generated by the FS

MG Solution For 3D-IC Extraction (Flow)


Rules

GDS

LVS

PHDB

PEX Rules

xRC/xACT

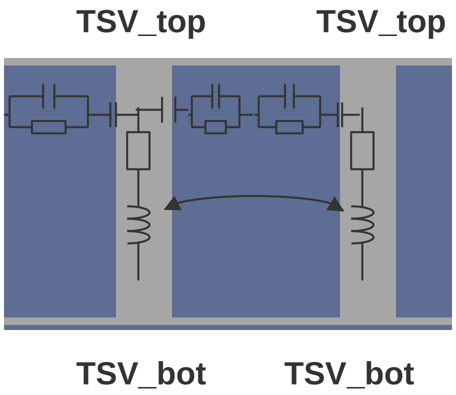
PDB

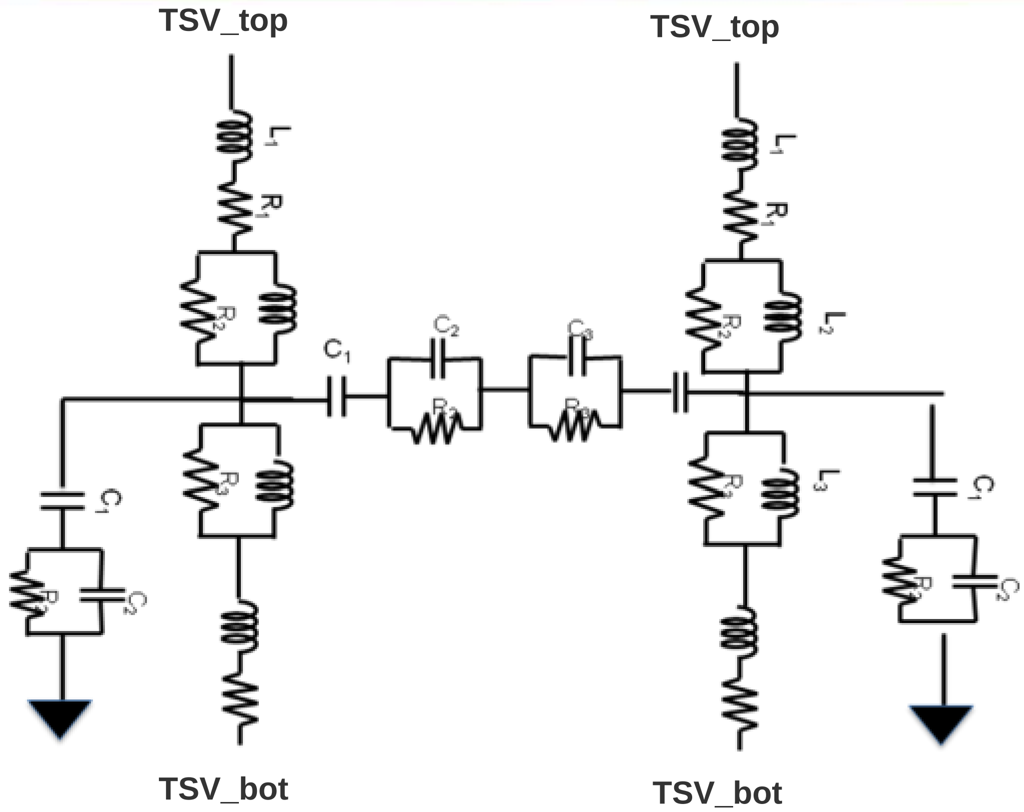
xACT TSV

Formatter

Final Netlist

MG Fast Field Solver Output



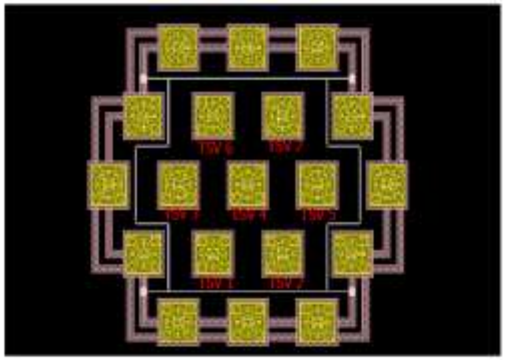


Output:

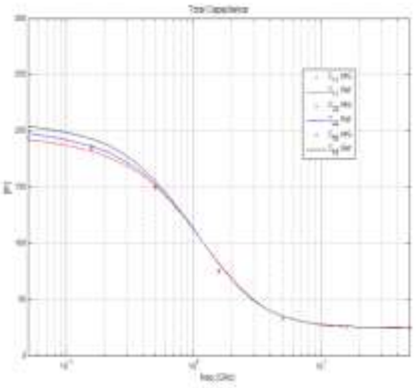
Netlist of frequency-independent linear elements. Values of those elements are computed by fitting the frequency dependent results of the field solver

Engagements and Accuracy Results

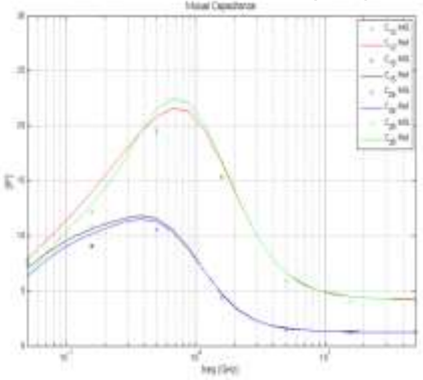
- Engaged with major foundries and customers
- Working on interposers-based (2.5D) and true 3D stacks
- Test chips and real designs
- Accuracy results (compared with full wave solvers)
- Performance very good; To be further improved w/parallelization and pattern matching



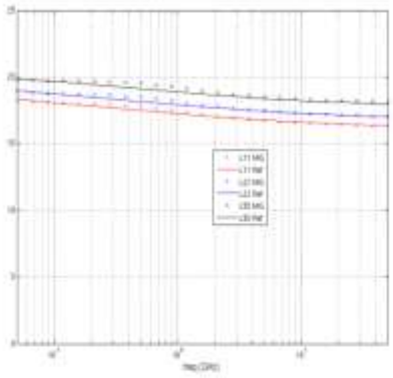
Total C



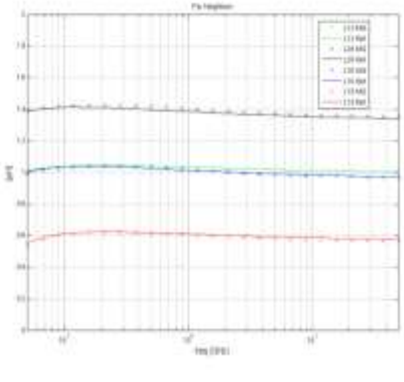
Coupling C



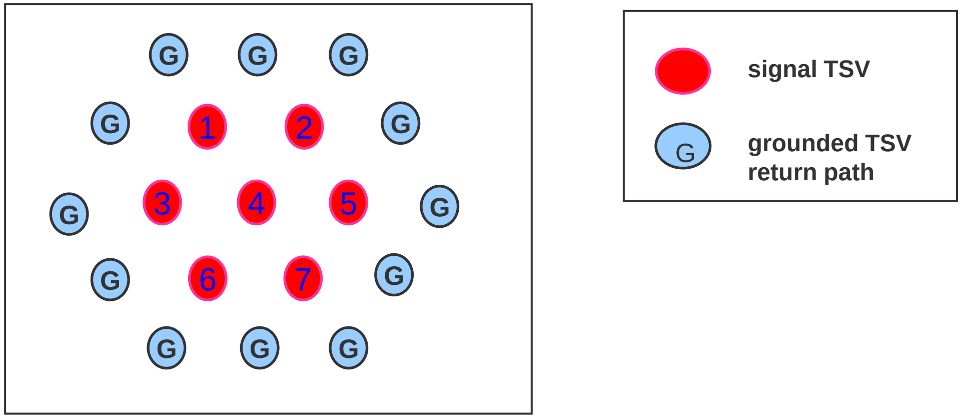
Self L



Mutual L

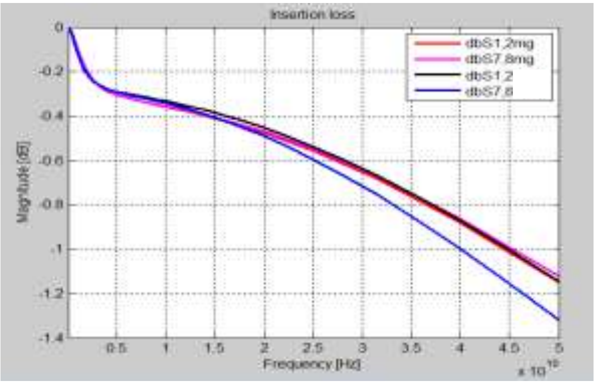


Insertion Loss, Reflection, Insulation



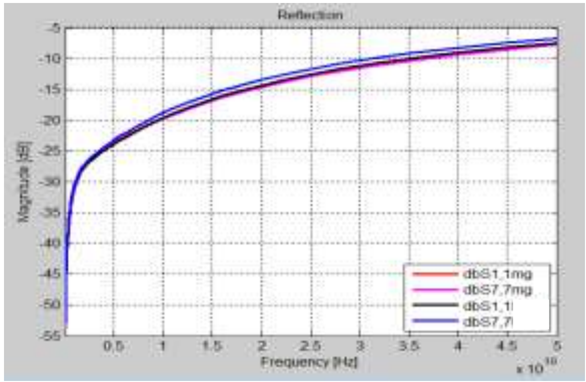
TSV1:	port1,	port2
TSV2:	port3,	port4
TSV3:	port5,	port6
TSV4:	port7,	port8
TSV5:	port9,	port10
TSV6:	port11,	port12
TSV7:	port13,	port14

Insertion Loss



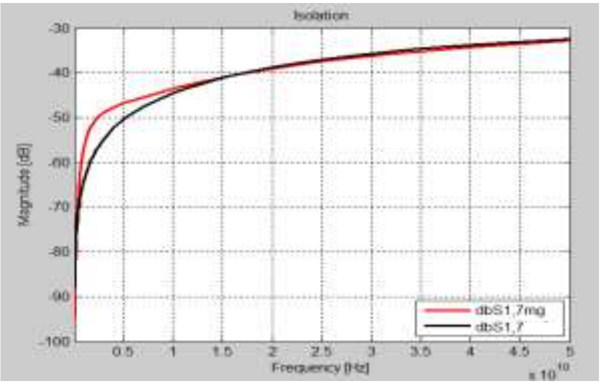
MG vs. Ref, dbS1,2 (port_m=1, port_n=2) and dbS7,8 (port_m=7, port_n=8)

Reflection



MG vs. Ref, dbS1,1 (port_m=1, port_n=1) and dbS7,7 (port_m=7, port_n=7)

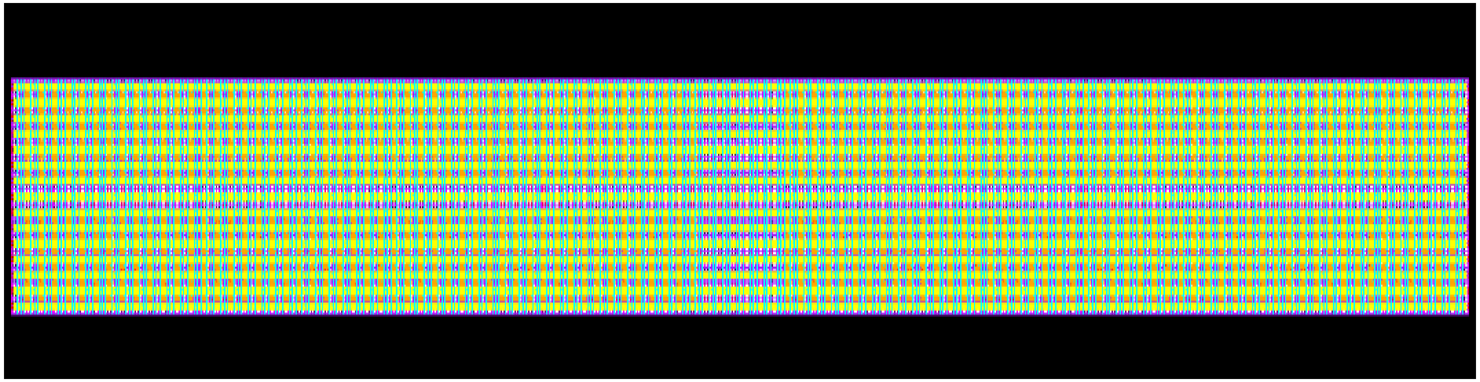
Insulation



MG vs. Ref, dbS1,7 (port_m=1, port_n=7)

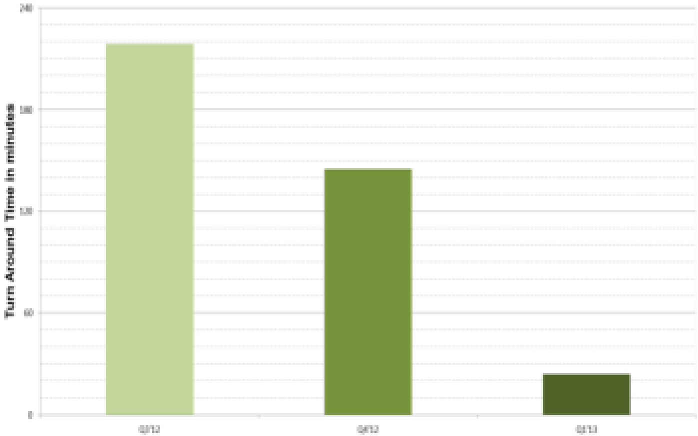
xACT-TSV Performance

- *Performance for Wide I/O Application*



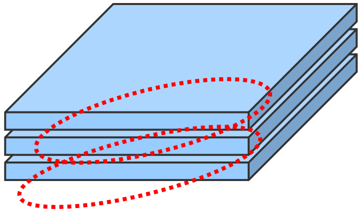
- 1200 TSV + Cu-Pillars Performance Improvement
  - Q1 2013: 0h24min

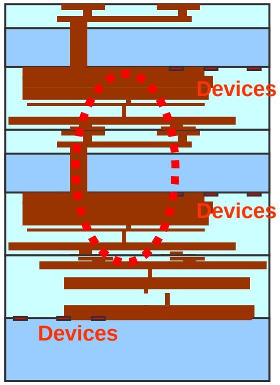
- It now takes less then a 1sec to extract TSV, all its interactions and do netlisting. There is loot of room for improvement by parallelization and “pattern matching”



Inter-die interactions

- Inter die Capacitive coupling
  - might not be negligible between the dies, especially in Face-to-Face connection
- Magnetic coupling between the dies
  - The dies are getting closer together
  - Overlapping loops between the dies

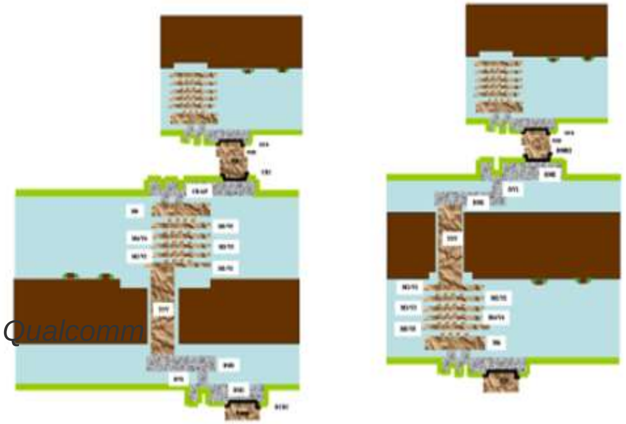




- Full stack IR drop is needed
  - As number of TSVs is increasing the interactions are becoming stronger and IR drop analysis has to be done simultaneously for the entire stack
- Inter die paths
  - the paths go across the dies and LVS, extraction and simulation have to go across the dies.

Dies Interface

- Bump/Pillar bonding is common

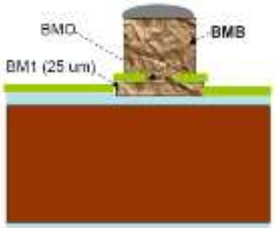


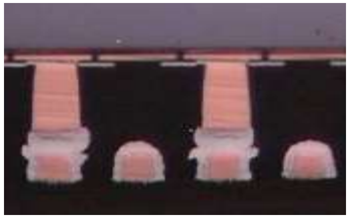
Source: Qualcomm

(a) AF-AF Bonding

(b) AF-BF Bonding (2BM)

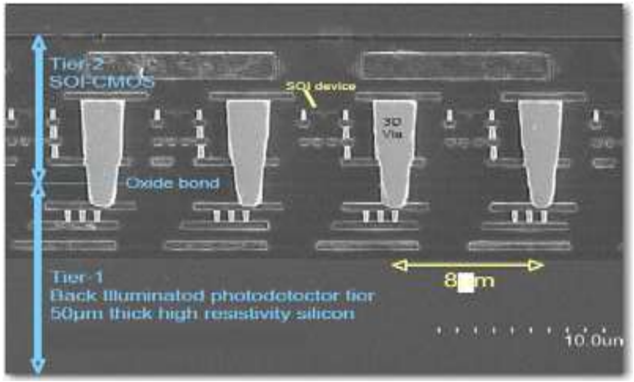
- Bump/Pillar modeling, interactions and shielding



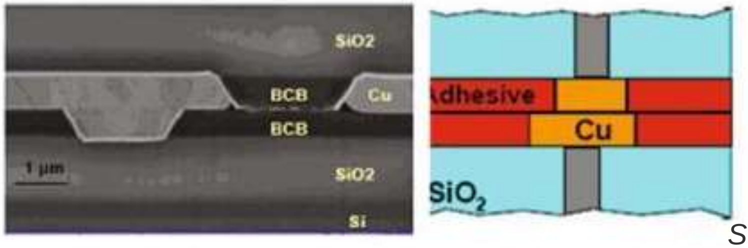


pillars

- Other bonding techniques (not of interest for this work)



Oxide Bonding – MIT Lincoln Lab



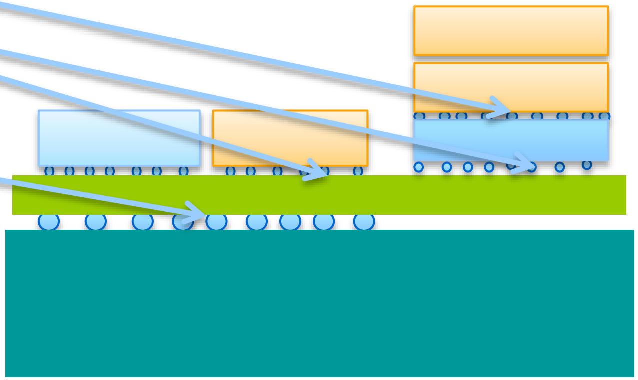
Source: RPI

Fig. 1.35 A die-Stack using a combination of Cu-Cu and BCB adhesive bonding at RPI [14]

Cu-Cu Bonding

Inter-die description

- Describe geometry and materials for inter-die region
  - Die –to die
  - Die –to- interposer
  - Die(or interposer) to package
- Geometrical
  - Distance between the dies
  - Pillars
  - Bumps
    - Micro-bumps
    - C4s
- Material
  - Inter die material properties (usually under-fill)
  - Material properties of the pillars and bumps
- MIPT is extended for the die bonding description



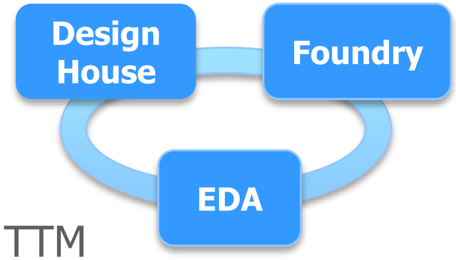
Enabling 3D Stack parasitic extraction

- Options:
  - Flat MIPT
    - Would not be practical
  - Hierarchical MIPT
    - Individual die + Inter-die area MIPTs + top level description
  - Expanded single die MIPT
    - would include single chip MIPT + above and below inter-die + pillars/bumps + specified number of adjacent dies layers
  - Expanded inter-die MIPT
    - Inter-die + pillar/bumps + specified number of adjacent dies layers

- Incremental calibration
- FS extract the interfaces (and the TSVs)
- Rule based tool extracts interconnect
- Tool produces system level netlist with parasitics

Summary

- 3D stacking is reality
  - Lot of recent activities and announcements
    - TSMC, Samsung, GF, UMC, Tezzaron,…
  - 2.5D and 3D configurations, various strategies and business models
  - Volume production expected in 2014/15
- There is need for accurate TSV modeling, including substrate and interactions
  - Various solution proposed: stand alone TSV, parametrized models, …
  - Mentor’s field solver based extraction: accurate and fast
- Chip interface modeling is now being considered
  - Fast inter-die links
  - Interface description and parasitic extraction
  - System level netlist and simulation
- Collaborative partnerships are crucial
  - Early cooperation eliminates redundant efforts and improves TTM
  - Results in timely, differentiating solutions



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