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20-nm (Planar) Mixed-Signal IP
A Stepping Stone To FinFET?

Navraj Nandra

April 2013

- Is this true?
- Is this the right question from a mixed-signal designer’s perspective?

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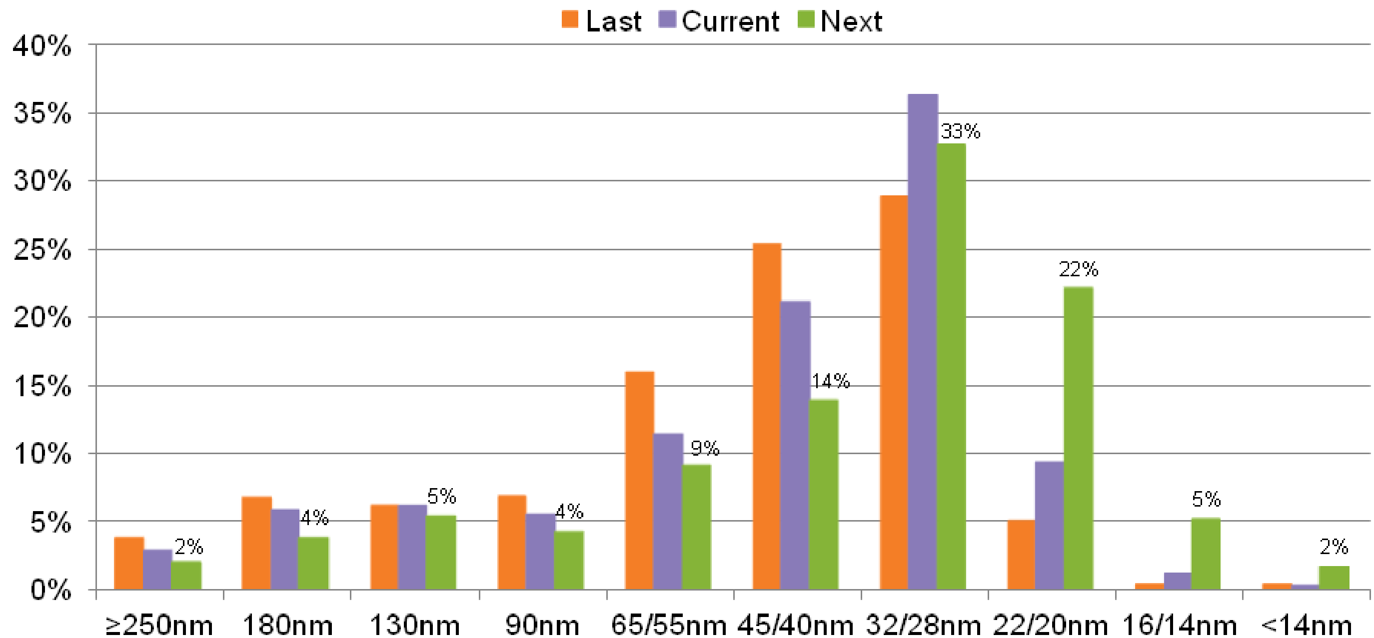
Recent Industry Comments Supporting The "Stepping Stone"

"To accelerate FinFET efforts foundries are looking at hybrid integration schemes and "modular fin" strategies"

"By being modular, vendors have the option to plug in the FinFET into an existing 20-nm planar BEOL flow."

Power, Performance, Area (PPA)
Driving Node Migration



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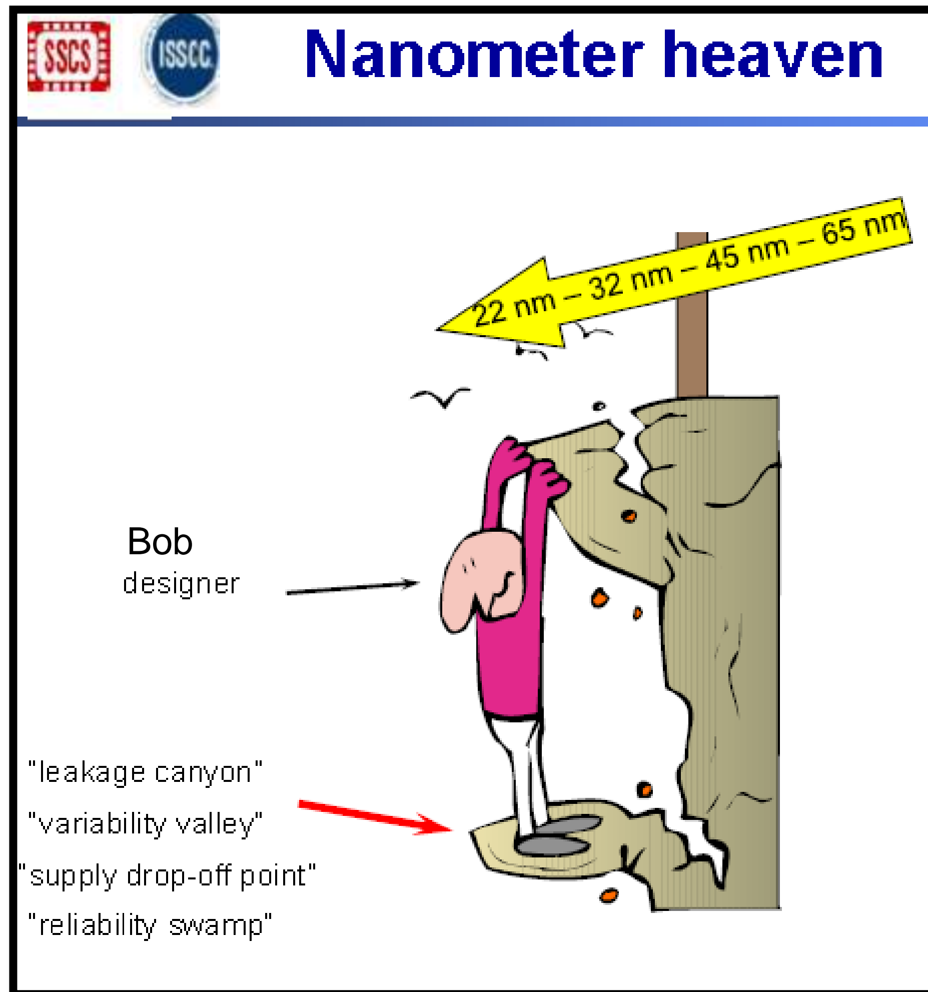
Bob’s Challenge



- 65-nm to 20-nm planar has involved design challenges to meet PPA in an SoC
- Can the planar architectures, know-how be applied to FinFET designs?

Is it a stepping stone?

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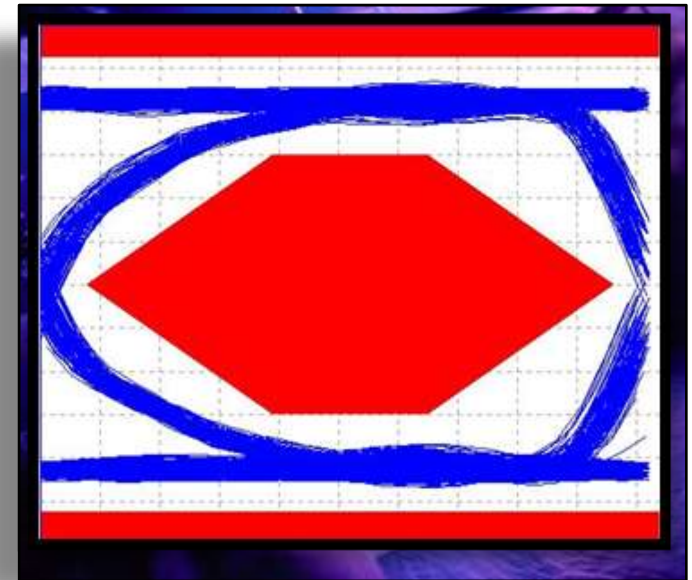
Agenda

20-nm Design Requirements

Advanced Design Methodology

Stepping Stone To FinFET

Summary



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Agenda

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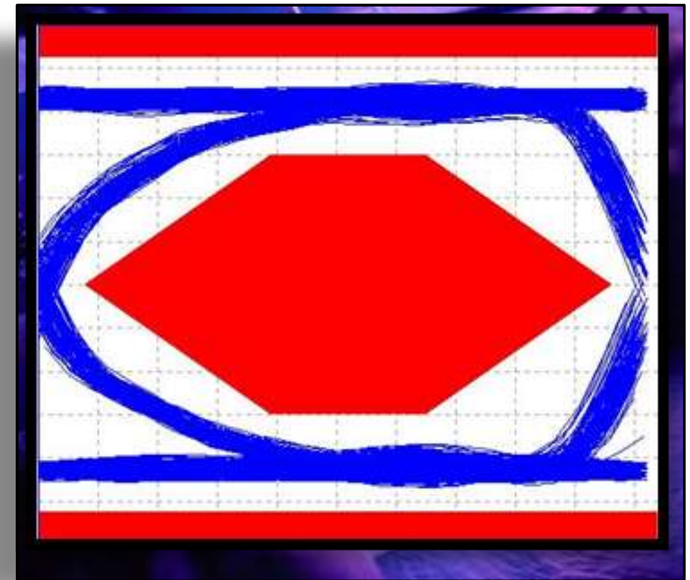

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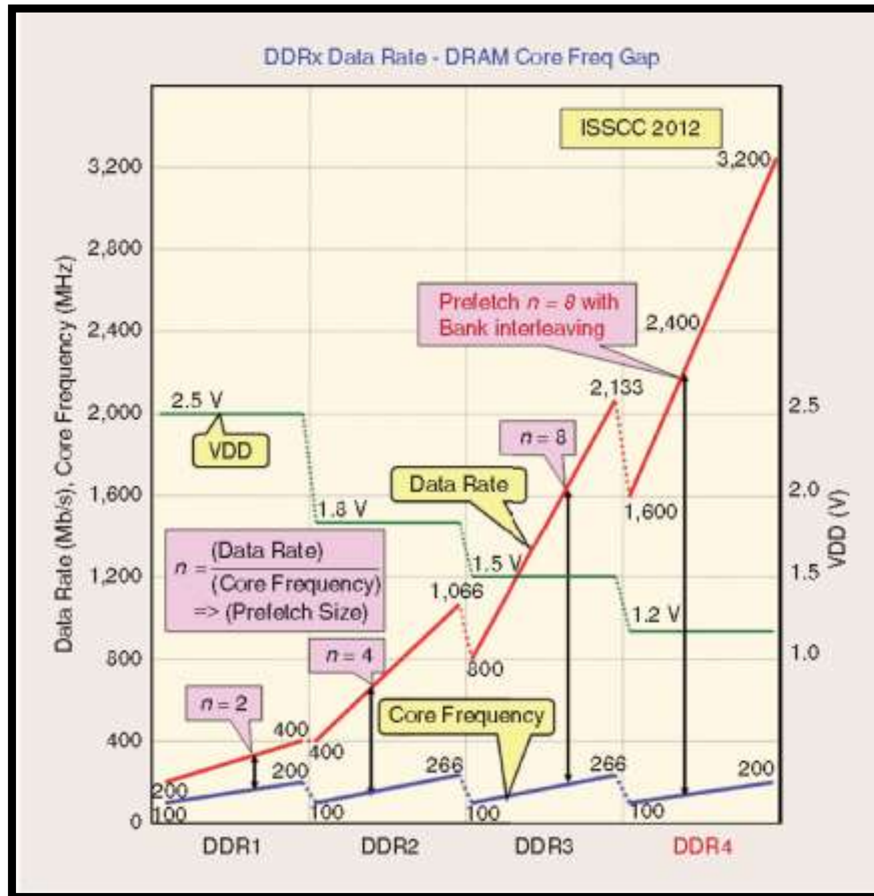
LPDDR3 – *Drives Foundry I/O Strategy*
DDR4 – *Drives Speed*



PPA target: DDR4 speed; LPDDR3 speed/low power

Specifications

- Evolving serial/parallel termination schemes
  - DDR4 is series + parallel to VDDQ
  - LPDDR3 tries to avoid termination
- Single ended interface
- DDR4: 1.2V 3.2 Gb/s
- LPDDR3: 1.2V 1600 Mb/s
- Need larger pre-fetch size,
  bank interleaving

20-nm design challenges

→ Better density, but *Vt* not scaling

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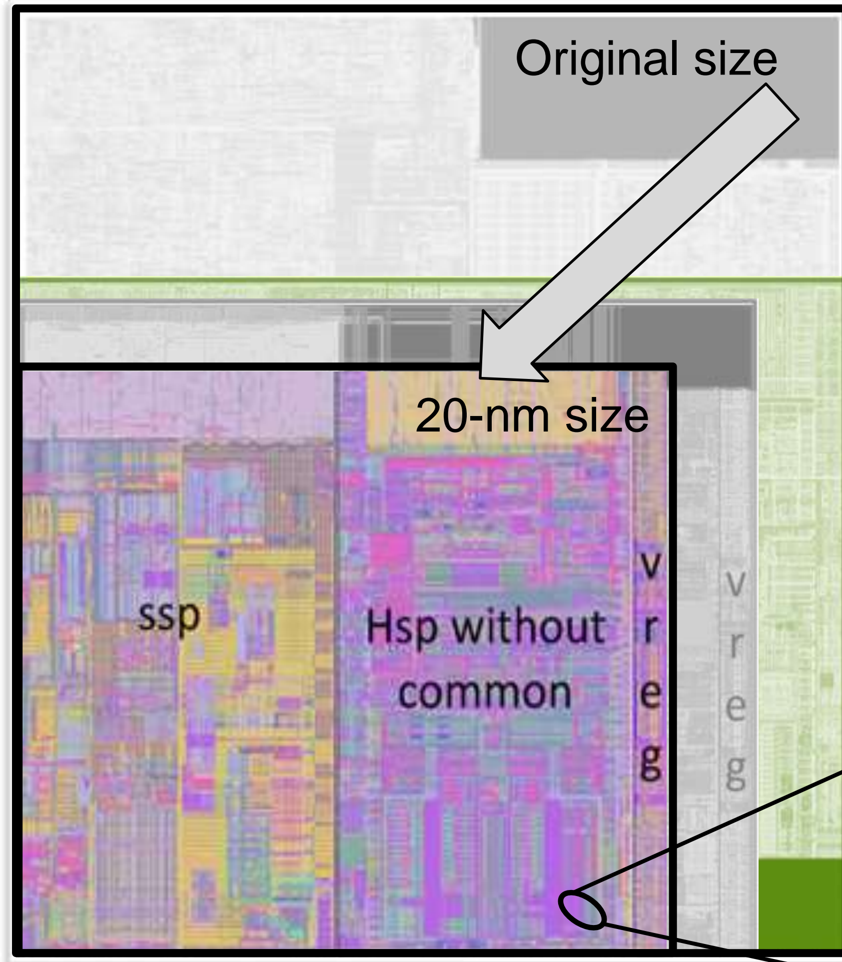
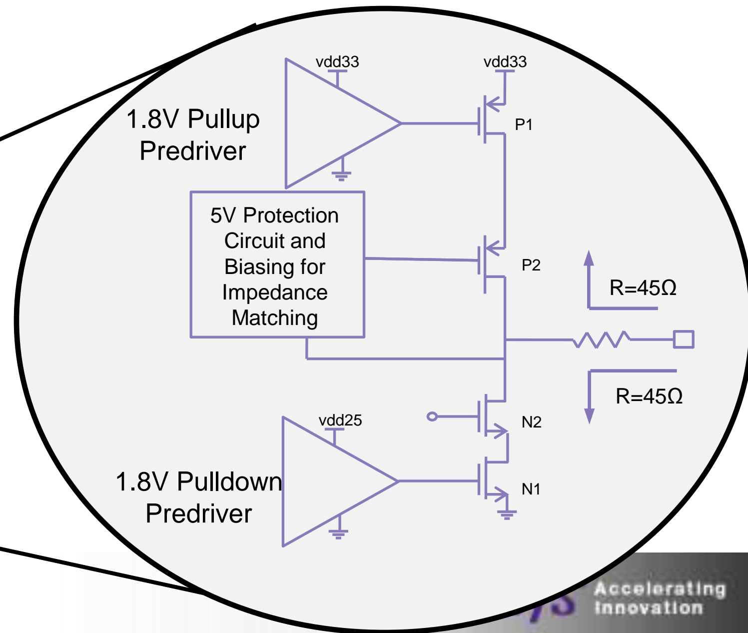
USB 3.0, 20-nm 1.8V I/O

Smaller area and electrical compliance must be met



- **Must support all four USB speeds:**
  5 Gb/s, 480 Mb/s,12 Mb/s, 1.5 Mb/s
- **5 V USB electrical compliance requirement**
  - Must be met using devices 1.8 V devices
  - Guaranteed device reliability meeting 3.3 V signal swings during Full Speed & Low Speed USB operation
  - Successfully operates after shorting the differential signal pair to 5 V for 24 hours
- **NBTI (high voltage overstress)** will impact receiver squelch threshold → causing electrical compliance failure



PPA target
Area reduction; 5V battery charging; all 4 USB speeds

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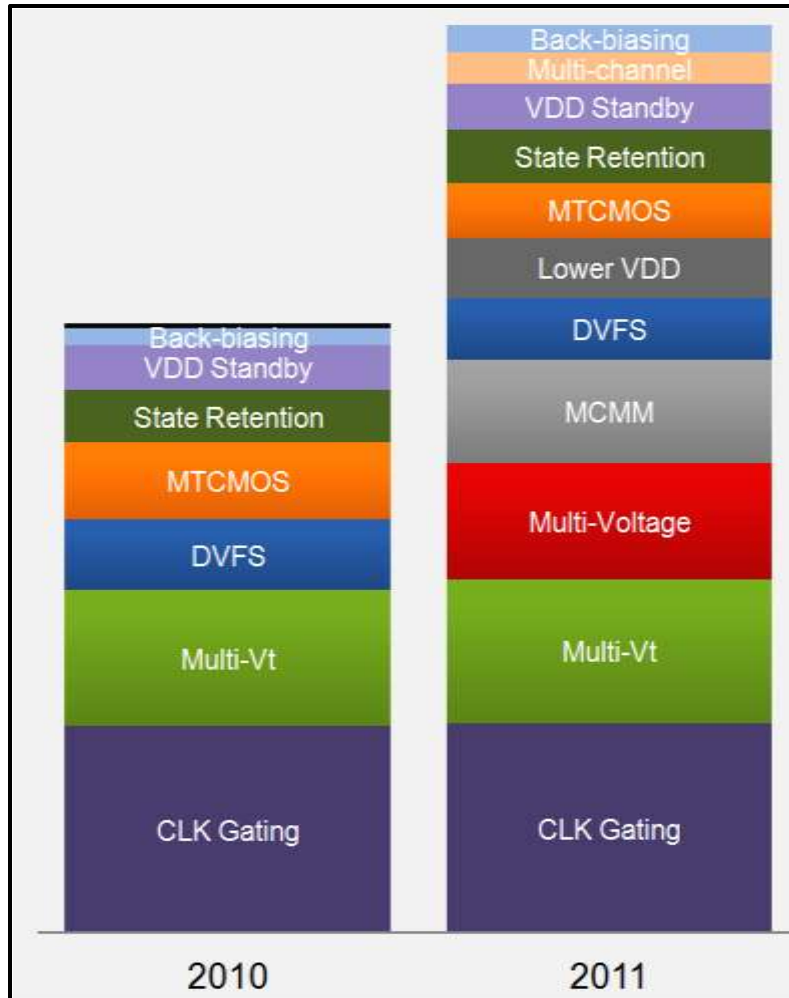
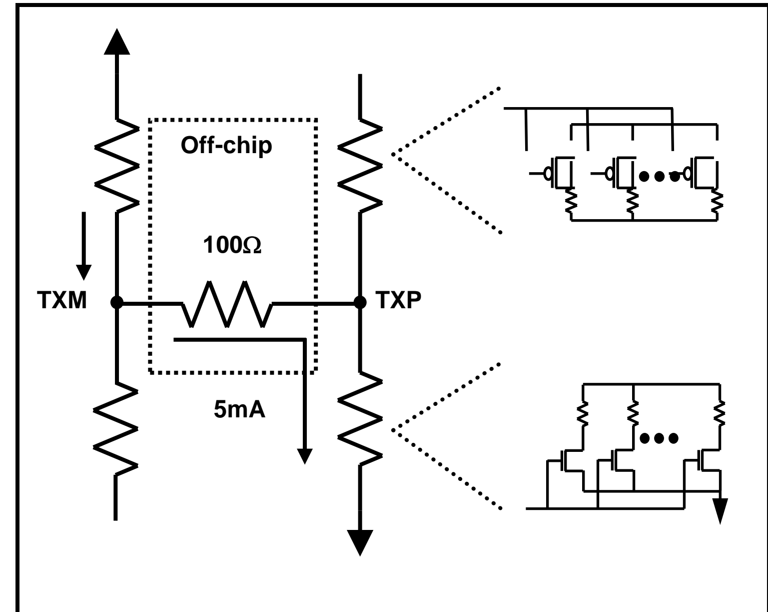
PCI Express: Lowering Power

Design techniques plus new specs





Low-power design techniques

Low-power architectures

New PCI Express specifications

PPA target: speed, new low power modes

Source: 2011 Synopsys Global User Survey. May only be used with authorization from Synopsys.

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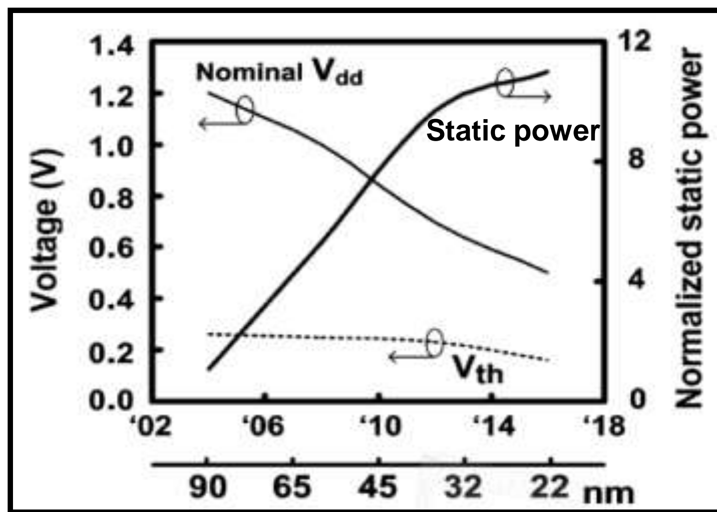
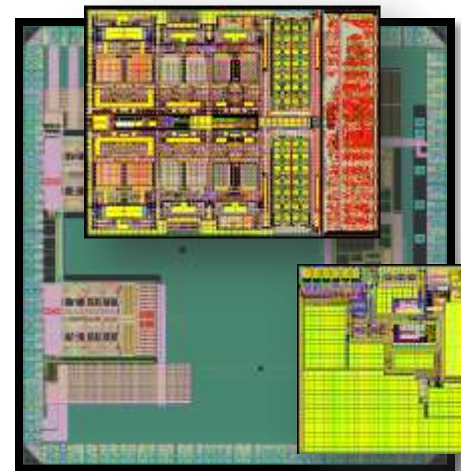
Data Converters
Meeting dynamic range

- Supply voltage almost halved from 65-nm to 20-nm
- Analog video / audio dynamic range > 1.3V means no voltage headroom for high linearity @ 1.8V supply
- Flicker (1/f) noise inversely proportional to transistor length (L)
- New analog techniques: clock boosting circumvents low supply voltage, internally processing signals with large voltage swings



Source: ITRS roadmap, supply voltage and threshold voltage



Synopsys : LTE analog front-end using 1.8 V

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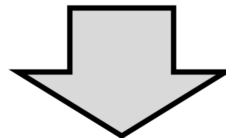
20-nm PPA Requirements

IP Specifications:

- DDR4, LPDDR4 → higher I/O speeds using single-ended interface
- USB 3.0 → must support all 4 speeds, meet electrical compliance
- PCI Express → 5 Gb/s, 8 Gb/s but support new low power modes
- Data converters → dynamic range versus lower voltage headroom

Market requirement:

- Physical IP scales (area, power) without performance degradation
- Supports aggressive schedules → designed on an early PDK
- Works on first instantiation in SoC



Requirements: advanced silicon design methodology and close co-operation with foundry

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20-nm Layout Dependent Effects

Semiconductor Process Requirements

- WPE
- LOD
- OSE
- PSE
- PO.DN.15
- Pattern Density Effect
- OPC (Optical Proximity Check)
- GDA (Gross Die Advisor) Criteria
- MFU (Mask Field Utilization) > 80%
- DFM LPC (Layout Patterning Check)
- HCI (Hot Carrier effect Injection)
- Dummy OD (DOD) rules
- Dummy Poly (DPO) rules
- SM (Stress Migration)
- NBTI
- PBTI
- PSM
- RTO

PPA Requirements For Physical IP

Agenda

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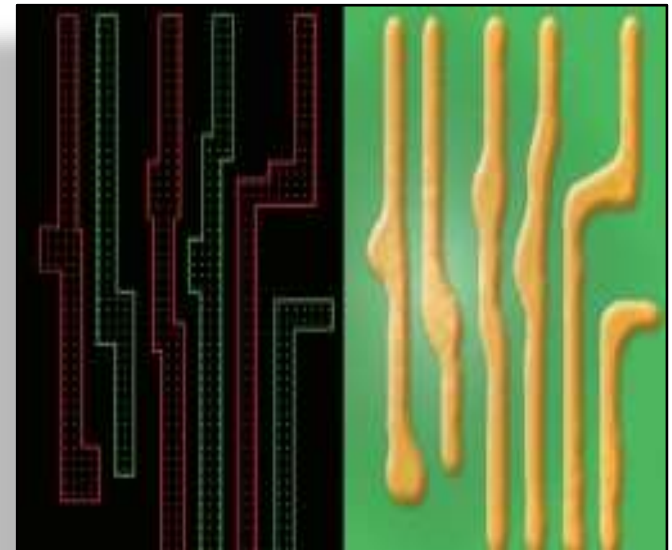
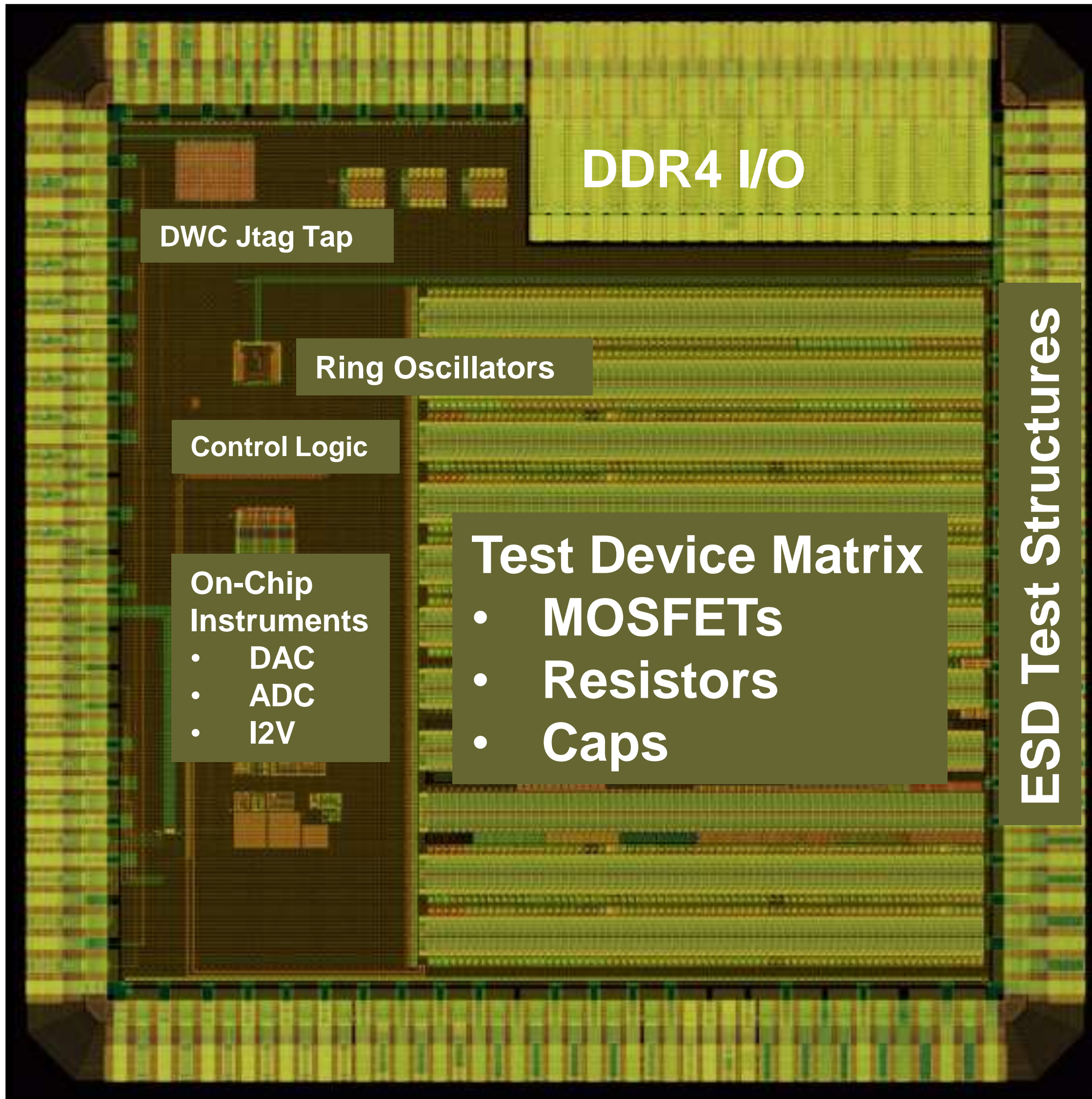


Enabling Robust IP Development

Analog Technology Assessment Chip



- CAD flow verification
- Correlate to simulation
- Fundamental IP structures:
  - Ring oscillators
  - DDR4 I/O
  - Analog IP
  - Test devices

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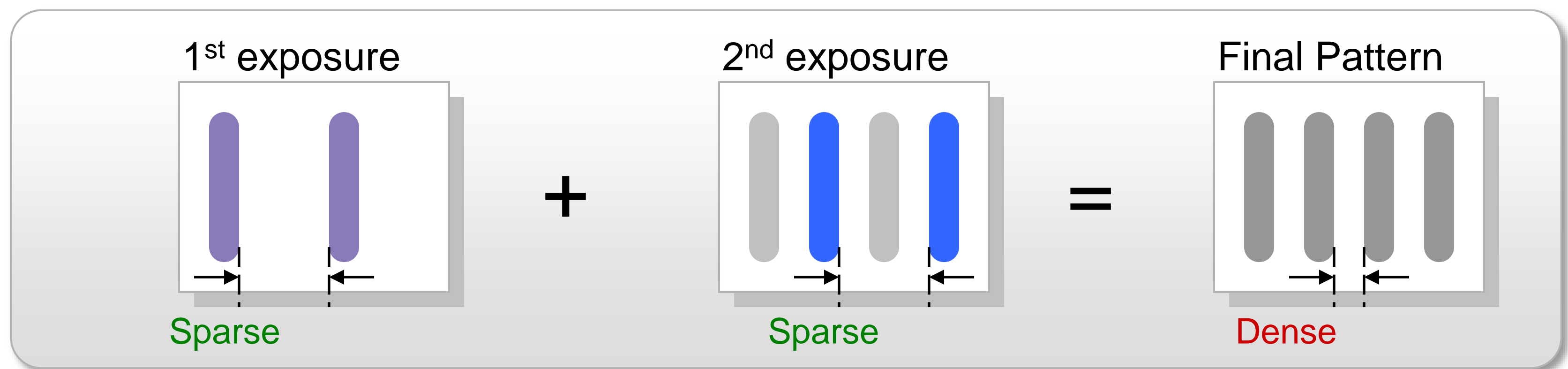
Technology Assessment Chip

Focused on analog/mixed-signal requirements

- **DPT (double patterning):** 1500 devices with different layouts and density dependencies providing data for resistor / transistor matching and metal mismatch
- **Analog performance, gate delay:** Ring oscillators and operational amplifiers give early insight
- **Electro-static discharge:** Need to be designed for HBM and CDM performance – for example CDM must be tested across different voltage domains
- **Ability to overstress devices:** Evaluate the reliability degradation due to NBTI, PBTI and HCI



Dense pattern can be split into two sparse patterns

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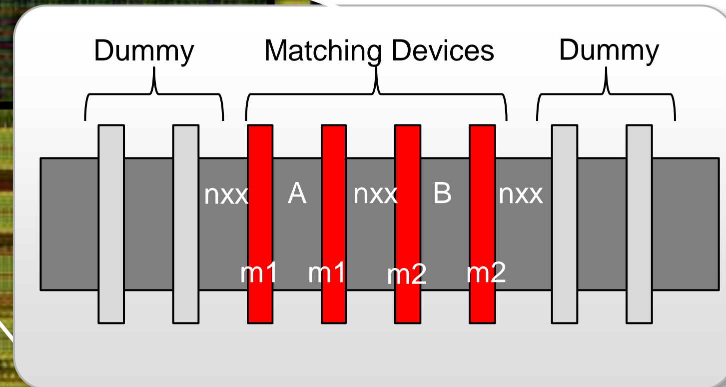
Test Matrix



On-Chip

- Device-Under-Test matrix
- I-to-V conversion
- DAC
- Current compare
- Fast BIST testing
- 1,500 test devices
- Matching & density aware

Gate Matching guidelines
Density rules optimized for analog matching

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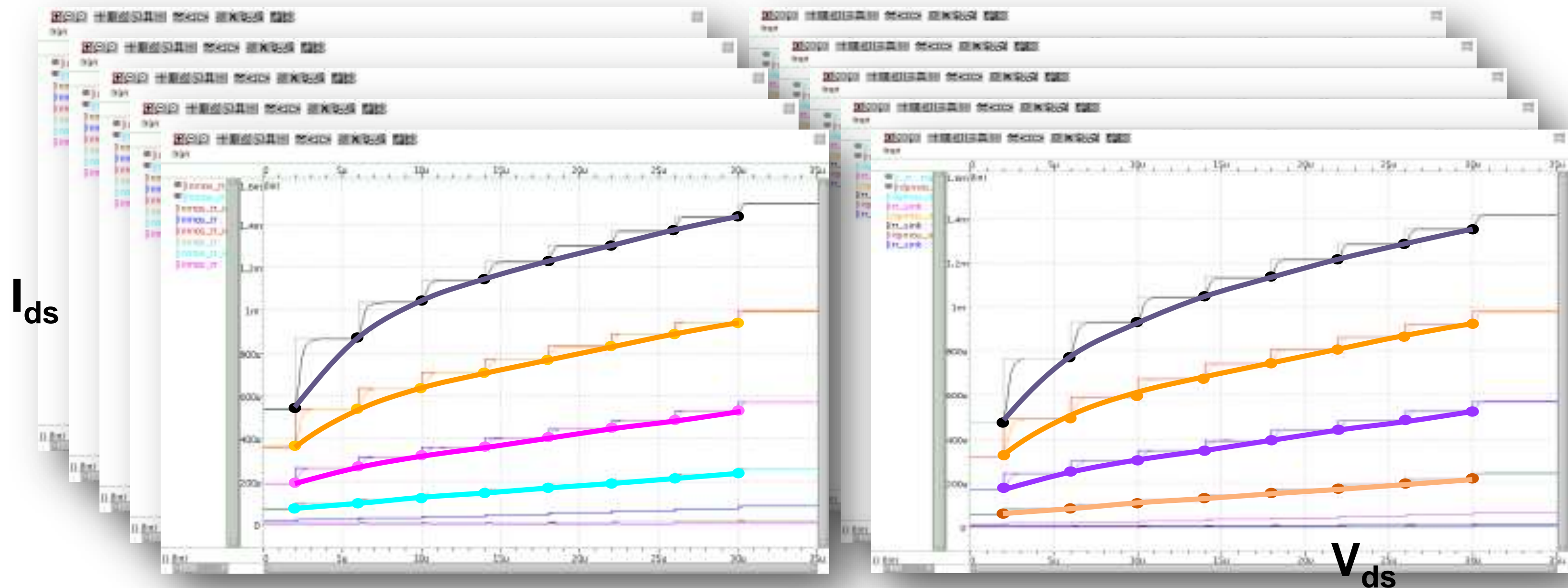
MOS characteristic: Classic IV Sweep

- Test device: NMOS/PMOS: 2.7 µm/0.018 µm
- TR simulation: V_{gs} (0.3V → 0.9V) & V_{ds} (0.1V → 0.9V) sweeping
- I_d range: 180 nA → 1.50 mA



Walk sequentially through all 1,500 devices

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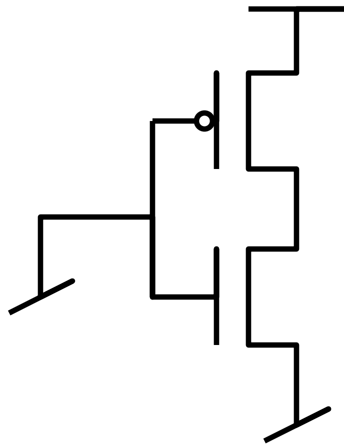
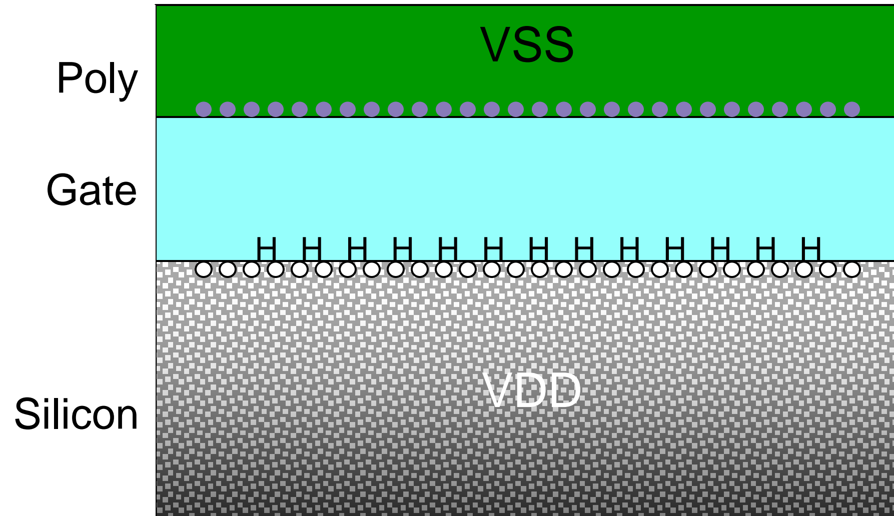
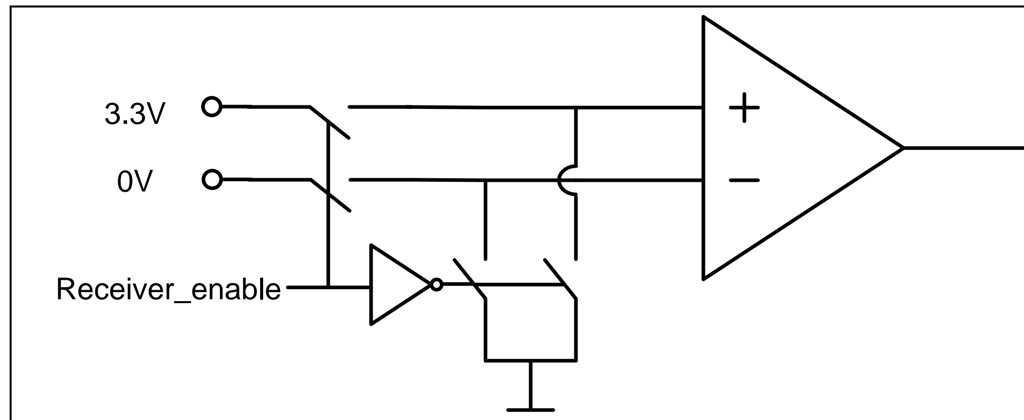
Example of a Simple Circuit Issue

Simple circuit





USB Example of NBTI Issue



Mitigation of the NBTI problem:
Introduction of symmetric stress on both inputs to the differential pair by pulling input to the same voltage during suspend mode.

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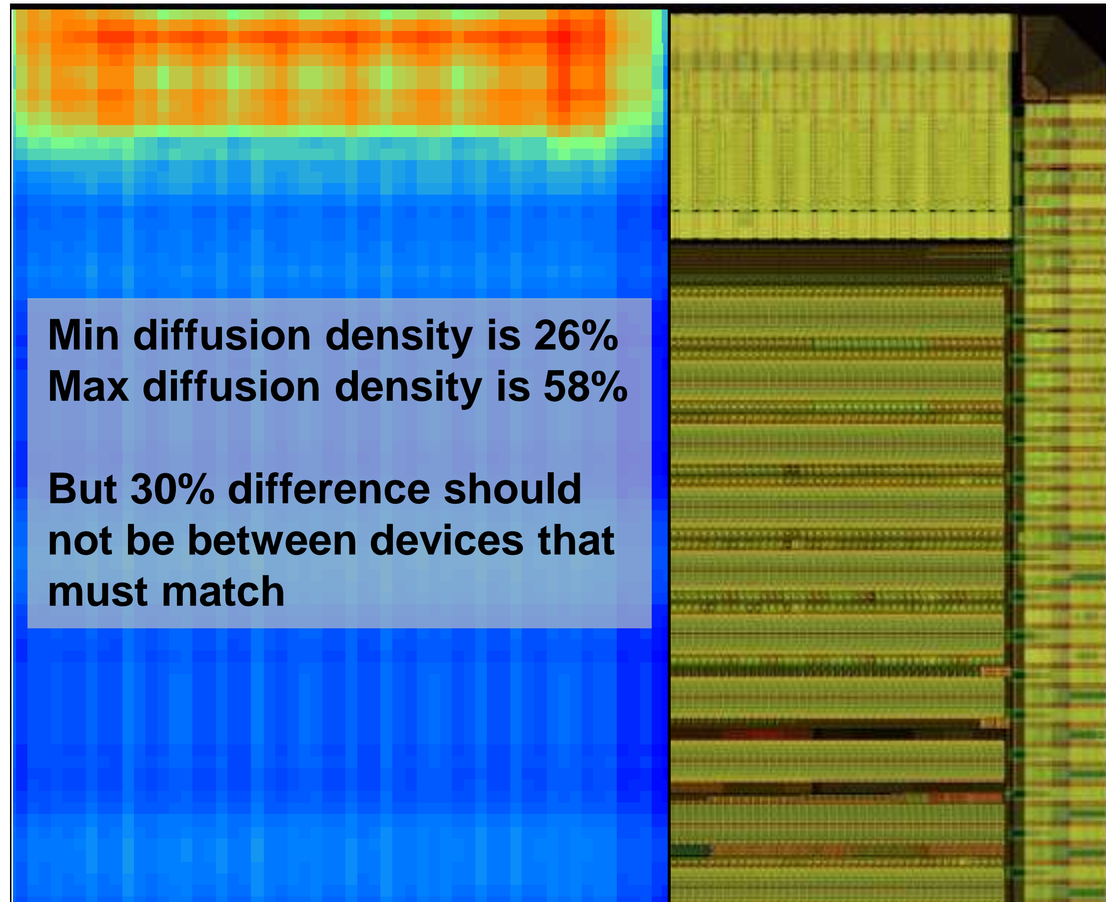
Layer Densities (Filled)
On-Chip ADC example



Know the Issue…
and Design Around It

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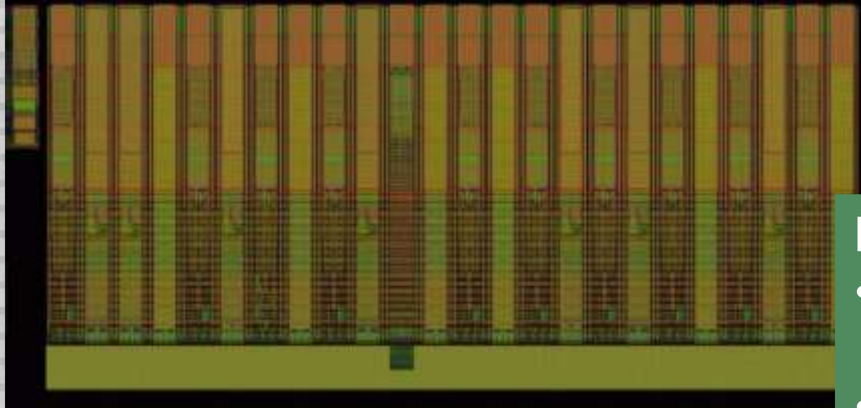
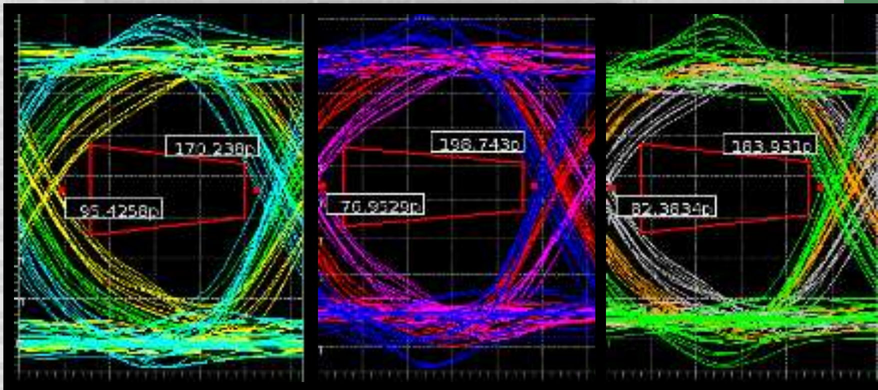
DDR4 I/O –
Overcoming Design Challenges



Implement:

- Novel circuits designed to meet DDR4 as well as legacy DDR3 (wide IO range)
- Pre-emphasis – to help with SI-based losses

  Improved Rx to deal with closed eyes



Feasibility Results

Showing pre-emphasis performance for DDR4 needs above 3.2 Gbps rates

Key Points

- **Deeper link between layout & performance** in 20-nm required (compared to previous nodes)
- **Double patterning** and its effect on circuit density under different metal stack conditions must be considered
- **Quantization of device sizes and restricted design rules (RDR)** mean no 28-nm re-use, 20-nm is a grounds-up development
- **PPA, schedule and early PDK** necessitates an advanced silicon design methodology with close foundry co-operation

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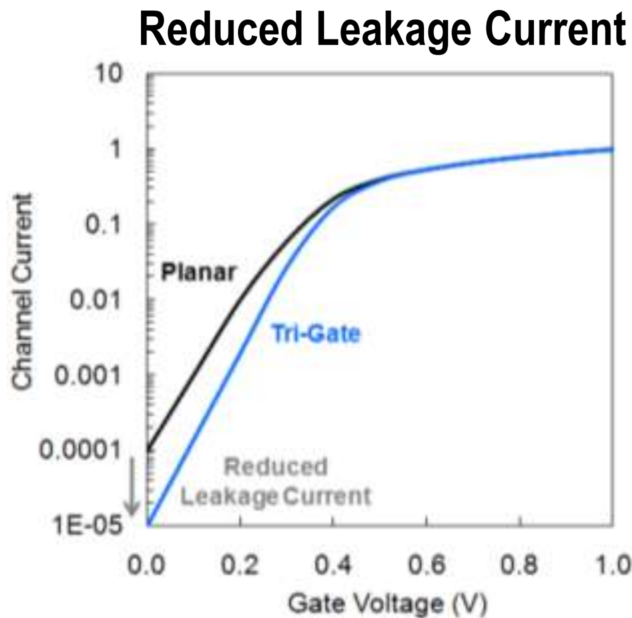
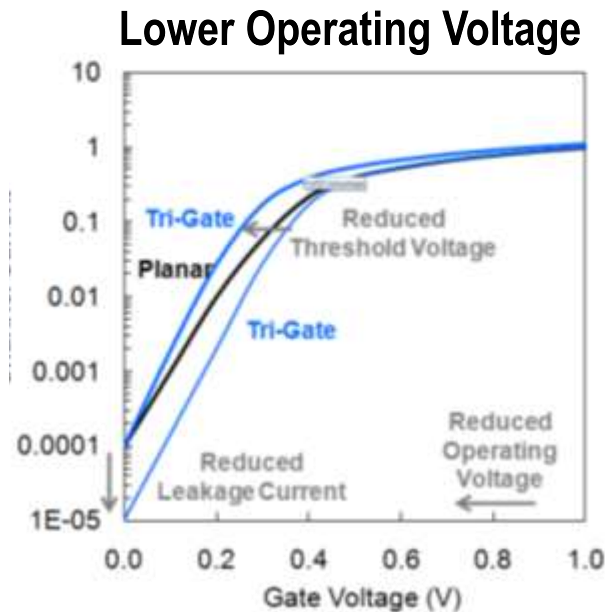
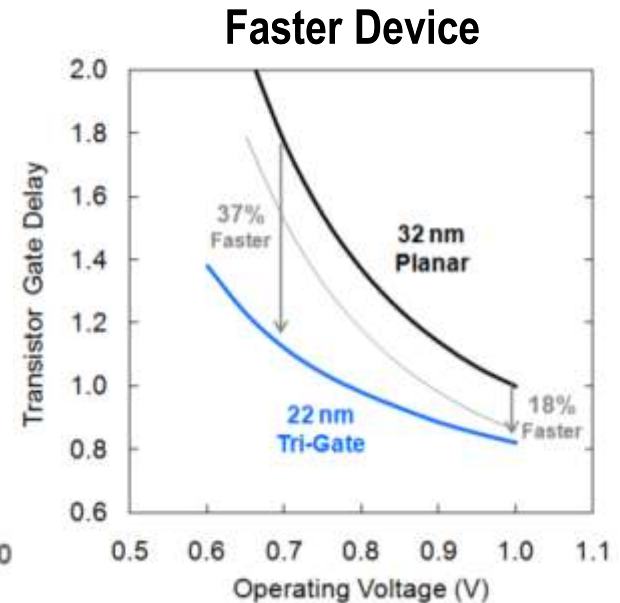
FinFET Advantage







Source: Mark Bohr, Intel Developer Forum 2011

Example of Intel's FinFET with respect to their 32-nm planar

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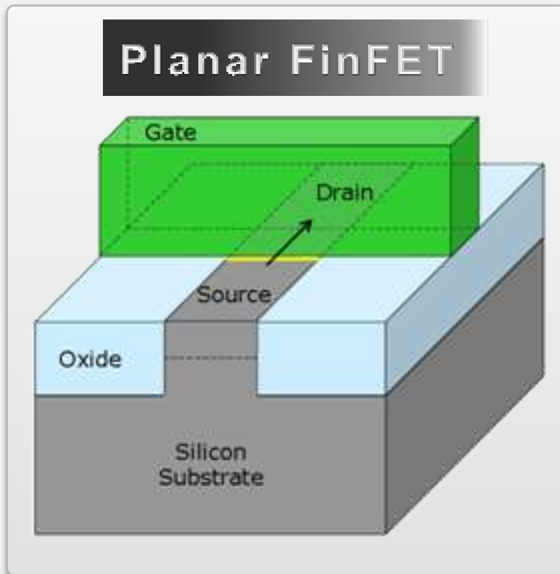
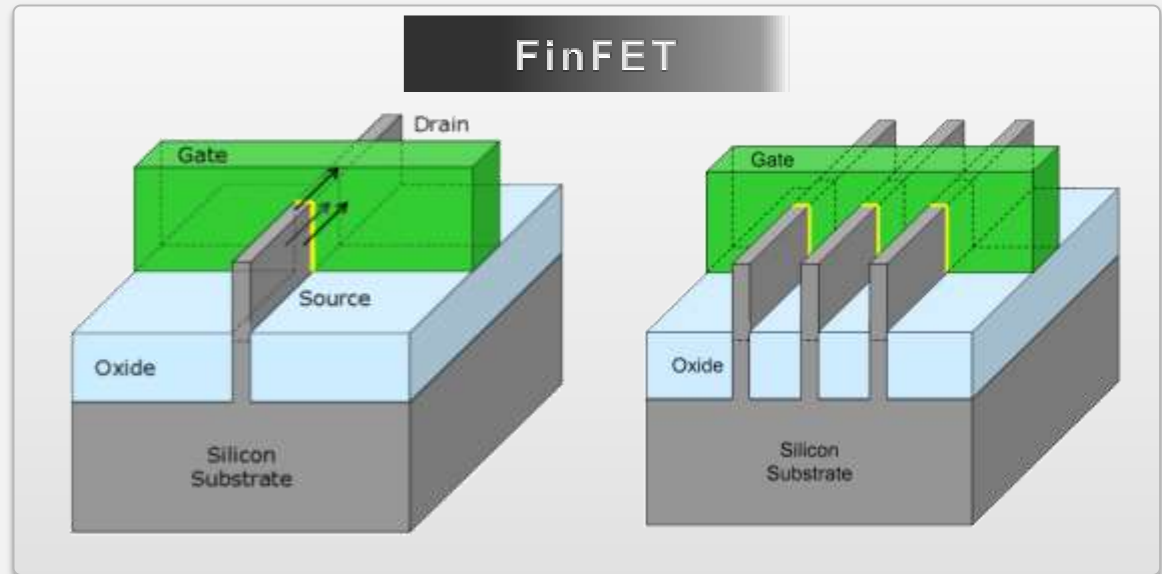
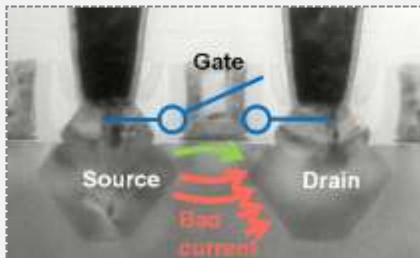
How FinFETs Work







Single gate channel control is limited at 20-nm and below

“**Multiple” gate** surrounds a thin channel and can “fully deplete” it of carriers. This results in much better electrical characteristics.

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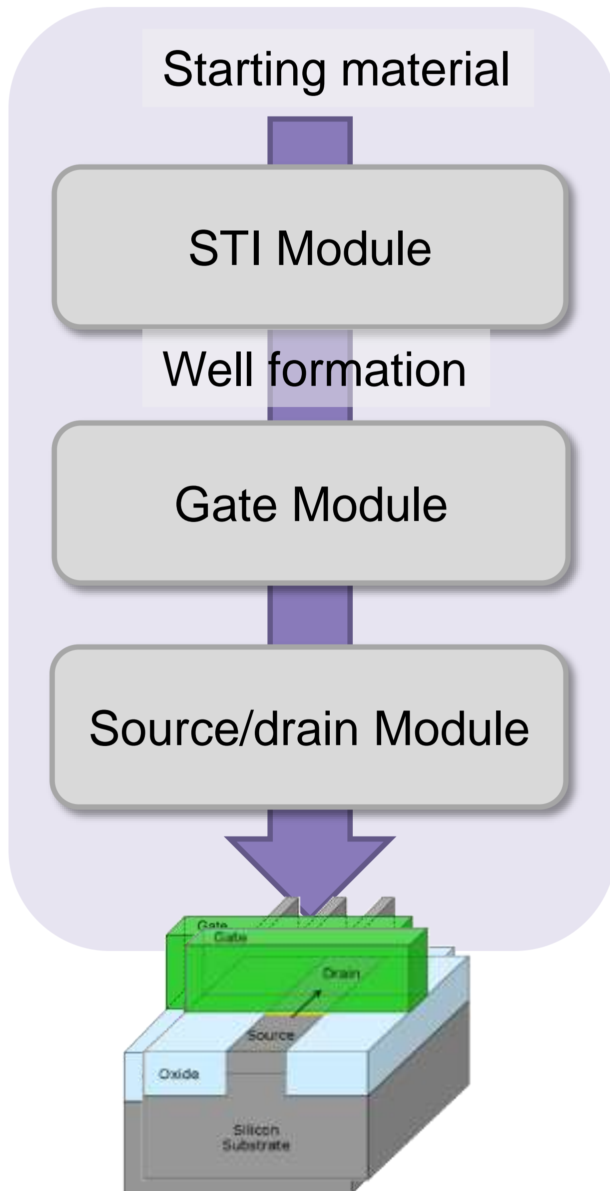
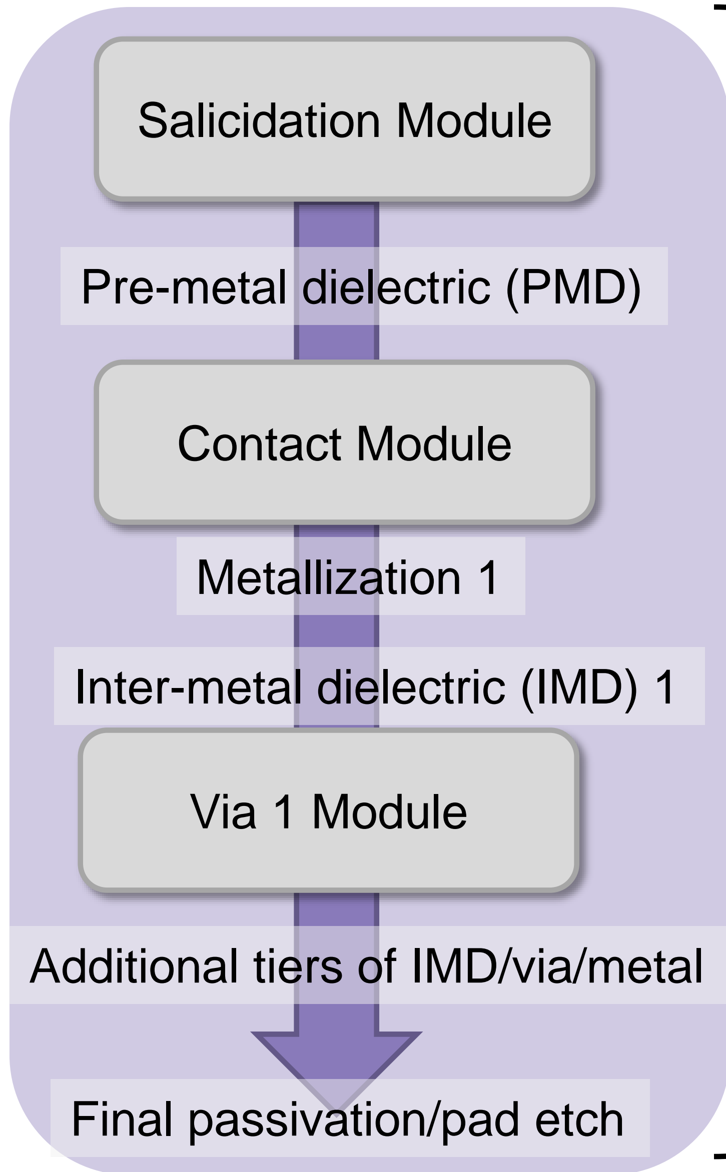
Remember this comment?

“By being modular, vendors have the option to plug in the FinFET into an existing planar BEOL flow.”

FEOL



BEOL



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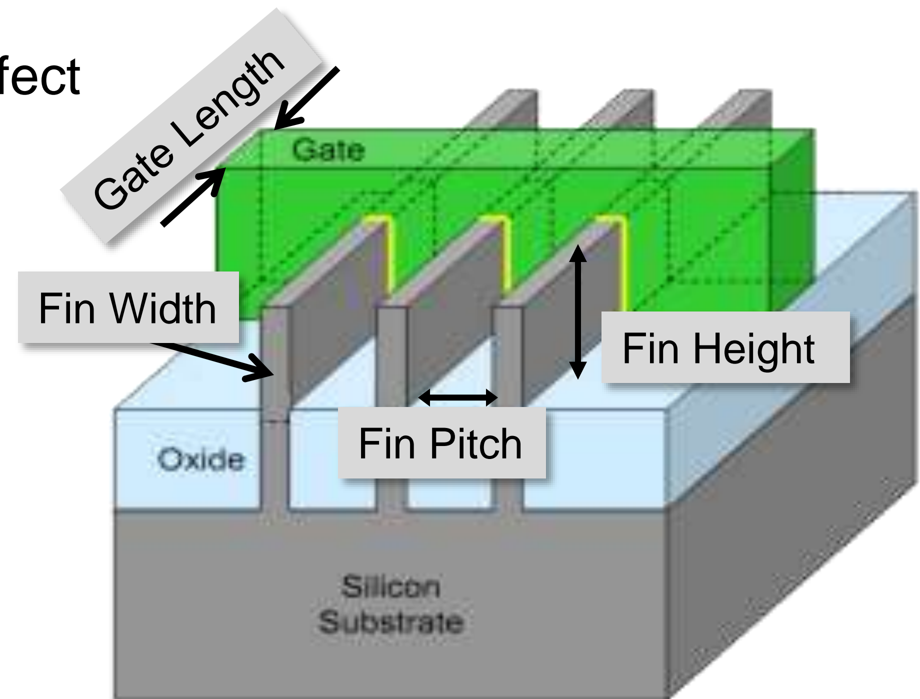
FinFET Technology Parameters

- Fin Width
  - Determines short channel effect (SCE)
- Fin Height
  - Limited by etch technology
  - Tradeoff: layout efficiency *vs.* design flexibility
- Fin Pitch
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance *vs.* layout efficiency



These parameters are fixed by the process,
The only parameters a designer can change: #Fin, #gates

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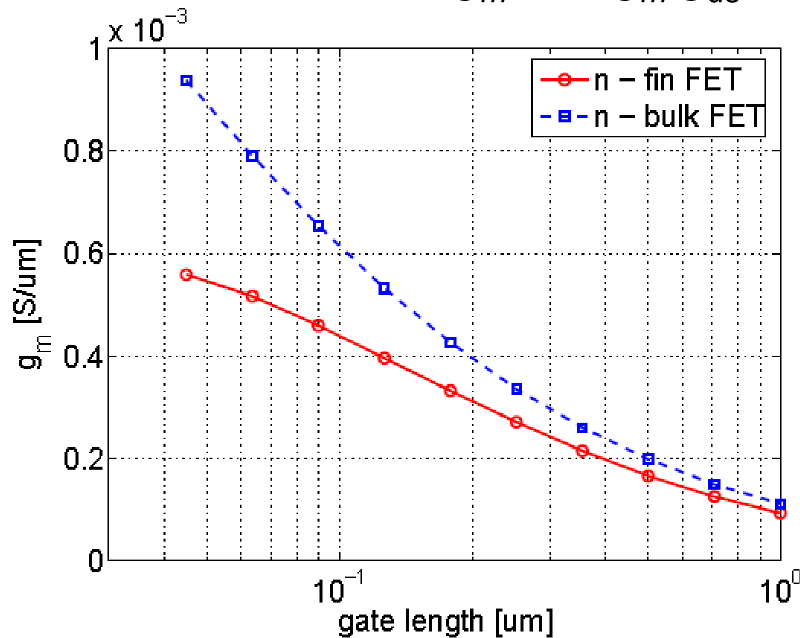
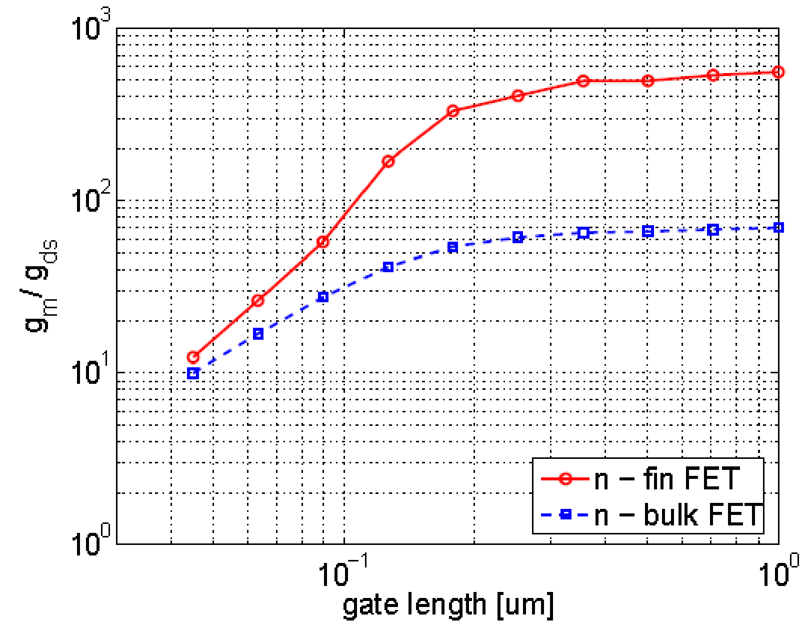
Planar Versus FinFET Comparison

g_m and g_m/g_{ds} of bulk and FinFET





FinFET's provide:

- Improved sub-threshold and short channel behaviour
- Enhanced intrinsic gain gm/gds
- Better matching behaviour
- Metal gates eliminate poly depletion effects
- Lower gm, lower Ft
- Lower output conductance

Source: M. Fulde et al.: Analog circuits using FinFETs (2007)

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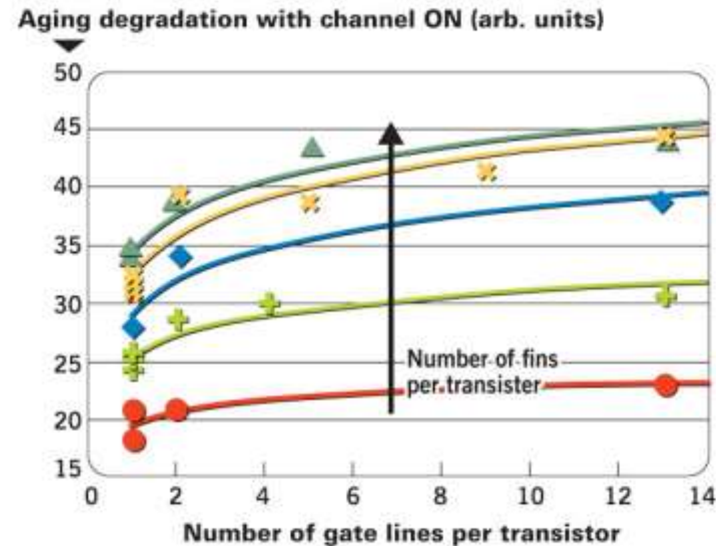
Matching, Self Heating

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}}$$



- FinFET's expected to show good matching behaviour
- Area of current sources in DAC's will improve
  (same matching for a lower area)
- Self-heating shows negligible impact

Source: M. Fulde et al.: Analog circuits using FinFETs (2007), Giuseppe Larosa, IRPS Technical Program 2013 Chair

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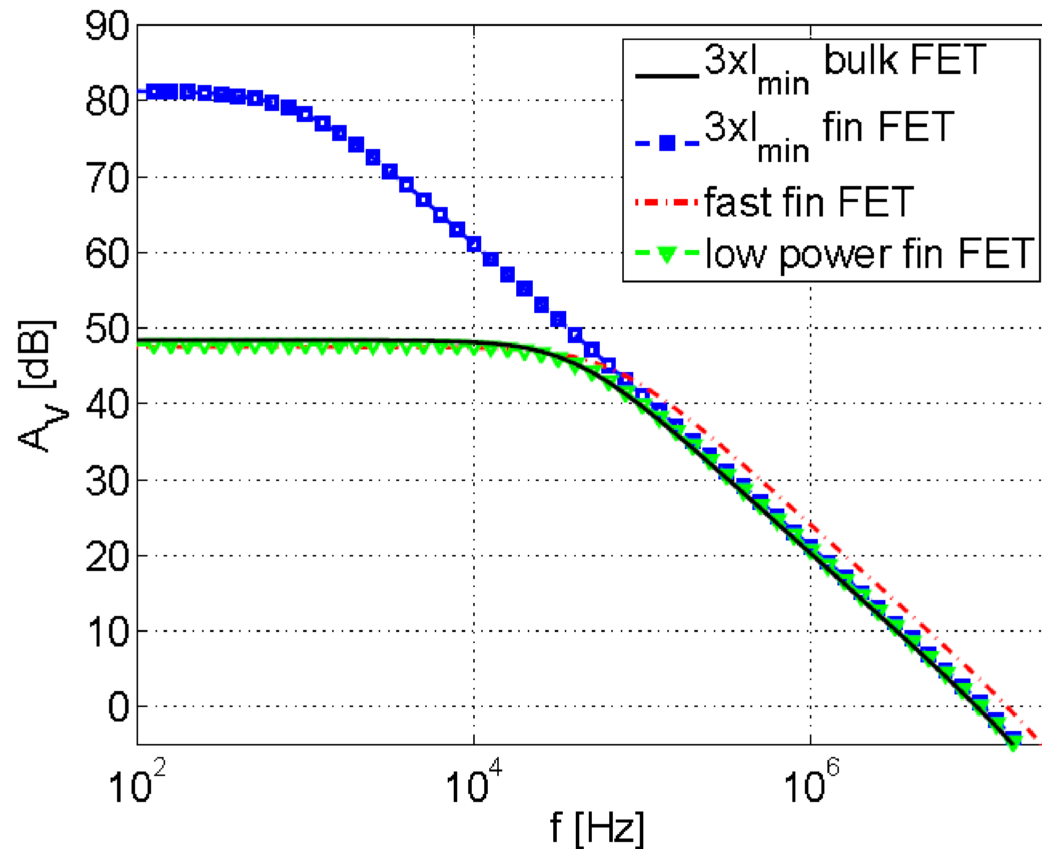
Impact Of Higher Intrinsic Gain

Bode plot of planar and FinFET implementations



Benefits of the improved intrinsic gain two stage Miller compensated OTA

Source: M. Fulde et al.: Analog circuits using FinFETs (2007)

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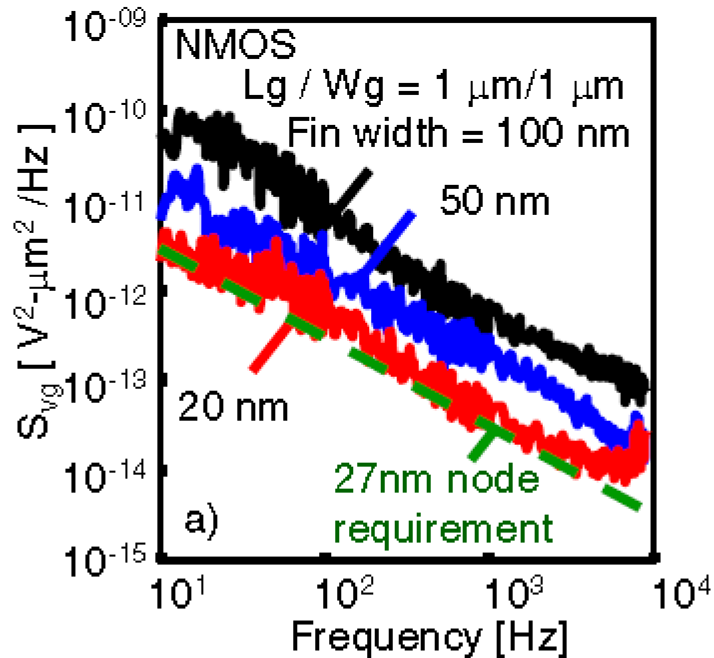
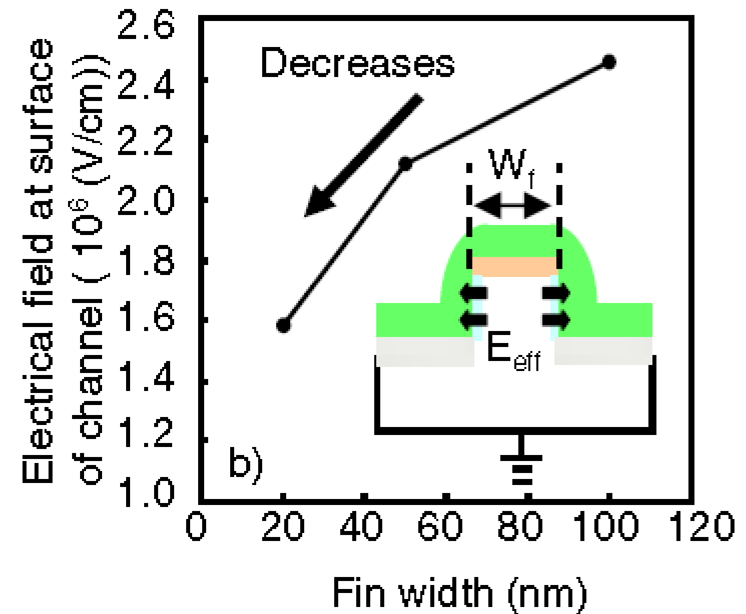
Addressing Flicker Noise

Flicker noise of FinFET decreases with scaling of fin width





Source: "The Optimum device parameters for high RF and analog/MS performance in planar MOSFET and FinFET" Ohguro et. al Y 2012 Symposium on VLSI Technology Digest of Technical Papers

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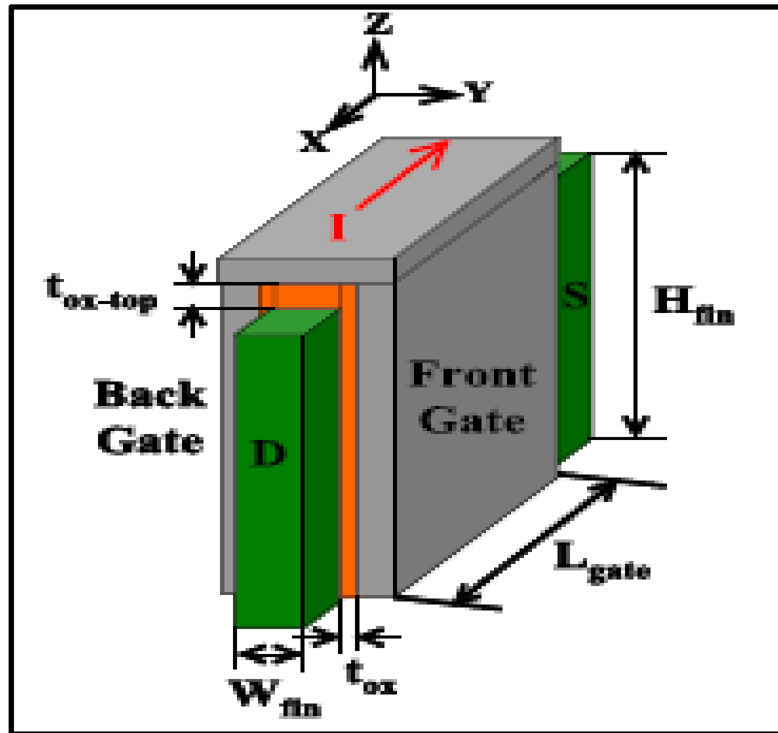
Higher Gate Capacitance



- FinFET has around 2x gate capacitance for the same device size
- Increased power:

  I = (2*Cg + Cwire)*V*F
- Higher On current
- Optimal device sizing is very critical to harness the power reduction

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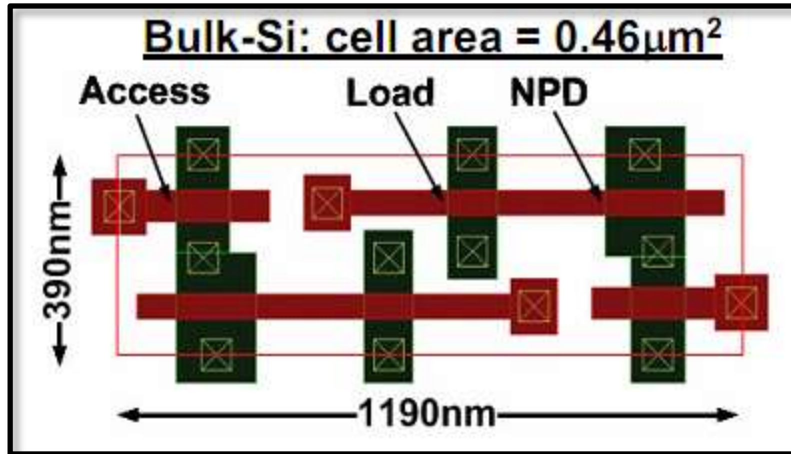
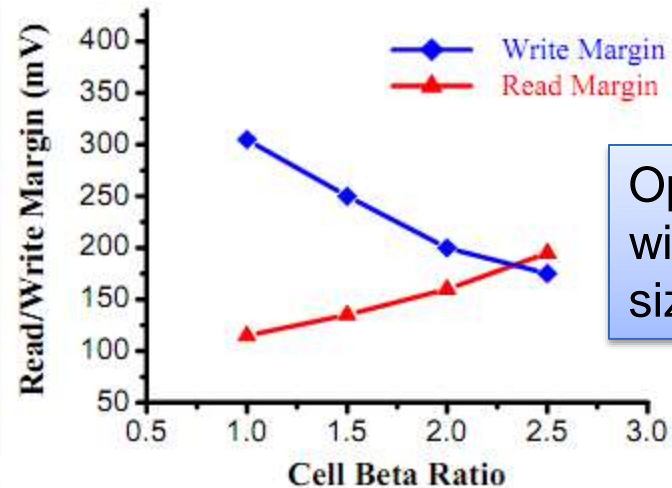
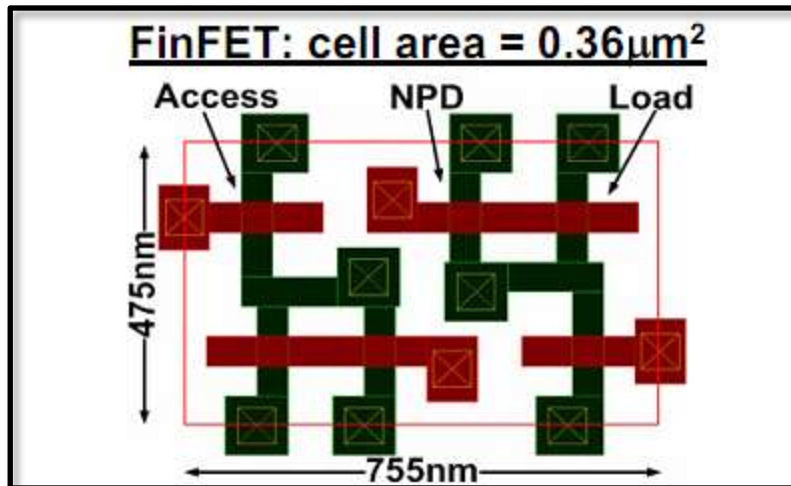
Width Quantization Impact on SRAM

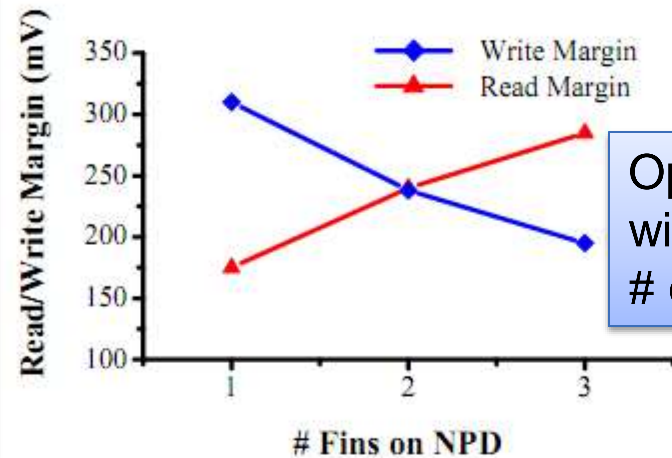
Bulk Si vs. FinFET





Optimization with continuous sizing





Optimization with discrete # of fins

(Prof. Tsu-Jae King Liu, UC Berkeley)

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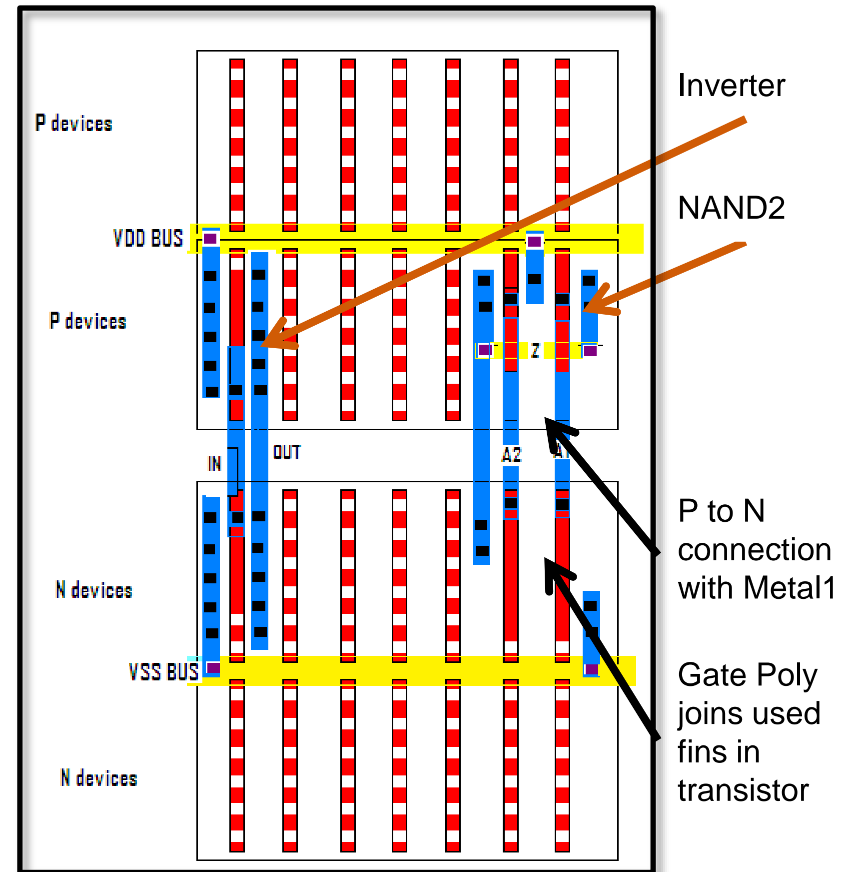
FinFET Standard Cells

- **DPT compliant std. cell layout**
  - Early testing through TCAD modeling & simulation
  - Layout faster
    (built-in features in CD, ICV)
  - Concurrent development process, std. cells
- **Concurrent optimization with P & R**
  - Strict color-compatibility constraints improve placement optimization
  - Optimize cell routability and router enhancements in the context of DPT



FinFET cell architecture from patent application related to standard cells

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Design Challenges, Impact, Solutions

Meet PPA, deep sub-micron technology requirements, layout dependent effects, early version of PDK

1. **Process design rules for manufacturability**
   - Impact: area, development time
   - Solution: earlier SoC floor-planning, new architectures
2. **System specs have not changed** to reflect lower I/O voltages
   - Impact: reliability
   - Solution: new architectures to handle "high voltage", aging sims.
3. **Different core devices** with lower g_m & g_d, higher gate leakage
   - Impact: analog design
   - Solution: new architectures
4. **Meet scaling trend**, SoC integrators expect analog/mixed-signal IP to scale
   - Impact and solution: new architectures needed

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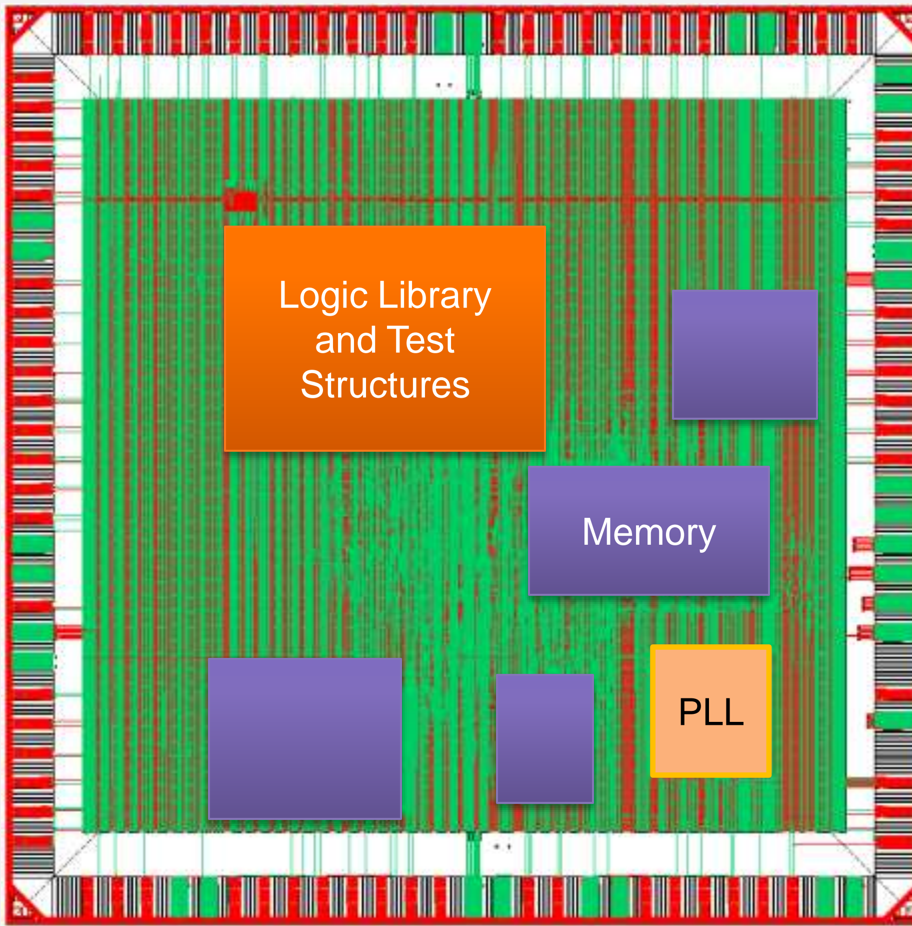
Remember what I said about advanced silicon design methodology?

Advanced Silicon Design Methodology FinFET



- Early memory IP qualification vehicle
- Characterization structures:
  - PLL
  - SRAMs
  - Test Structures
  - Logic library
- Enables process correlation to simulation models

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Technology Assessment Chip
Key Points

- **Very early PDK** used for technology assessment chip
- **PDK variations** methodology had to adapt to known and unknown changes
- **Highly experienced engineers required** (analog, mixed-signal, layout, process, CAD) that could handle the uncertainty
- **CAD flow verification (fill, DRC)** significantly helped in meeting the next set of 14-nm FinFET analog/mixed IP tape-outs

But…for FiNFET's you need more…
an infrastructure (tools, extraction, device simulation)

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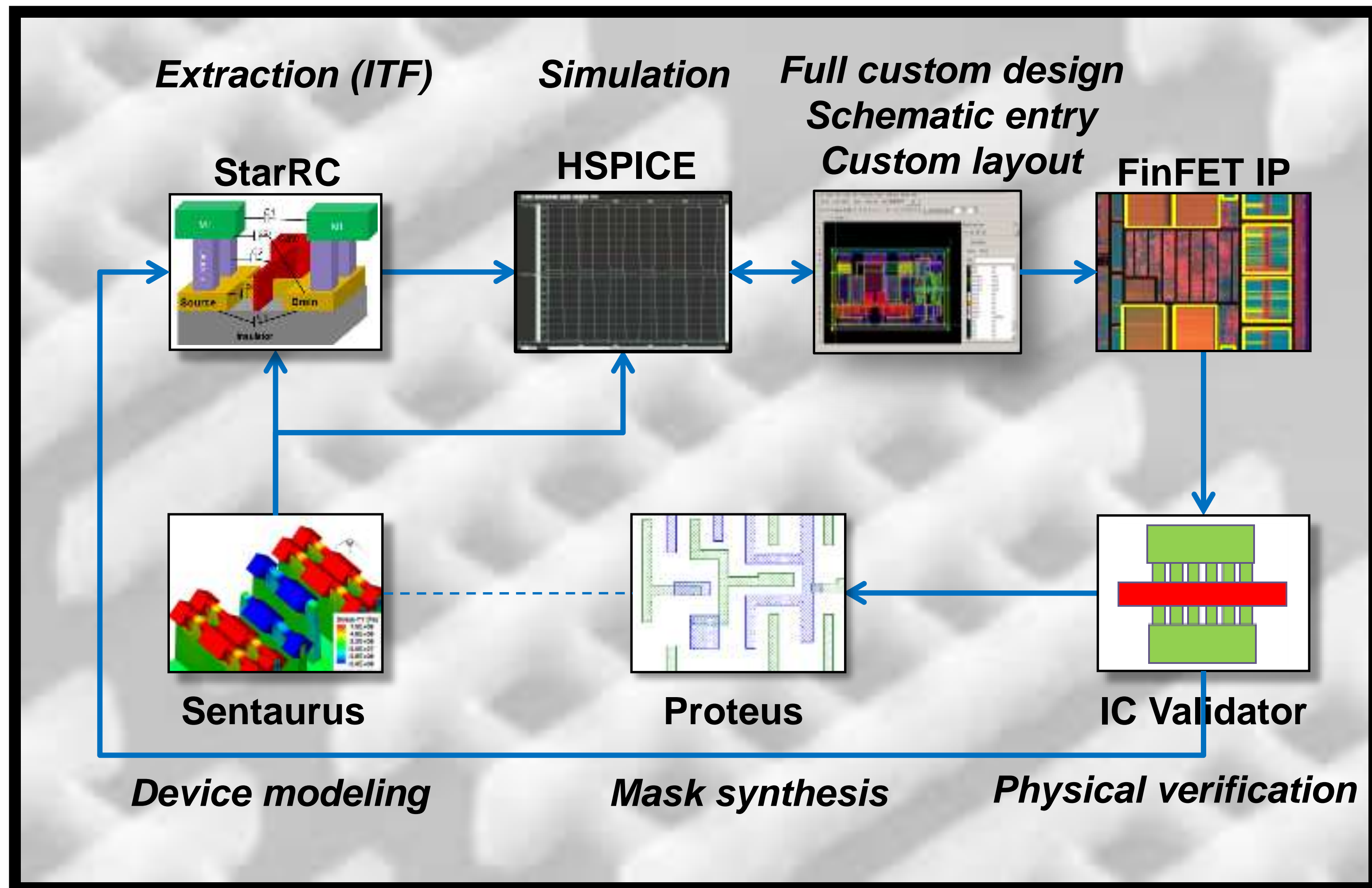
It Takes A Village…



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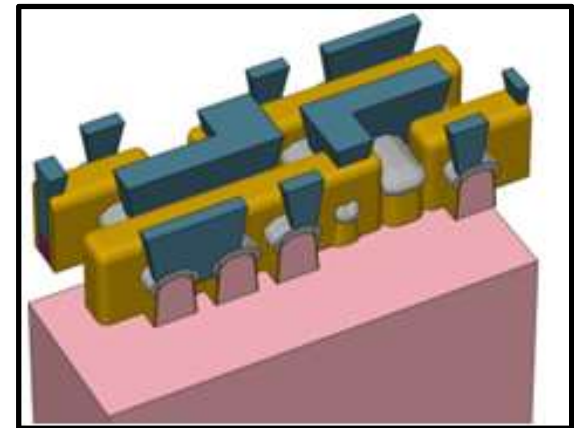
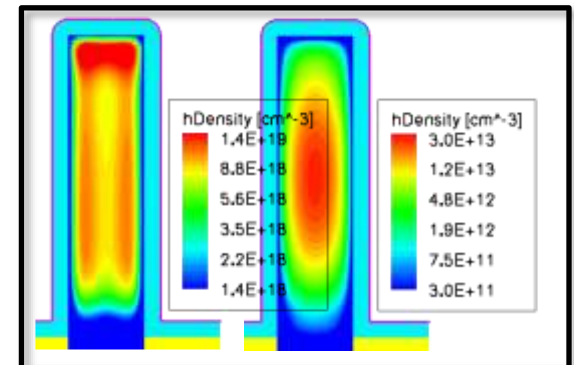
Sentaurus TCAD

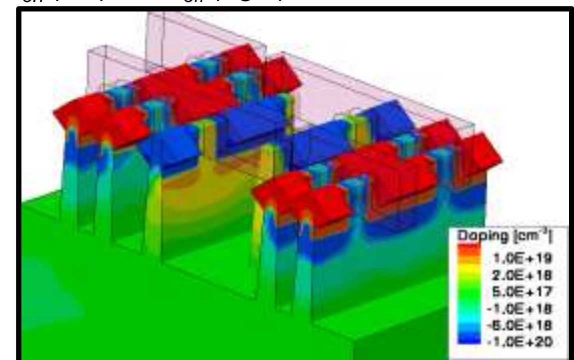
- **Sentaurus Process**
  - Plasma model enables optimization of Fin doping
- **Sentaurus Device**
  - Simulate the current along sidewalls and top of the fins, for on-state and off-state
  - Analyse random process variation < 14-nm
  - Characterization of proximity effects
- **Used at foundries and IDMs**
  - Effect of Fin geometry on scaling, electrostatics
  - Optimization of processing flow, doping, stress



FinFET SRAM cell showing 3D structure



I_{on} (left) and I_{off} (right) in Fin cross section



Doping proximity effects in SRAM cell

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FinFET Impact On The Designer

"Being modular, vendors have the option to plug in the FinFET into an existing planar BEOL flow."

Same metal → no impact to the mixed-signal designer

The impact of FinFETs is largest below metal 1: standard cells, memory compilers and full custom design such as analog/mixed-signal, are impacted.

Double patterning and restricted design rules, while associated with FinFETs, are not unique to them; they are necessary for planar technologies → <u>this 20-nm planar experience can be applied to standard cells, memory compilers and full custom design</u>

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Evolution Of Electronic Devices

- Triode vacuum tube
- BJT transistor
- MOSFET transistor

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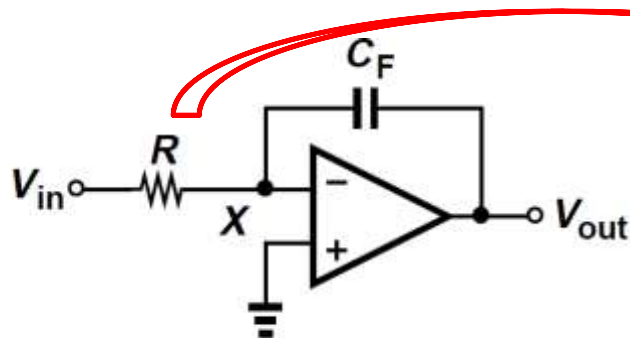
Circuit Invention Triggered By New Devices

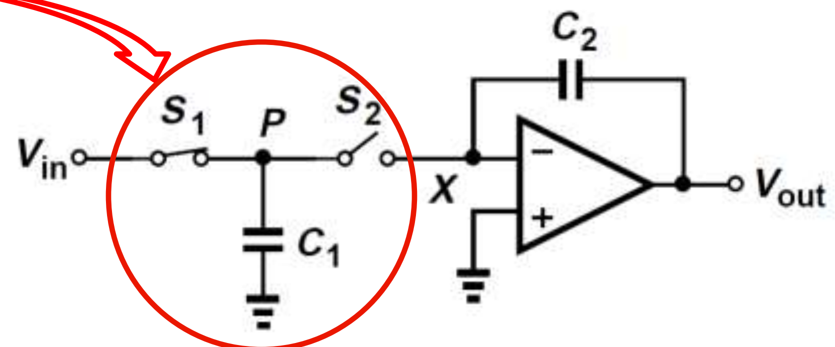
The continuous time integrator

- Pole freq. is a function of R and C_F
  - Precision of R is very limited
- Pole freq. is inversely proportional to R
  - Impractical to have large R's in IC
  - R requires trimming for precision

The switched capacitor integrator

- Pole freq. is a function of ratio of C's
  - High accuracy and stability
- Pole freq. is proportional to C_1
  - Small C's are easy to implement
- Only practical in CMOS
  - BJT not good switches, off leakage





- SC architectures enabled by MOSFET devices
- Used in most integrated analog functions: Filters, Data Converters For Communication, Audio, Signal Processing

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Analog/Mixed-Signal Design
In The FiNFET Generation

New architectures will be created to solve the design challenges and take advantage of the characteristics of FinFET:

- Lower leakage
- Higher intrinsic gain
- Higher speed
- Abundance of devices

The micro-electronics innovation cycle
New devices → Challenges → Innovation

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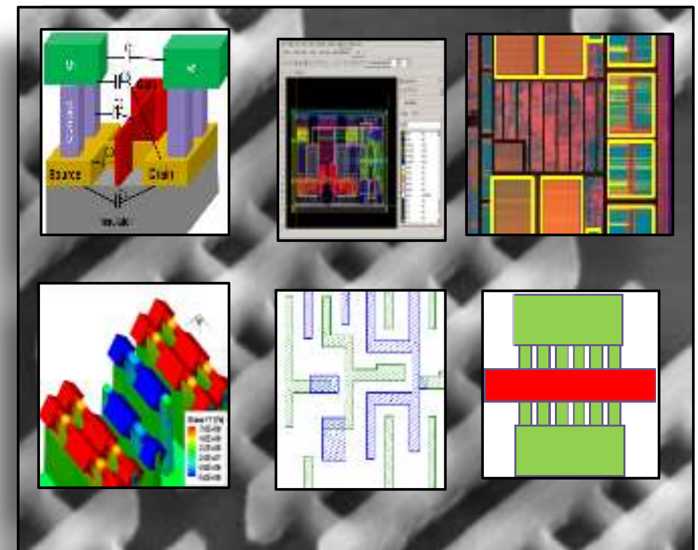
Agenda

20-nm Design Requirements

Advanced Design Methodology

Stepping Stone To FinFET

Summary



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20-nm (Planar) Mixed-Signal IP
A Stepping Stone To FinFET?

Is this true?

Is this the right question?

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Summary

- **Designers care about the same parameters** (g_m, g_d, F_t, F_{max}, matching, noise) in planar or FinFET to get performance while meeting the SoC constraint of power, area
- **20-nm planar provides designer with DPT and RDR experience**, → stepping stone to FinFET
- **Additional stepping stones are related to methodology**
  - **Process qualification vehicles** using early design kits necessary to provide insight into impact on CAD verification and analog performance
  - **New architectural development** planar (28-nm → 20-nm) required new architectures to meet power, performance and area, same applies to FinFET
- **Change to FEOL impacts transistors** changing analog performance, the same BEOL (metal) has no impact
- **Designers will leverage FinFET properties** to invent new circuits

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