



End-to-End Automated Hardware/Software Co-Design for Reconfigurable SoC



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Agenda



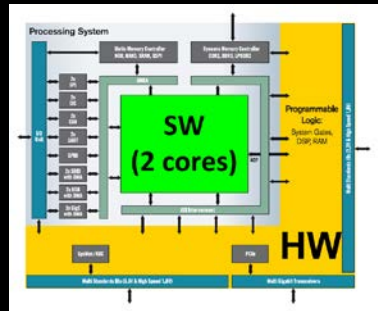
- **Problem**
- **Our solution**
- **Details about the Flow**
- **Case Study**
- **Conclusion**

Problem

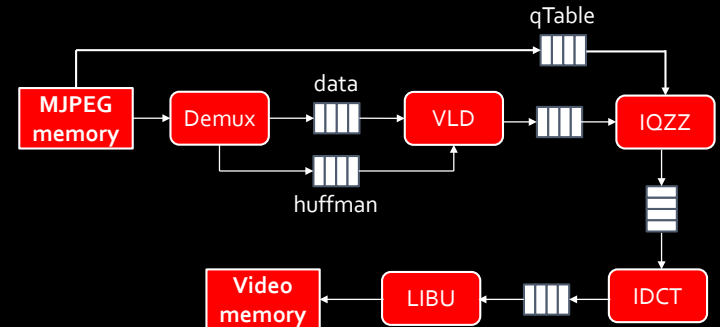
- **FPGA design is dealing with larger, more complex Hardware and Software systems**
- **System Architects must perform rapid decision-making on functions to be realized in HW or SW to meet specific application requirements**
- **HW and SW engineers must refine for optimal HW/SW partitioning to fit system requirements in implementation.**
- **The last two points (namely HW/SW codesign and HW/SW cosynthesis) are not well established in FPGA design flow.**

Problem (cont'd)

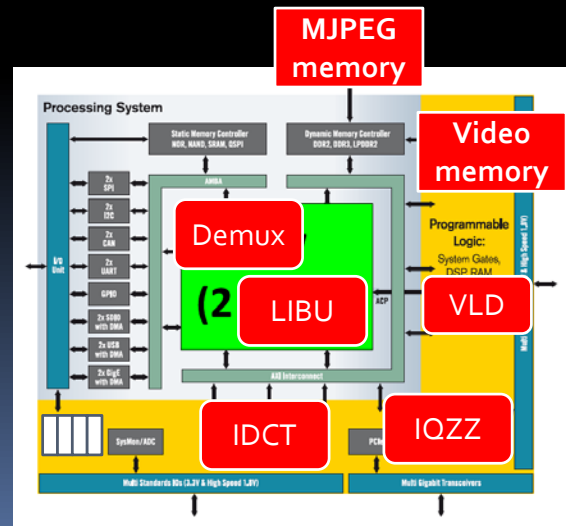
Today's FPGA workflow may take many iterations
And many hours per iteration



Architecture



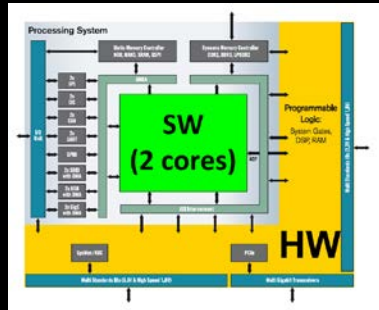
Application



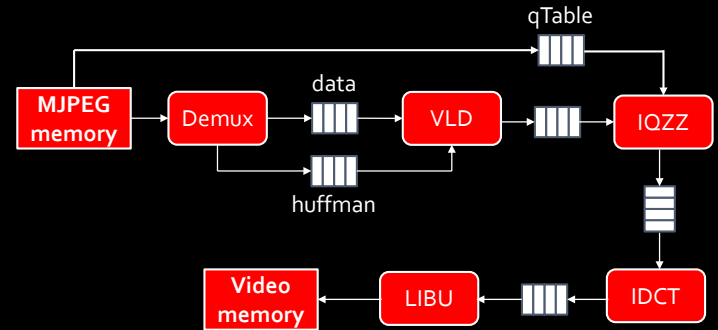
Mapping

Problem (cont'd)

Today's FPGA workflow may take many iterations
And many days per iteration



Architecture



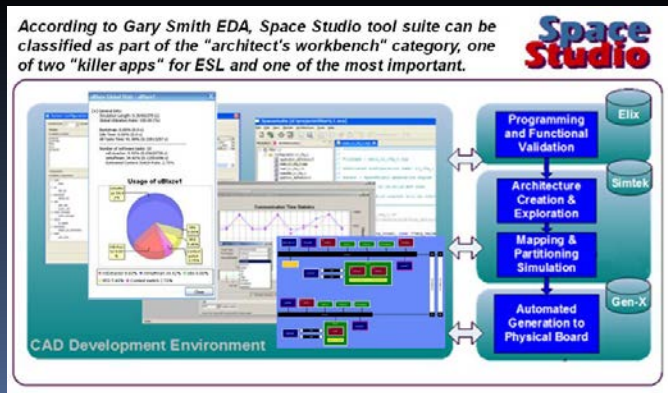
Application (Algorithm)



Partitioning (days)

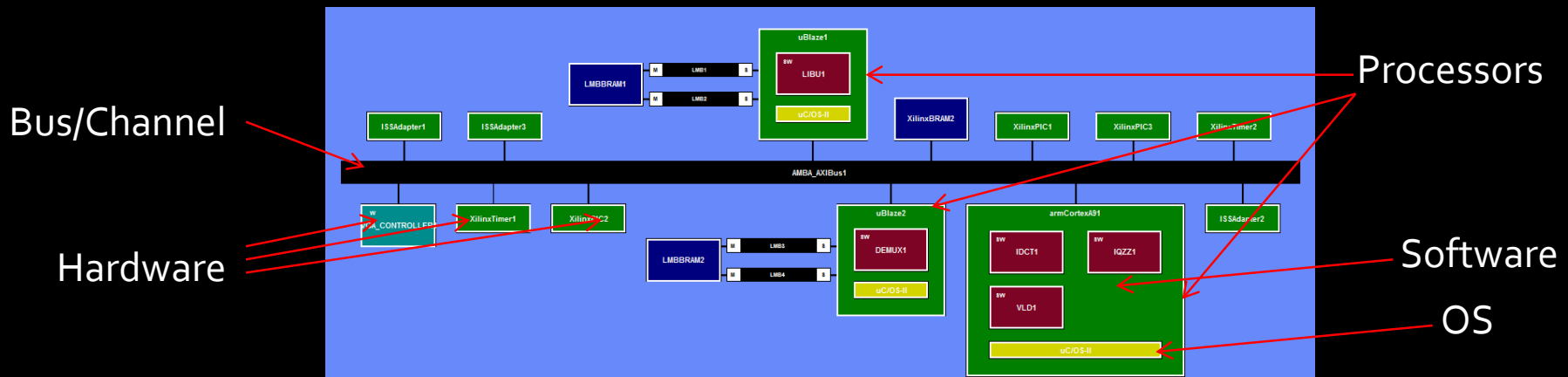
Our Solution

- Rapid decisions at front end of design process
 - Electronic System Level (ESL)
 - Create Large Complex Systems at Higher Level → reduce complexity of details ...
 - Co-design of Software AND Hardware – together (Software content is *increasing*)



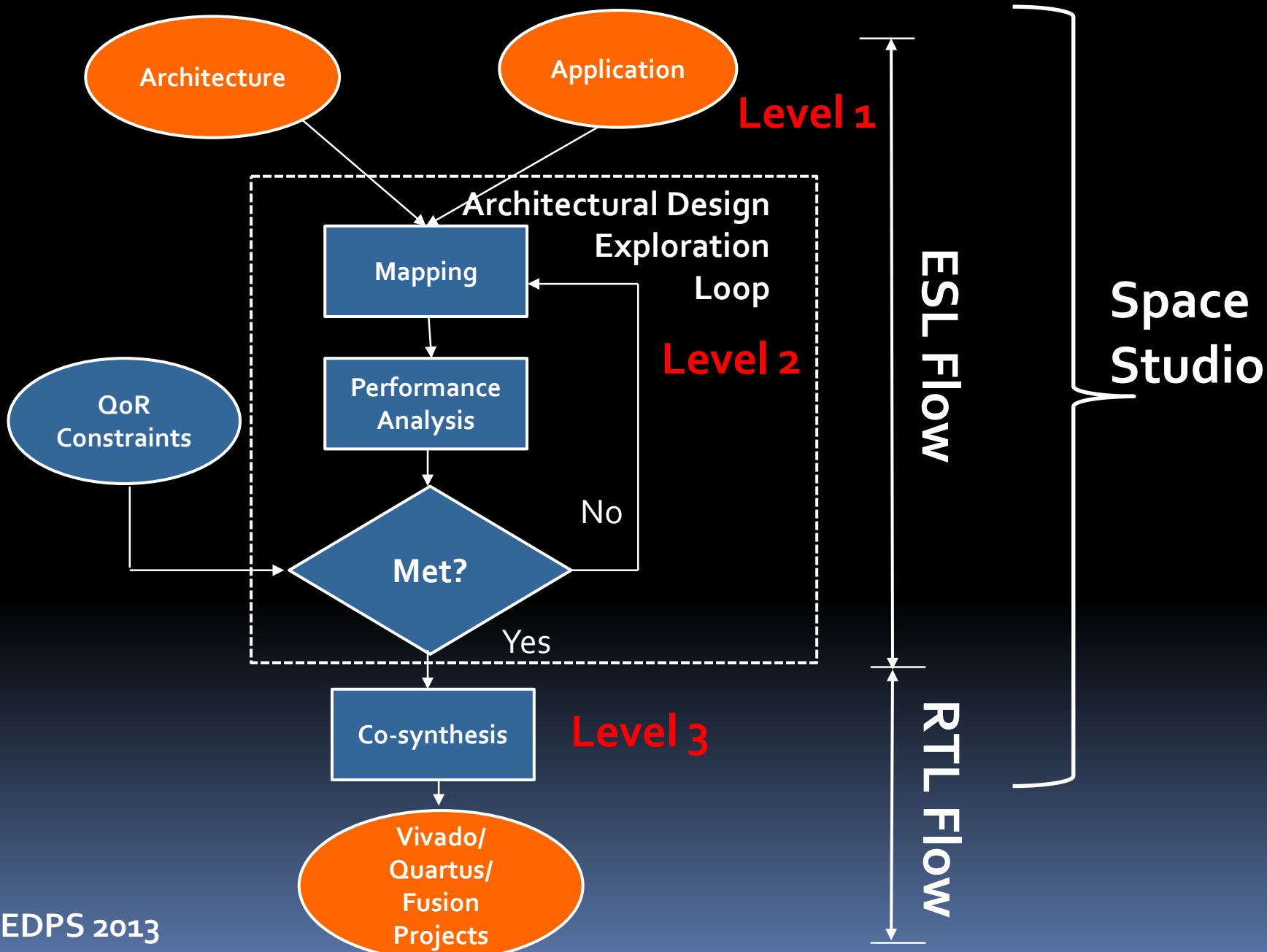
Our Solution (cont'd)

- Level 1 – Algorithm/Functional Specification
- Level 2 – Architectural Design Exploration



- Level 3 – Implementation Manager (IP Mapping, HLS) Programmable right now – ASIC tbd

Our Solution (Cont'd)



1) Application (Algorithm)

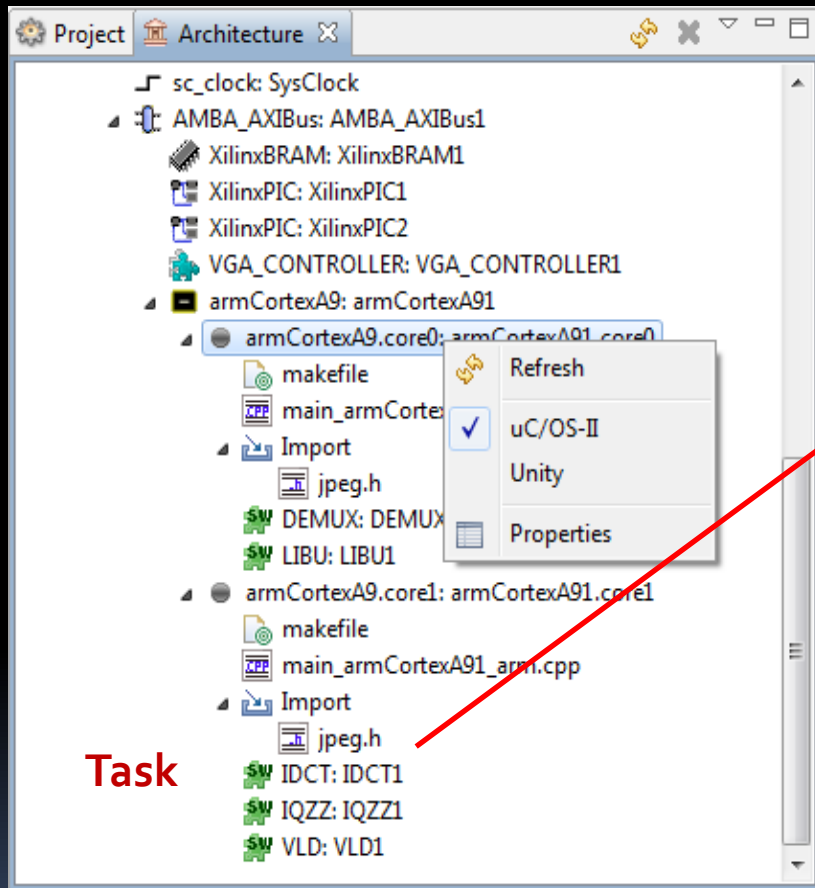
- **Multi-task application specification at a high level of abstraction using C/C++ blocks**
- **Supported communication semantics**
 - **FIFO-based message passing**
 - **Shared memory**
 - **Memory-mapped I/O**

2) Architecture Design (Virtual Platform)

- **Library of TLM-2.0 models for:**
 - **Processors**
 - **OS (BareMetal, uC, Linux, etc.), AMP, SMP**
 - **Busses and interconnects**
 - **Memories**
 - **I/O peripherals**
- **Extensions for third-party or user-defined IPs**
 - **User IP Import**
 - **C/C++ model import w/SystemC + TLM-2.0**
 - **IP-XACT description for parameters and interfaces of the component**

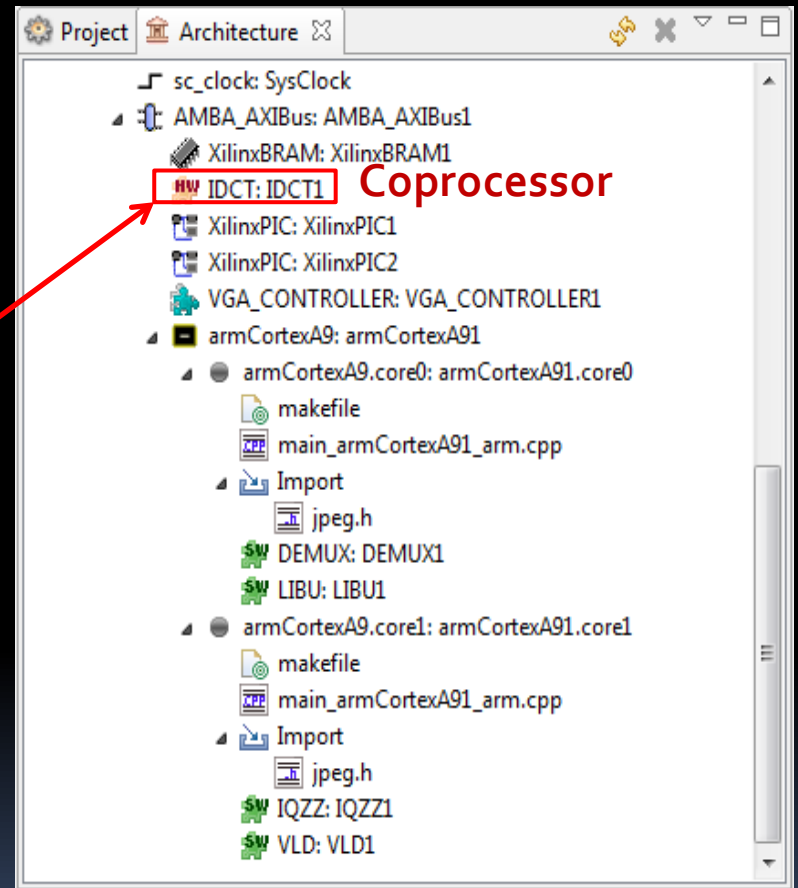
3) Function Mapping and Partitioning

- Drag and Drop Mechanism Supports Design Iteration



Task

SW 2 HW



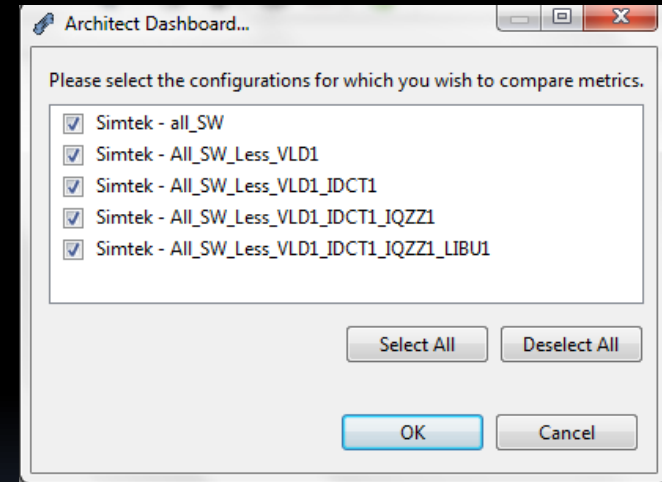
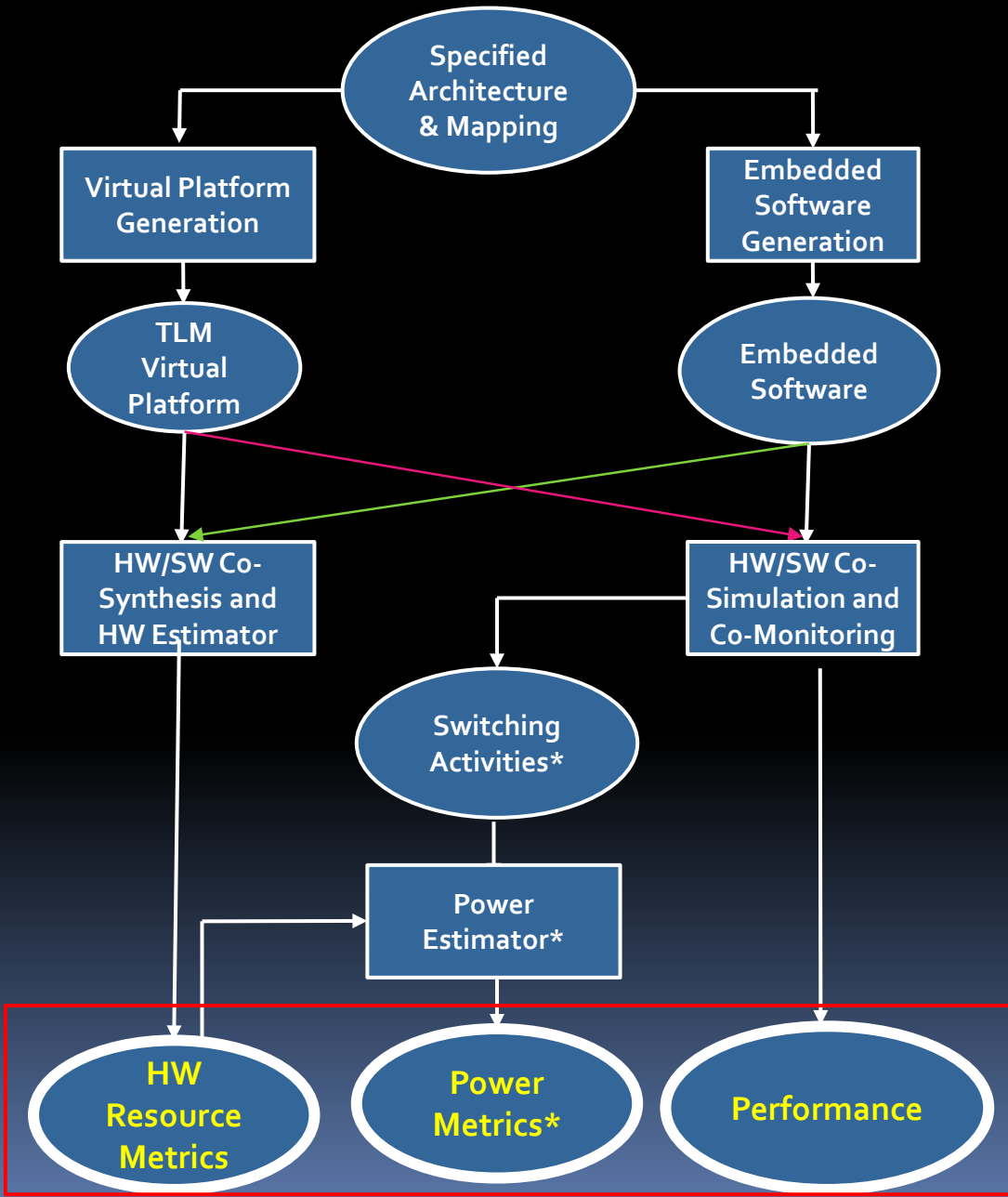
1st Mapping
Configuration 1:
All SW

Drag + Drop

Iteration

2nd Mapping
Configuration 2:
All SW less IDCT

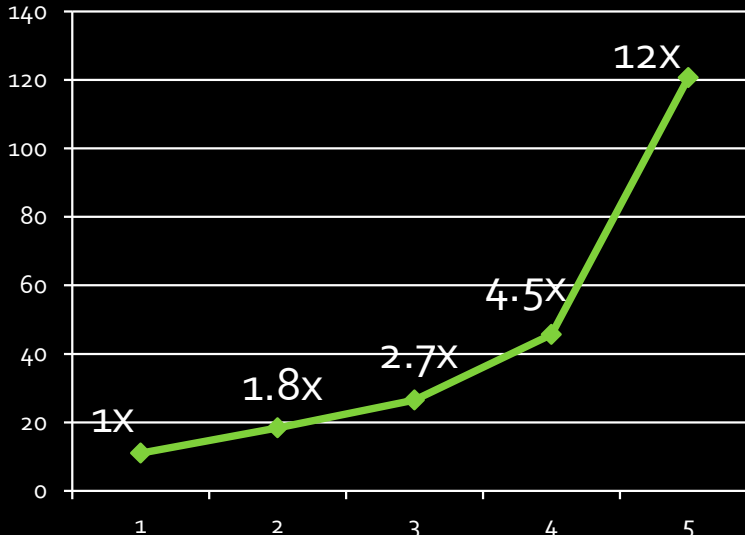
4) Performance Analysis and Evaluation



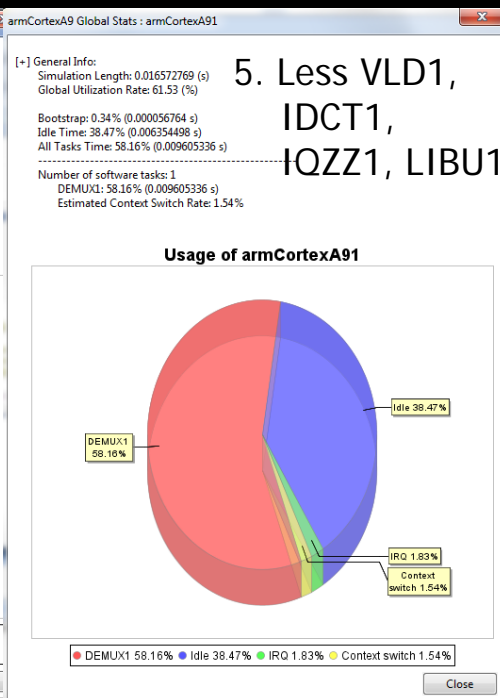
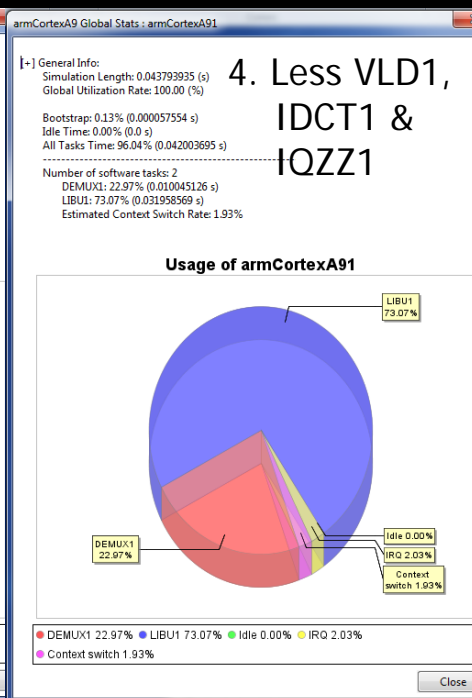
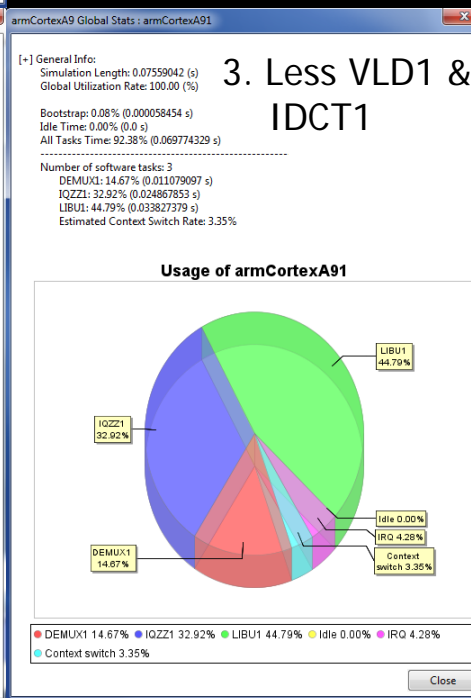
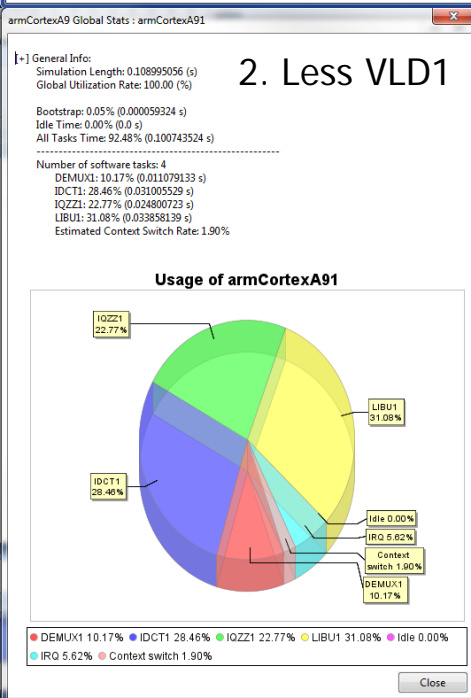
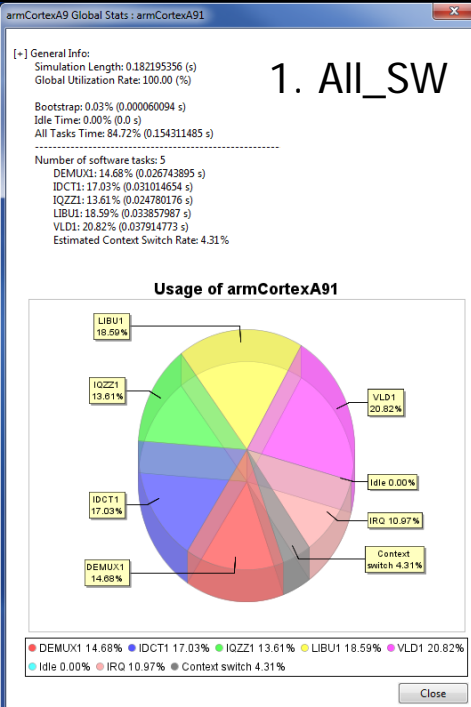
Evaluation can be automated through an Architect Dashboard

Example: Load on a single ARM Cortex-A9 core

Images/sec



HW/SW conf.



Another example: Resource and Power Estimation

FPGA Estimation Results From Simulation ...

Computer Aided Design (CAD) Tools
EDA: Xilinx - EDK 14.1

Board
Board: Zynq_Z-7010
Vendor: Xilinx
Family: zynq
Device: xc7z010
Package: clg400
Speed grade: -1

Platform Resource Usage

bonded IOBs :	<input type="text" value="0.00 %"/>	0.00 %	0 of 100 bonded IOBs
Slice LUTs :	<input type="text" value="52.40 %"/>	52.40 %	9,223 of 17,600 Slice LUTs
Slice Registers :	<input type="text" value="17.13 %"/>	17.13 %	6,029 of 35,200 Slice Registers
BUFG/BUFGCTRLs :	<input type="text" value="18.75 %"/>	18.75 %	6 of 32 BUFG/BUFGCTRLs
Block RAM/FIFO :	<input type="text" value="18.33 %"/>	18.33 %	11 of 60 Block RAM/FIFO
DSP48E1s :	<input type="text" value="3.75 %"/>	3.75 %	3 of 80 DSP48E1s

< Back Next > Finish Cancel

Device	
Family	Zynq-7000
Device	XC7Z045
Package	FBG676
Speed Grade	-2
Temp Grade	Industrial
Process	Typical
Voltage ID Used	
Characterization	Advance_v0.7_2012-04-23

Environment	
Junction Temperature	<input type="checkbox"/> User Override
Ambient Temp	25.0 °C
Effective ΘJA	<input type="checkbox"/> User Override
Airflow	250 LFM
Heat Sink	Medium Profile
ΘSA	3.4 °C/W
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
ΘJB	
Board Temperature	

FPGA Implementation	
Usage/Optimization	Power Optimization

Resource	Power (W)	(%)
<i>(Jump to sheet)</i>		
Core Dynamic	CLOCK	0.016 1
	LOGIC	0.034 3
	BRAM	0.010 1
	DSP	0.001 0
	PLL	0.000 0
	MMCM	0.000 0
	PHASER	0.000 0
I/O	PCIE	0.000 0
	IO	0.000 0
Transceiver	GTX	0.000 0
PS Dynamic Static	PS	0.829 77
		0.048 4
FPGA Static		0.134 12

Source	Voltage	Total (A)
VCCINT	1.000	0.139
VCCBRAM	1.000	0.003
VCCALUX_IO		
VCCALUX	1.800	0.030
VCC0 3.3V	3.300	
VCC0 2.5V	2.500	
VCC0 1.8V	1.800	
VCC0 1.5V	1.500	
VCC0 1.35V	1.350	
VCC0 1.2V	1.200	
MGTVCCALUX	1.800	
MGTAVCC	1.000	
MGTAVTT	1.200	
VCCPINT	1.000	0.585
VCCALUX	1.800	0.078
VCC0_DDR	1.500	0.102

Summary

Junction Temperature	27.0 °C
Total On-Chip Power	1.072 W
Thermal Margin	73.0 °C 37.2W
Effective ΘJA	1.9 °C/W

Power supplied to off-chip devices: 0.000W

- 0% Transceiver: 0.000W
- 0% IO: 0.000W
- 83% PS+FPGA Dyn.: 0.890W
- 17% Device Static: 0.182W

Messages

Comments

[XILINX Power Advantage \(check for updates\)](#) [File Support Request \(WebCase\)](#) [XPower Estimator User Guide](#)
[Copyright © 1994-2012 Xilinx, Inc. All Rights Reserved](#) [Whitepaper - 7 Steps for Worst Case Power Estimation](#)

Legend User Entry Calculated Value Summary Value User Override Warning Error

Power estimates obtained through Xilinx's XPower Estimator

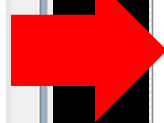
5) Co-synthesis (From ESL 2 RTL)

- **Export RTL implementation of Architecture**
 - **RTL platform IP's, Glue Logic**
 - **Embedded Firmware and Software**
 - **Project for downstream tools (e.g., ISE, Vivado, Quartus, Fusion, etc.)**
 - **Support for High Level Synthesis flows for HW accelerators**

5) Co-synthesis (cont'd)

Project Architecture

- sc_clock: SysClock
 - AMBA_AXIBus: AMBA_AXIBus1
 - XilinxBRAM: XilinxBRAM1
 - IDCT: IDCT1**
 - XilinxPIC: XilinxPIC1
 - XilinxPIC: XilinxPIC2
 - VGA_CONTROLLER: VGA_CONTROLLER1
- armCortexA9: armCortexA91
 - armCortexA9.core0: armCortexA91.core0
 - makefile
 - main_armCortexA91_arm.cpp
 - Import
 - IQZZ: IQZZ1
 - VLD: VLD1
 - armCortexA9.core1: armCortexA91.core1
 - makefile
 - main_armCortexA91_arm.cpp
 - Import
 - DEMUX: DEMUX1
 - LIBU: LIBU1



Bus Interface View

Name	Bus Name	IP Type	IP Version
AMBA_AXIBus1		axi_interco...	1.06.a
armCortexA91		processing_...	4.02.a
XilinxBRAM1		bram_block	1.00.a
axi_bram_ctrl3		axi_bram_ctrl	1.03.a
DebugModule1		mdm	2.10.a
XilinxPIC1		axi_intc	1.03.a
XilinxPIC2		axi_intc	1.03.a
axi_slave_adapter0		axi_slave_a...	2.00.a
axi_slave_adapter1		axi_slave_a...	2.00.a
axi_slave_adapter2		axi_slave_a...	2.00.a
axi_slave_adapter4		axi_slave_a...	2.00.a
axi_slave_adapter5		axi_slave_a...	2.00.a
IDCT1		IDCT	2.00.a
VGA_CONTROLLER1		VGA_CONT...	2.00.a
ISSAdapter1		iss_adapter	2.00.a
ISSAdapter2		iss_adapter	2.00.a
ISSAdapter1_FIFO_0		iss_adapter...	2.00.a
ISSAdapter1_FIFO_1		iss_adapter...	2.00.a
ISSAdapter1_FIFO_2		iss_adapter...	2.00.a
ISSAdapter2_FIFO_0		iss_adapter...	2.00.a
adap_slave_IDCT1_AMBA_AXIBus1_ReadInterface		module_sla...	2.00.a
adap_slave_IDCT1_AMBA_AXIBus1_WriteInterface		module_sla...	2.00.a
fifo_IDCT1_adap_slave_IDCT1_AMBA_AXIBus1_ReadI...		module_sla...	2.00.a
fifo_IDCT1_adap_slave_IDCT1_AMBA_AXIBus1_WriteI...		module_sla...	2.00.a
fifo_IDCT1_adap_slave_IDCT1_AMBA_AXIBus1_WriteI...		module_sla...	2.00.a
signal_inverter8		signal_inver...	2.00.a

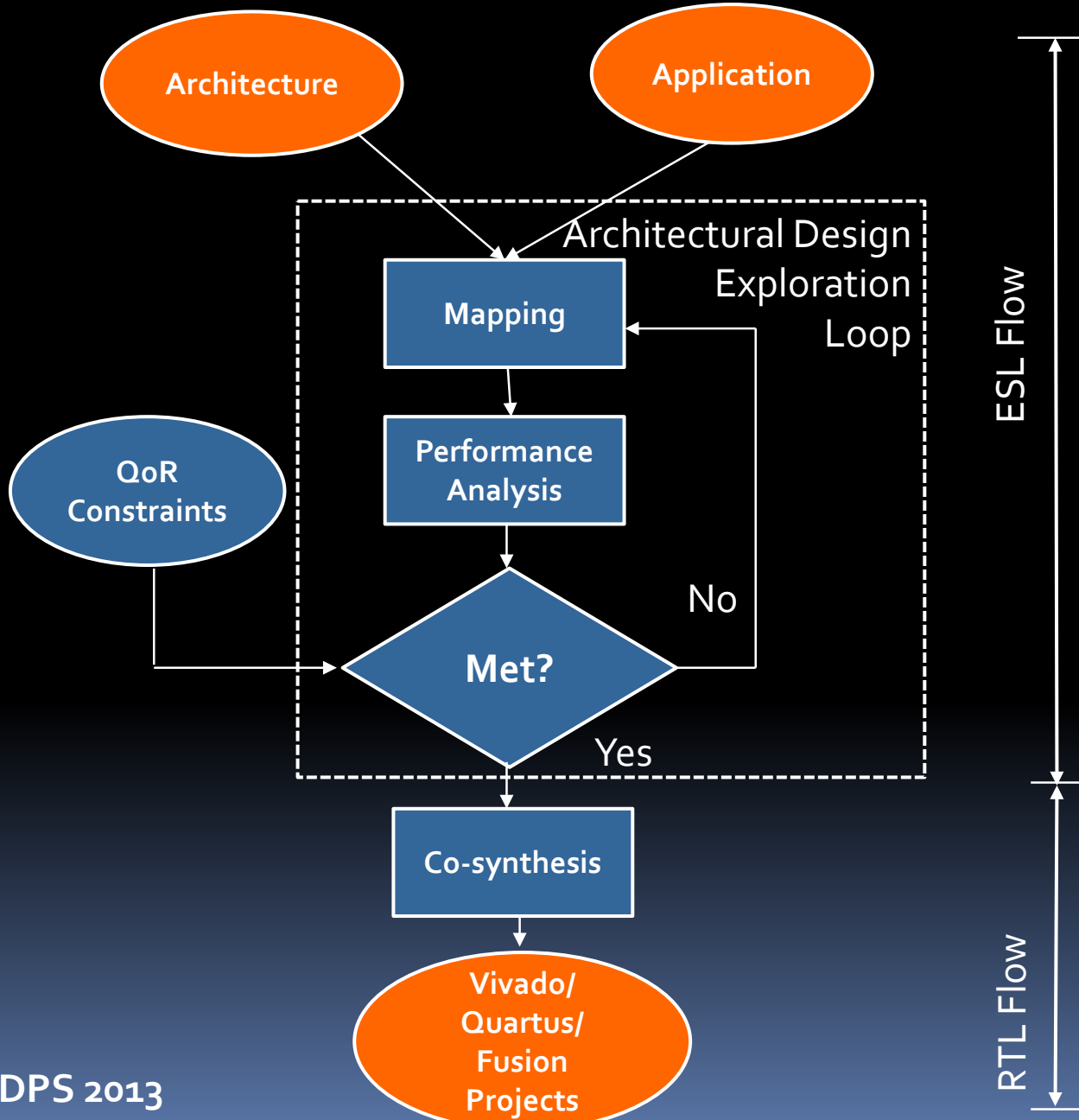
RTL IP Adapters Automatically Generated

```

15
16
17
18 -- Entity declaration
19
20 entity IDCT is
21   generic (
22     ANWIDTH: integer := 32;
23     DWIDTH: integer := 32
24   );
25   port (
26     -- Below are the SDL master links used to write into a SDL (SW is reading from this SDL)
27     --
28     -- Communication link for 3
29     SDLO_M_Clk      : out std_logic;
30     SDLO_M_Data     : out std_logic_vector(0 to DWIDTH-1);
31     SDLO_M_Write    : out std_logic;
32     SDLO_M_Full     : in  std_logic;
33

```


In summary



Benefits

Extensive automation:

- Iterations within minutes for all mapping changes
 - HW→HW, SW→SW, HW→SW, SW→HW
- OS as an IP block
- Fully transparent non-intrusive monitoring for performance analysis

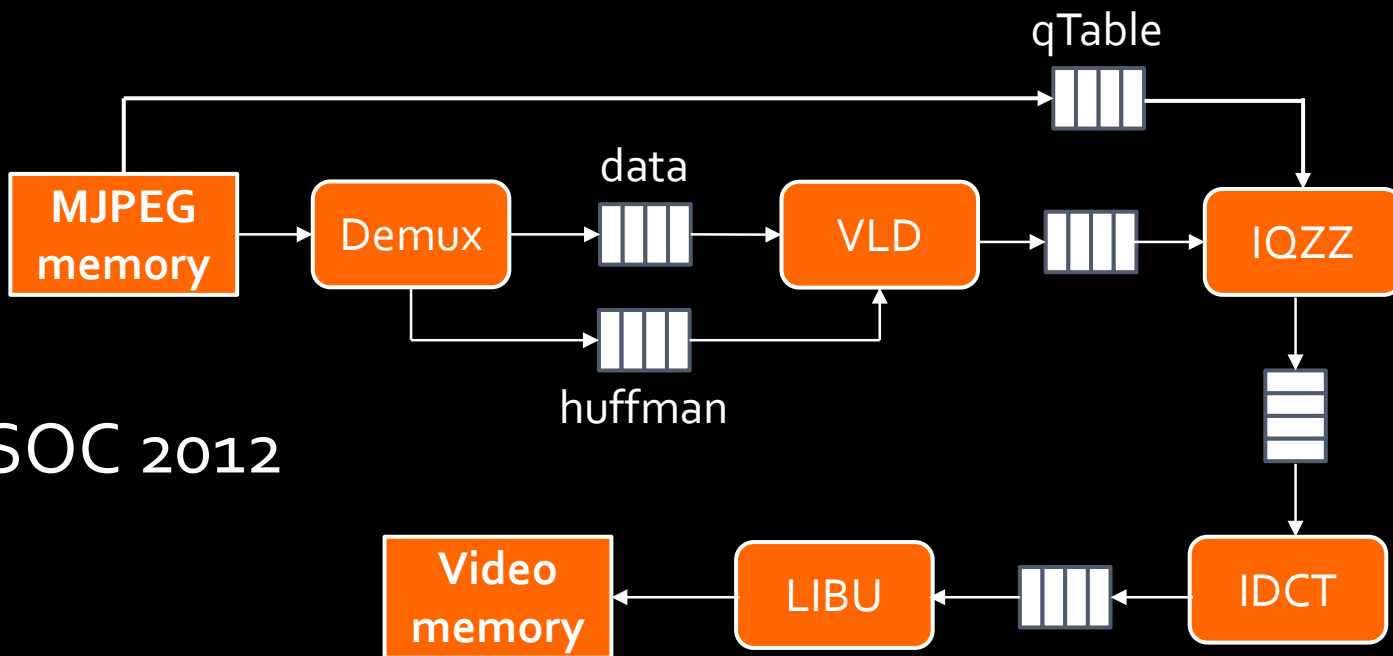
- No manual recoding to RTL
- Firmware and adapters are automatically generated

ESL Flow

RTL Flow

Case Study: M-JPEG Video Decoder

MPSOC 2012



QoR Constraint Set	Performance (FPS)	Area (Largest Device)	Power (W)
1	24	Zynq-7010	1.10
2	30	Zynq-7020	0.75
3	60	Zynq-7020	0.90

Requirements (Performance, Power, Resources)

Design Space Exploration (Part 1)

- **Rapid spec. & evaluation of 26 different architectures over 2.5 days**
 - 1 using 1 ARM Cortex-A9 core
 - 5 using 2 ARM Cortex-A9 cores
 - 7 using 2 ARM Cortex-A9 cores + 1 MicroBlaze soft-core
 - 3 using 2 ARM Cortex-A9 cores + 2 MicroBlaze soft-cores
 - 1 using 1 ARM Cortex-A9 core + HW accelerators
 - 5 using 2 ARM Cortex-A9 cores + HW accelerators
 - 4 using mix of MicroBlaze soft-cores + HW accelerators
- **Architecture has significant impact on QoR**
 - Performance goes from 10 FPS to 200+ FPS
 - Power goes from 1.15 W to 1.75 W
 - Number of HW resources used goes from 1X to 6.3X

Design Space Exploration (Part 2)

- Several architectures met FPS but used too much power
- Selected 3 architectures for power/perf. trade-off
 1. LIBU → MicroBlaze, VLD → ARM core 1, others → ARM core 2
 2. DEMUX, LIBU → ARM core 1, others → HW accelerators
 3. DEMUX → ARM core 1, LIBU → ARM core 2, others → HW

Arch.	FPGA Freq. (MHz)	ARM Freq. (MHz)	Perf. (FPS)	Power (W)	Area (Smallest Device)
1	100	500	24	1.072	Zynq-7010
2	50	333	54	0.727	Zynq-7020
3	50	333	72	0.861	Zynq-7020

- No. Cores, Mapping, HW/SW Part., Freq. Scal. ⇔ QoR
- Total manpower: 1 System Engineer over 25 hours

Conclusions

- **From the B. Bailey's Blog:**
"FPGA companies would be some of the first to implement true ESL flows"

Xilinx Builds Vivado Into Full ESL Solution, [4/3/2013](#)

- **We agree with this (e.g. , for HW/SW integration, HLS and IP's), but a complete HW/SW Co-design flow is still missing**
- **As a design creation front end for Xilinx Vivado, we have shown that SpaceStudio fills this gap.**