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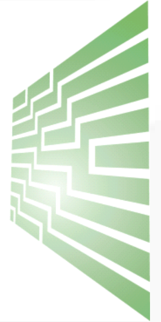

ESL Power and Thermal Modeling and Analysis

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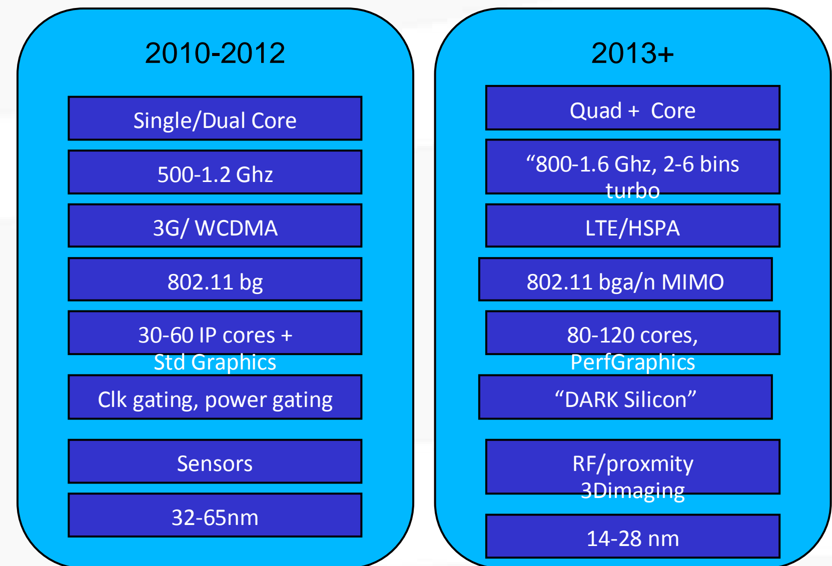
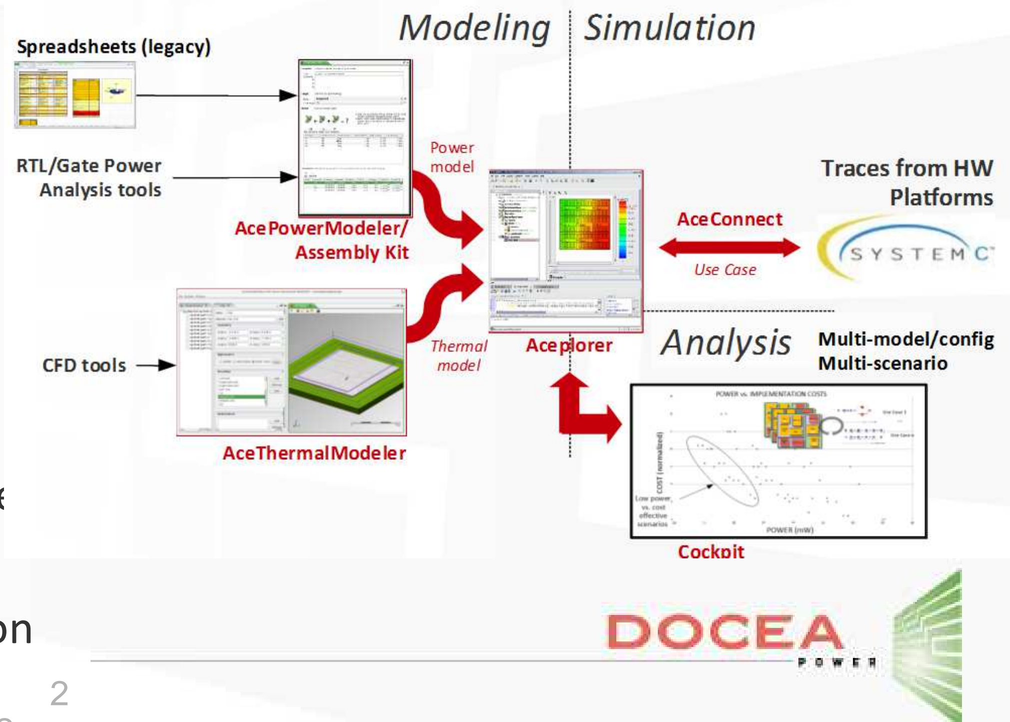
April 2013

Power saving can reach
40-70% if handled
at the Electronic System Level

Technology Challenges and Trends

- **Higher complexity and integration**
  - Smaller form – factors, especially z-height
  - Higher performance (media processing, and hence IO and memory)
  - Thermal and power constraints can hinder your innovation
- **Model size, complexity and risks compound**
  - Logic/Circuit Component models
  - Thermal models
  - Workload/trace perf models
- **Modeling, Simulation and Analysis require a better tool box**
  - Robust import/export and exchange
  - Thermal/Power coupling, Power/Perf/Functional co-simulation





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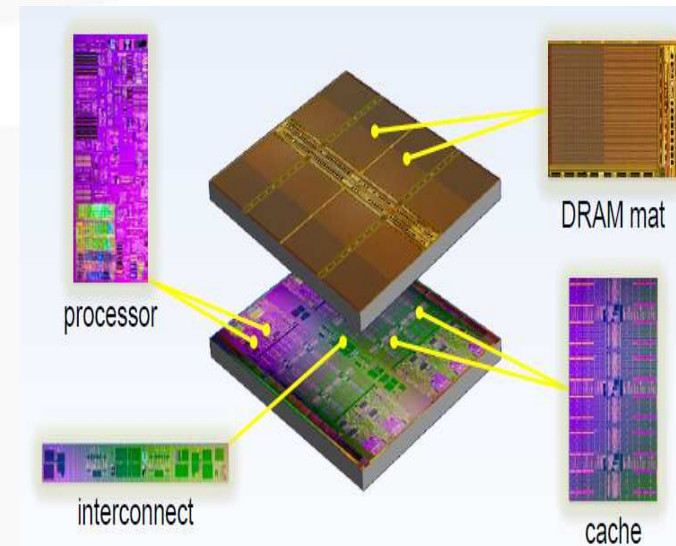
Power and Thermal Tools

- Accurate yet independent Power Models of complex components
- Models of complex Interconnects
- Mixed power models, thermal and materials
  - Especially in stacked multi-chip, POP and 2.5/3D
- System level modeling and analysis from Soc chip level all the way to the application



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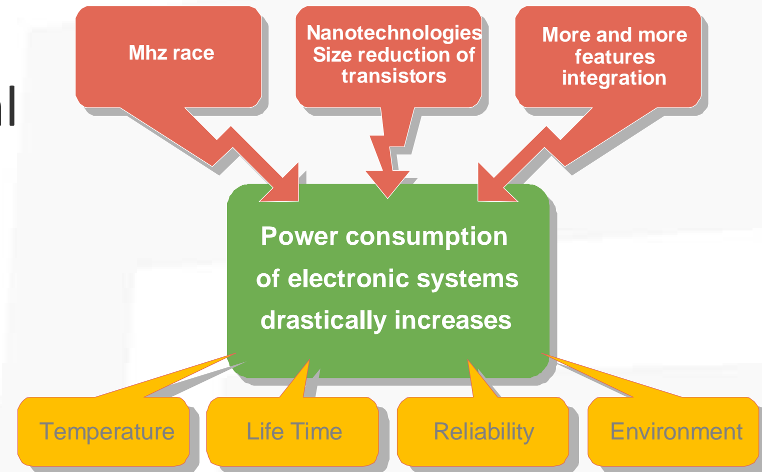
Summary

- Coupled Power and thermal modelling and simulation is critical
- Designing for the thermal limits are key for 2.5/3D-Chip designs
- Architectural level is where most of the power can be saved



- Increasing design complexity requires system approach along with higher level of abstraction: Chip-Package-Board-Software
- Power consumption optimization requires a new design flow and process throughout the supply chain

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