Adapt-IP

Michael McNamara, CEO

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Overview

- We created Adapt-IP in 2012 to apply System-Level design tools and techniques for the commercial creation and deployment of standard IP
  - For each standard protocol or accelerator, we provide
    - Soft IP implementing the logic, targeted at the customers' technology library or FPGA
    - Firmware coordinating the functionality
    - Device driver integrating the device to the O/S
    - Virtual platform model facilitating fast bring up
- In addition we are structured to customize the design to add (or often, to delete) functionality to better fit project requirements

The Company

- Michael McNamara, CEO
  - 7 years at Cadence, VP of System Level Design
  - Director, SVP at Verisity Design (sold to Cadence in 2005)
  - CEO of SureFire Verification (sold to Verisity in 1999)
  - VP Engineering, Chronologic (created VCS)
  - Designer at TRW, Cydrome, Ardent
- Phil Tharp, CTO
  - CEO Vreelin Engineering (USB1, 2 and USB3 cores)
  - 20 Years at NASA, Intel & Adobe
- Sean Smith, Principle Engineer
  - 5 years at Denali, CTO
  - 15 years as Verification expert, Cisco
- Dr. John Sanguinetti, Chairman
  - CTO, Forte Design
  - CEO Chronologic
- Dr. Lucio Lanza, LanzaTech Ventures, Director

Products

Available

- USB 3.0 host, device & embedded host
- USB 2.0 host, device & embedded host

Under Development

- HEVC Decoder & Encoder
- LTE hard & soft IP

Conclusion

- System Level Design & Verification
  - Design Works
    - Generate designs in the *same* amount of time as it would take to write RTL
    - Retarget designs in *days*
  - Verification is faster
    - VIPs work at the System Level
    - Then we need do just Validation at RTL Level
  - Implementation is still a challenge
    - FPGA realization requires patience with the tools
    - ASIC realization remains time consuming
    - The rapid retargeting feature of SLD helps reduce the implementation bottleneck