SYSTEM LEVEL EMULATION:
WHY IS IT STILL SO HARD?

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SYSTEM LEVEL EMULATION
WHAT DO INTEGRATED PROGRAMMABLE FABRICS AND PROCESSORS DELIVER?

- The current generation of programmable fabrics combined with hard processor cores (for example, the Xilinx Zynq 7000 series and similar Altera products) offer:
  - Rich arithmetical resources (multiplier or MAC cores),
  - Generous resources for implementing random logic,
  - Adequate in-fabric memory, which can be augmented by external external memory (hard memory controllers make this more attractive).
- Now we have fast processors cores that can be closely coupled to the fabric. These cores run commodity operating systems (usually Linux), for which we can readily recruit developers. What's not to like? Our system emulation problems are solved, right?

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WHAT DO INTEGRATED PROGRAMMABLE FABRICS AND PROCESSORS DELIVER?

Despite all of the promises, even with integrated processors cores, the FPGA remains the world's hardest-to-use SRAM.

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WHY IS IT SO HARD?

The fundamental problem is that once we have a system the involves hardware and software, we have three problems: the design the hardware, writing the software and building and debugging the HW/SW interface.

The trouble is more than it appears at first glance because we have to treat software and hardware at different levels of abstraction.

- Hardware intellectual property tends to come in smaller blocks with limited functionality, which need to be stitched together to build a solution.
  - Tool support for this process is still mediocre.
  - There are also few large, high quality examples for beginning designers to examine and learn from.
  - After thirty years, we still have a choice between a rock (VHDL) and a hard place (Verilog)!?

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WHAT CAN BE DONE TO MAKE IT BETTER?

Integrating general purpose processors into programmable fabrics is a necessary, but not sufficient, condition for speeding up the task of system level emulation.

- We still need to raise the level of abstraction of the hardware design. But the low level we work at is dictated by our tools. Could hardware designers learn from the experience of the LLVM compiler?
  - Target our designs for a virtual logic/memory/DSP fabric.
  - The vendors' proprietary magic can live in the mapping from the virtual to the physical fabric.
- We ought to be using the capabilities of the processors to speed up the design cycle. It's easy enough to put an ethernet interface, full IP stack and a webserver into one core. Why am I still using JTAG?

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SUMMARY

The latest generation of programmable systems-on-a-chip provide and embarrassment of riches in computing resources.

We ought to be embarrassed that we are not using them as well as we can to get designs out the door faster.

There are many opportunities to make things better, but the biggest bang for the buck is probably going to come from raising the abstraction level of the hardware.

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