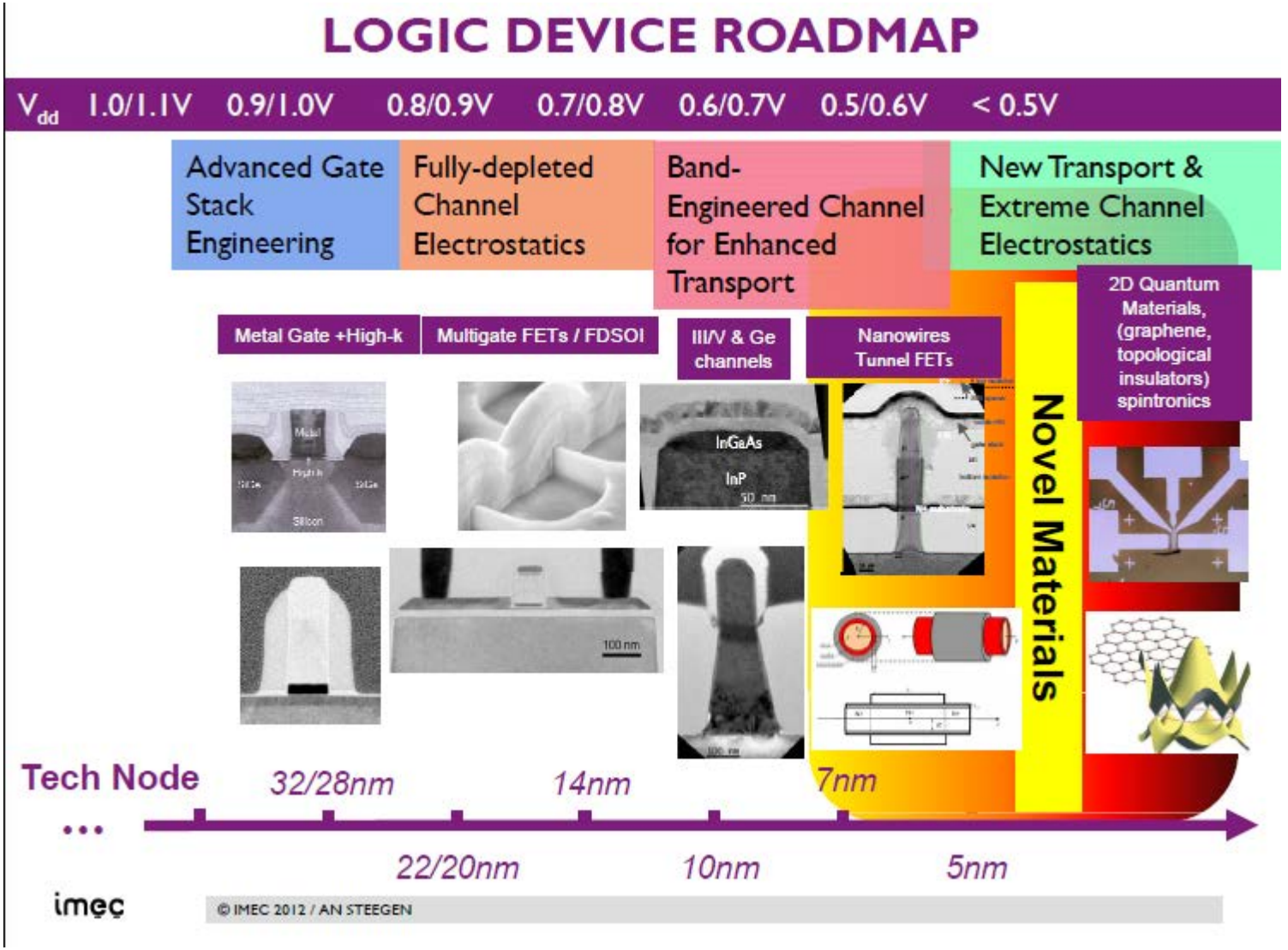
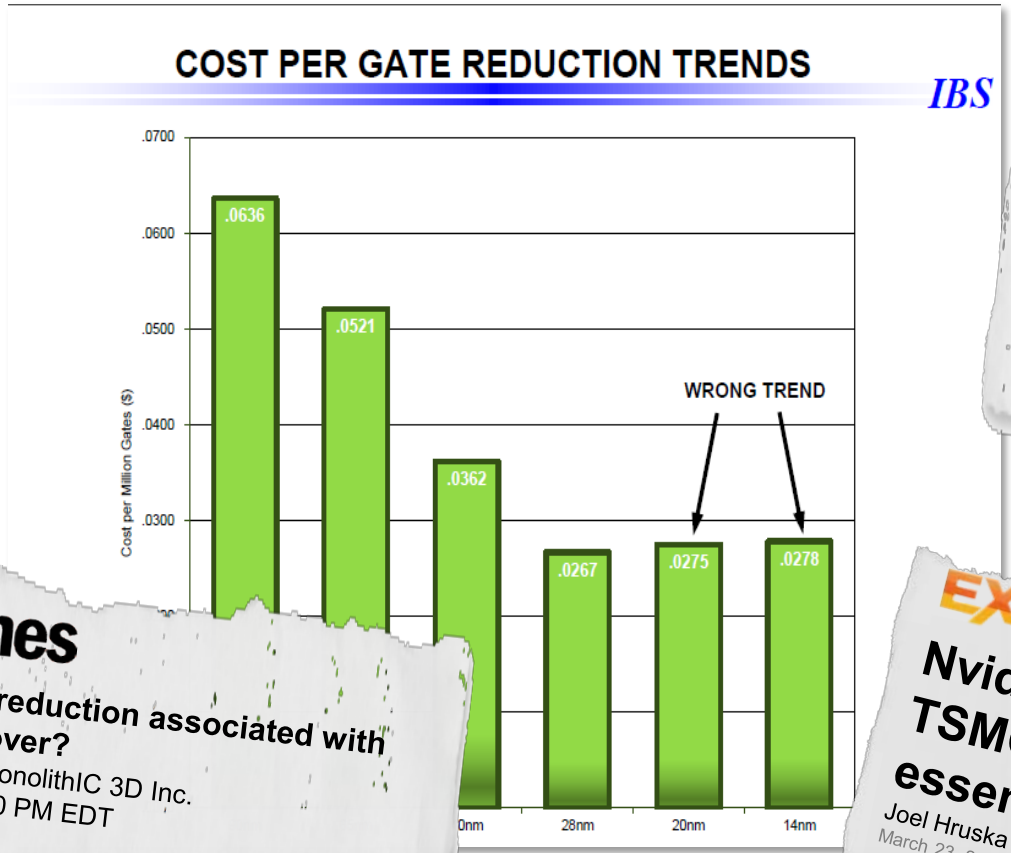

# FPGA Entering the Era of the All Programmable SoC

**Ivo Bolsens,**
**Senior Vice President & CTO**

# Moore's Law: The Technology Pipeline



# Industry Debates on Cost




EE Times

**TSMC raises capex to record $8.5 billion, pulls in 20-nm**

Peter Clarke
4/26/2012 12:23 PM EDT

LONDON – Taiwan Semiconductor Manufacturing Co. Ltd. has raised its planned capital expenditure for 2012 to between $8 billion and $8.5 billion. The move accompanied the announcement of first quarter financial results and strong second quarter outlook by the foundry.

EE Times

**Is the cost reduction associated with IC scaling over?**

Zvi Or-Bach, MonolithIC 3D Inc.
7/16/2012 12:20 PM EDT

The last 50 years of the semiconductor industry have been all about the manifestation of Moore's Law with regard to the dimensional scaling of Integrated Circuits (ICs). As consumers of electronic devices, we all love to see better products at a lower cost with each and every new product cycle. But now storm clouds are forming,

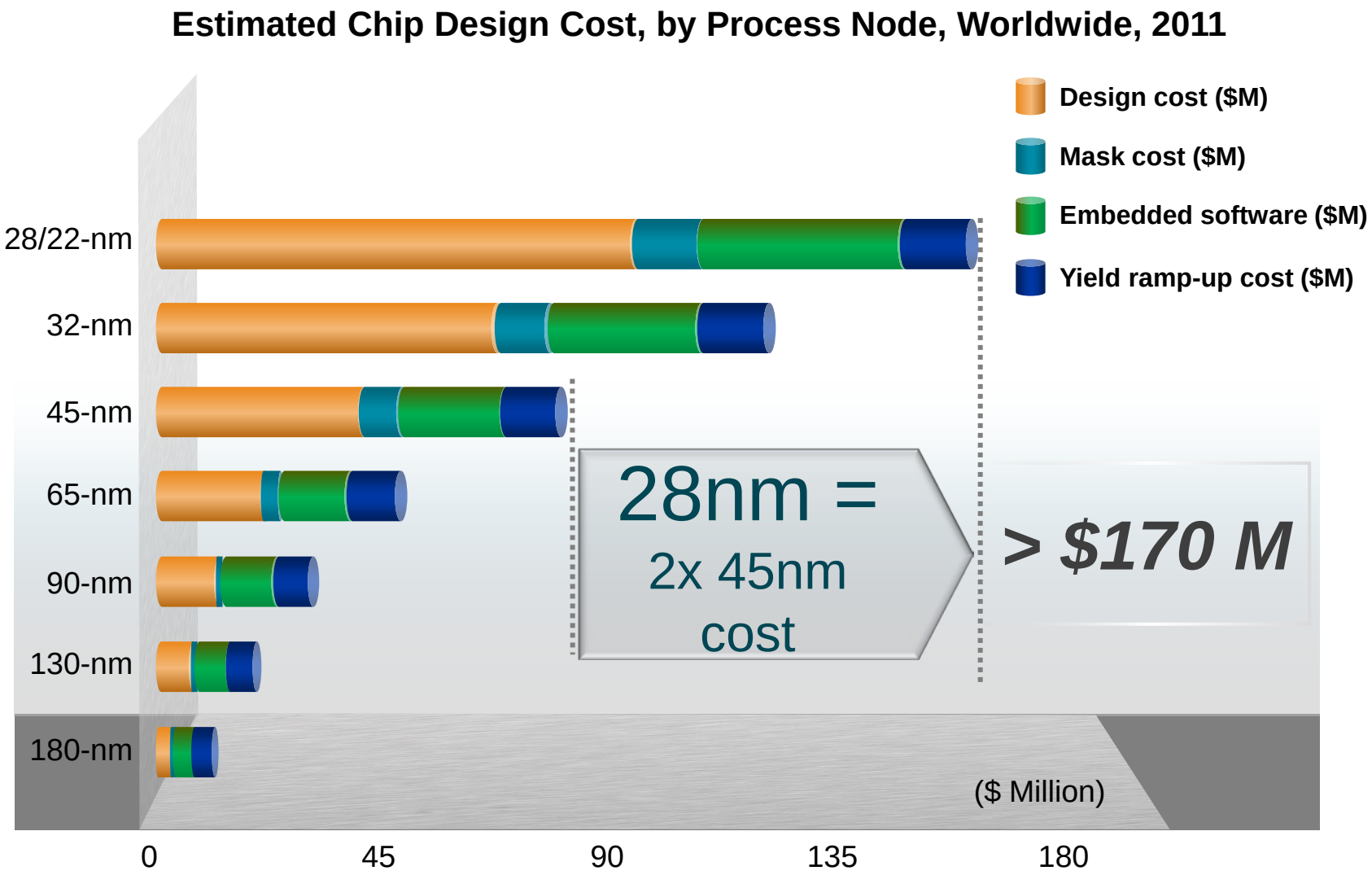
EXTREMETECH

**Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless**

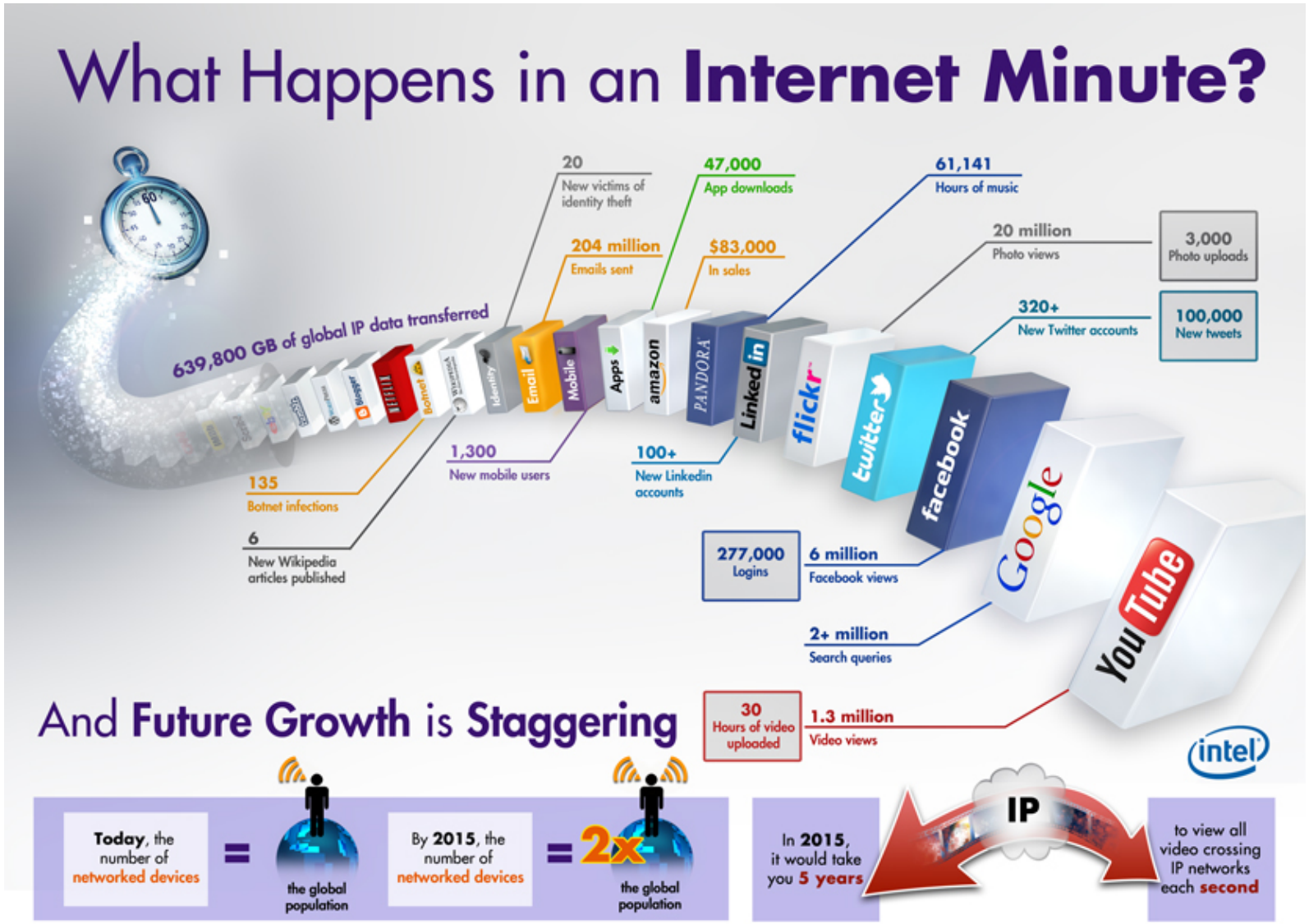
Joel Hruska
March 23, 2012 at 12:13 pm

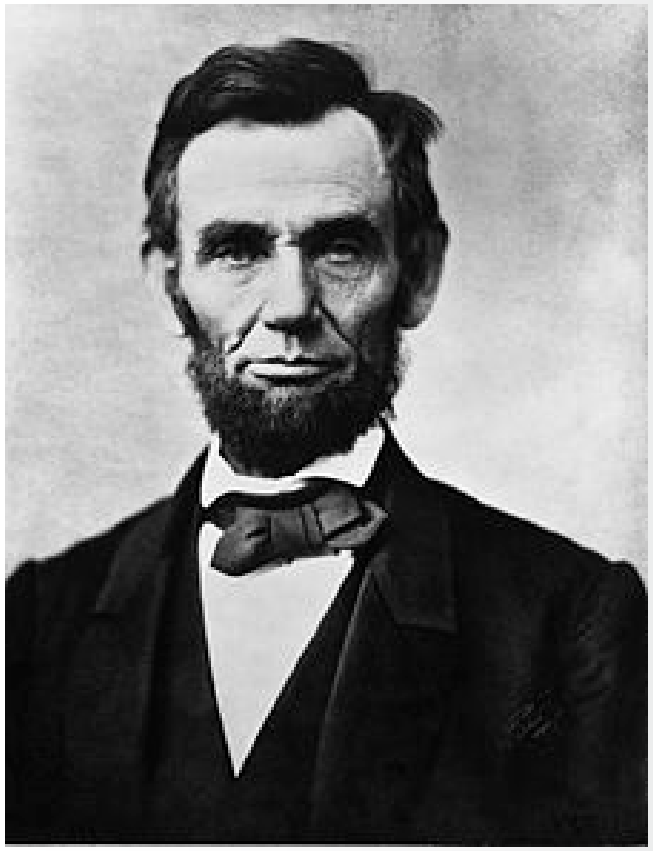
One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia

# Design Cost



# Internet





*"Don't believe everything you read on the Internet."*

***Abraham Lincoln,***
***U.S. President***

Photo Source: Wikipedia

# More Intelligence in Every System

## SMART Data Center Revolution

New Opportunities to Control Costs and Increase Strategic Advantage…

MACHINES THAT UNDERSTAND

embedded VISION ALLIANCE

## Smart wireless networks to the rescue

Carriers are turning toward more intelligent network management…

## The Next Big, Digital Economy; 'Smart Energy'

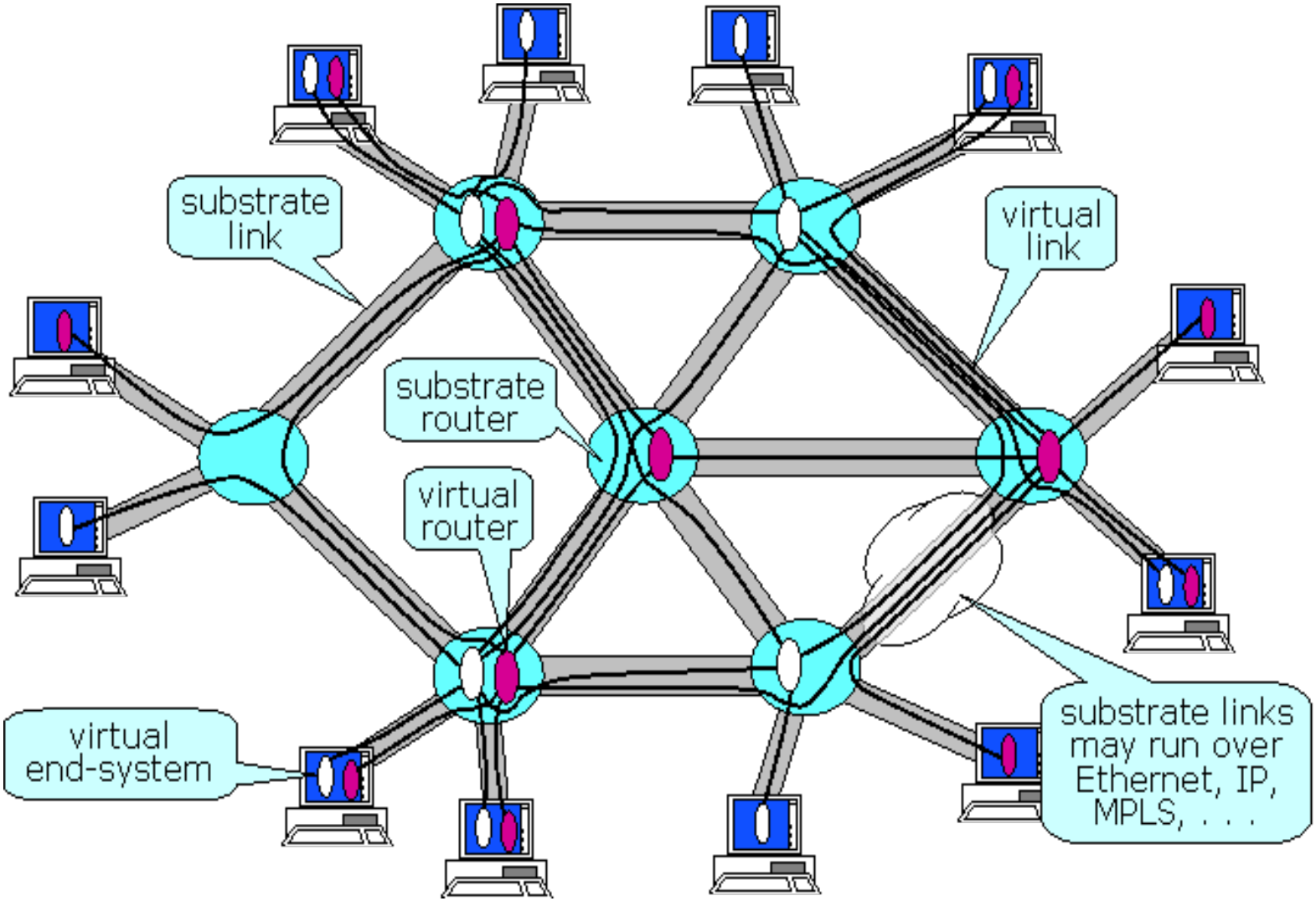
The energy market is undergoing a major transformation…

## Smart Factories

For factory management in the future, it will become essential to strive to implement smart capabilities…

From Dumb Pipes to Smart Networks

# Trend Wired Infrastructure: Software Defined Networks




**Slide credit:** From “Virtualizing the Net” by Jon Turner (2004)

# Trend Wireless Infrastructure: Scalable Platforms

*Capacity*

**Indoor**

**Residential Femto**

4-16 Users
<100mW

Home

**Enterprise Femto**

30-60 Users
<250mW

Office

**Picocell**

30-200 Users
<1W

Dense Indoor
(Malls, Transport Hubs)

**Outdoor**

**Microcell**


Urban Infill

~200 Users
<1-10W
Single Sector

**Macrocell**

Wide Area

~200 Users/ sector
20-100W
Multi-Sector

**Macrocell + Active Antennas**

Wide Area

**2-3x Data Capacity of RRU**

*Coverage*

# Trend Data Center Infrastructure: Cloud Computing

## Big Data

Increasing Volume, Velocity, and Variety

## Low power

Reduce operation and cooling costs

## Security

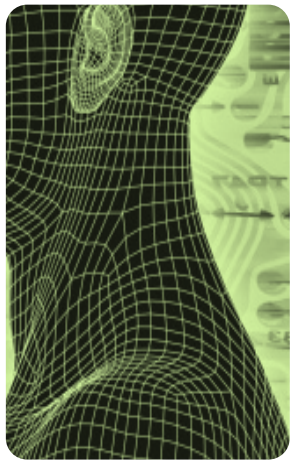
Both outside and inside

# Industry Mandates

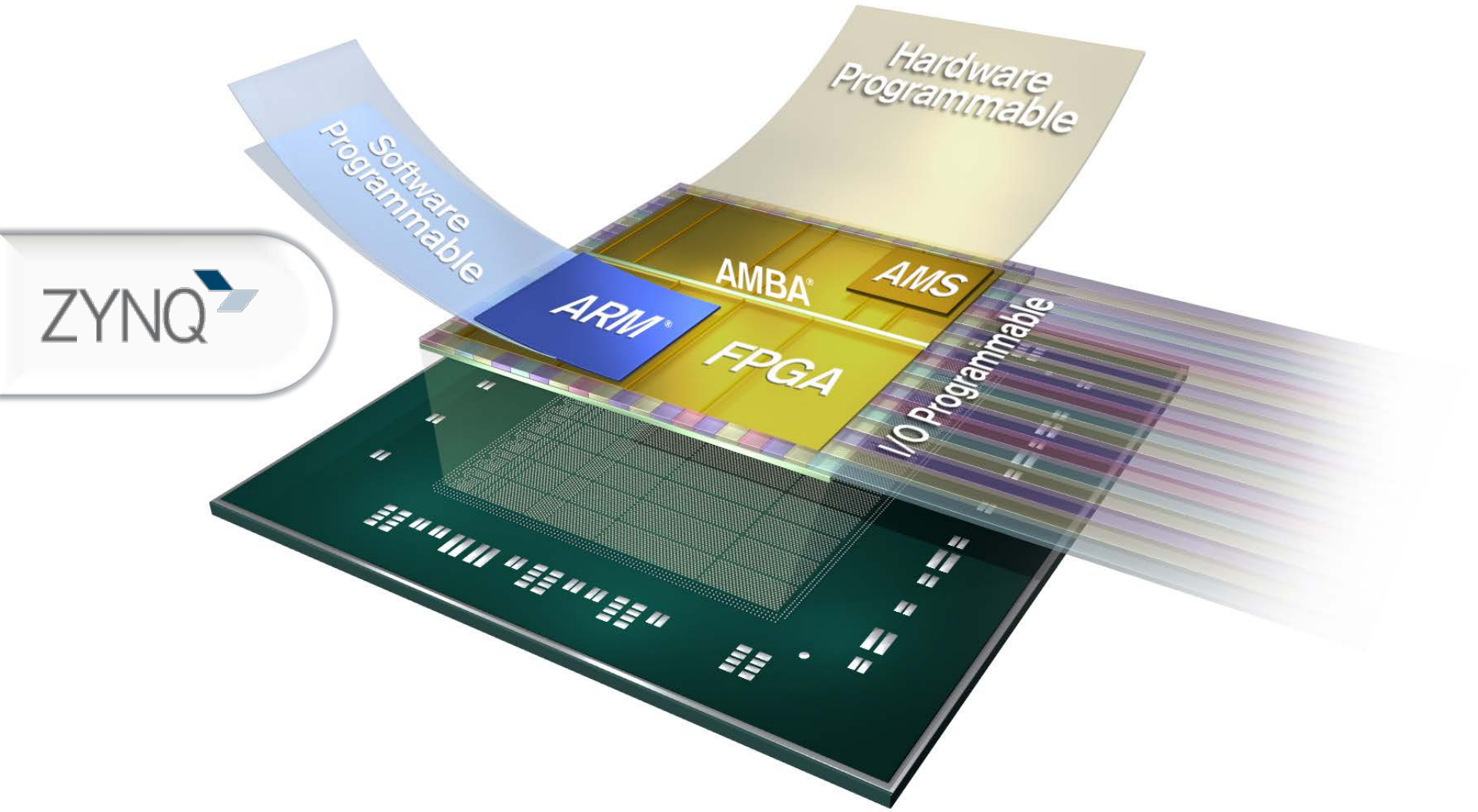
**Programmable Imperative**

**Programmable Systems Integration**

**Insatiable *Intelligent* Bandwidth**

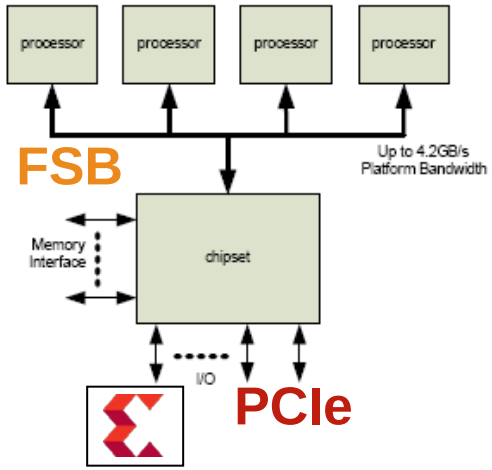


# The Era of All Programmable SoC

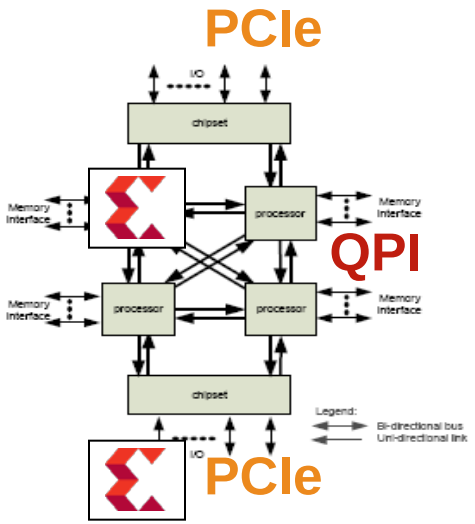


# CPU + FPGA Evolution

**2005**

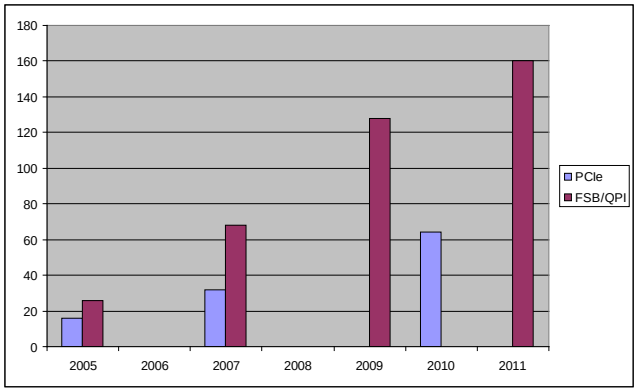



**2011**



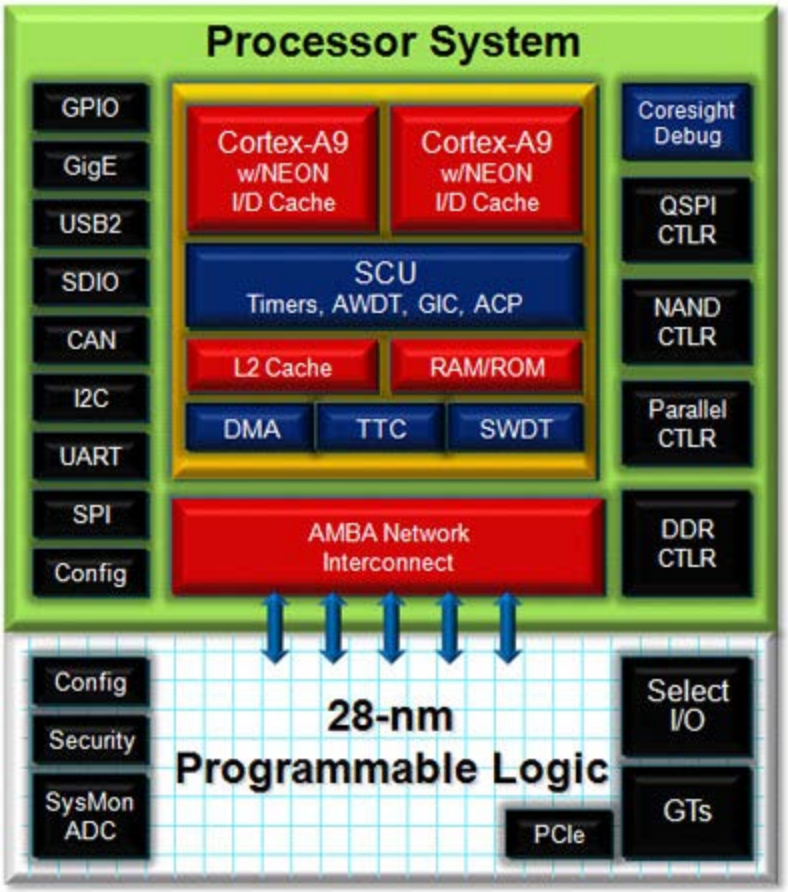

| | | |
|---|---|---|
| Equal BW: FSB vs PCIe | → | FSB/QPI: 2x PCIe BW |
| PCIe IO Device | → | In-Socket Accelerator |
| Cache Flush | → | Direct Cache Access |
| Device Driver Call | → | Shared Memory Function |

## Bandwidth



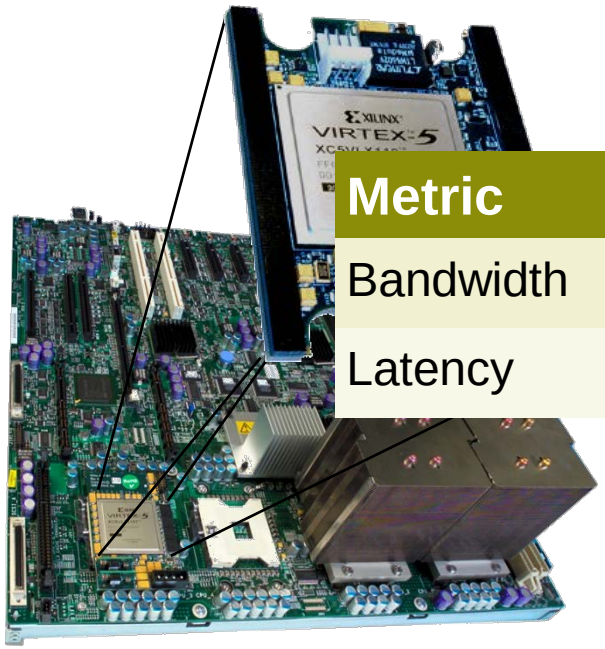
# Extended Processing: Embedded ARM

- **Processor System boots first**
  - Separate power for PL*
  - Peripherals alive before PL configuration
- **Processor controls PL configuration**
  - Multiple security levels supported
  - Boot in secure or non-secure mode
  - Download PL image via network, SD, USB
- **Multiple AXI interfaces to PL**
  - Processor System can access IP in PL
  - PL IP has access to Processor System peripherals and memory system at full BW

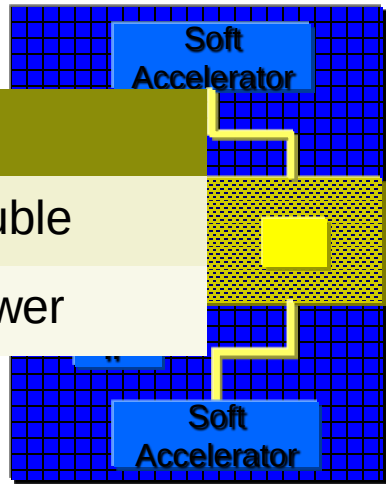



*PL = Programmable Logic

# Programmable Platform Opportunity

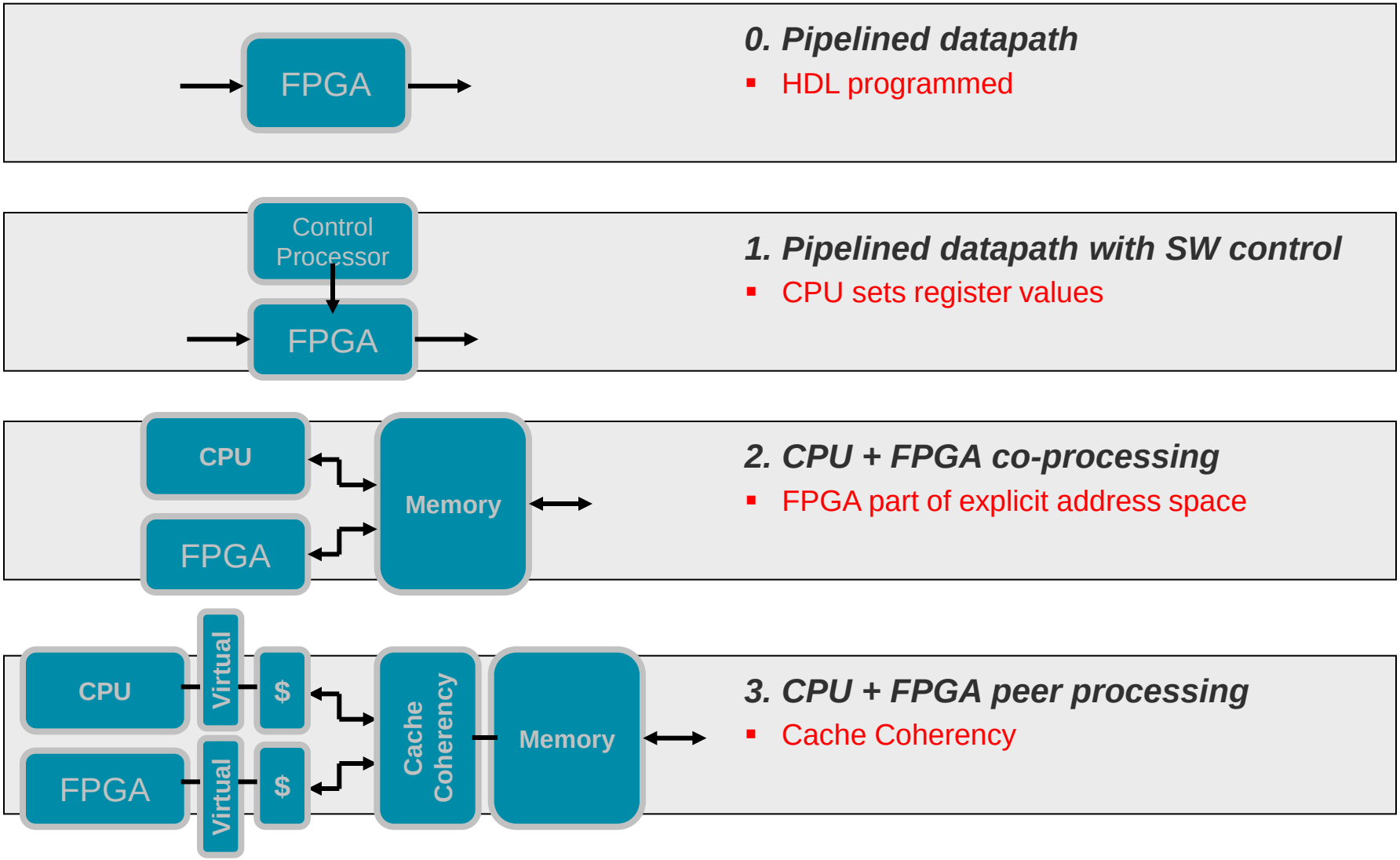



| Metric | |
|---|---|
| Bandwidth | > Double |
| Latency | 4x lower |

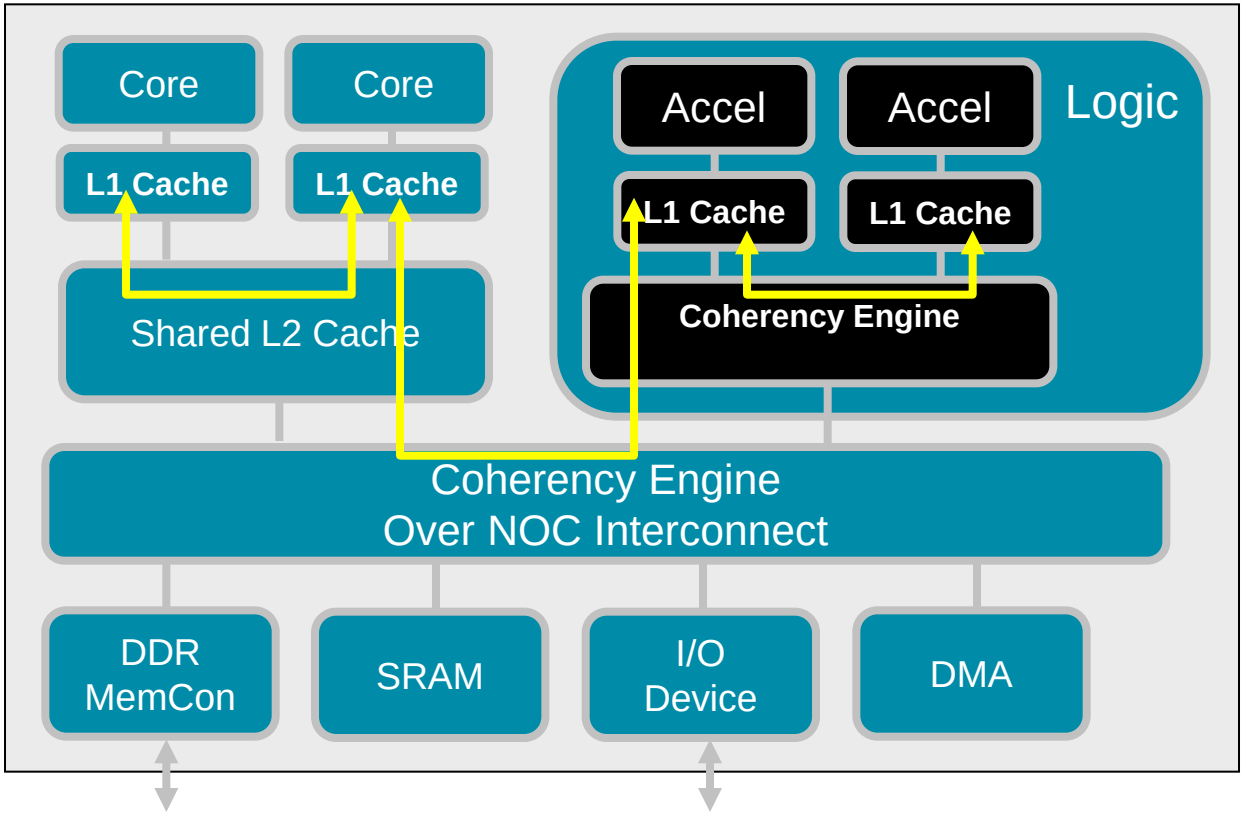



***Major Leap in Cost and Performance***

# FPGA/CPU Use Models



# Programmable Platform: CPU + FPGA Peer Processing



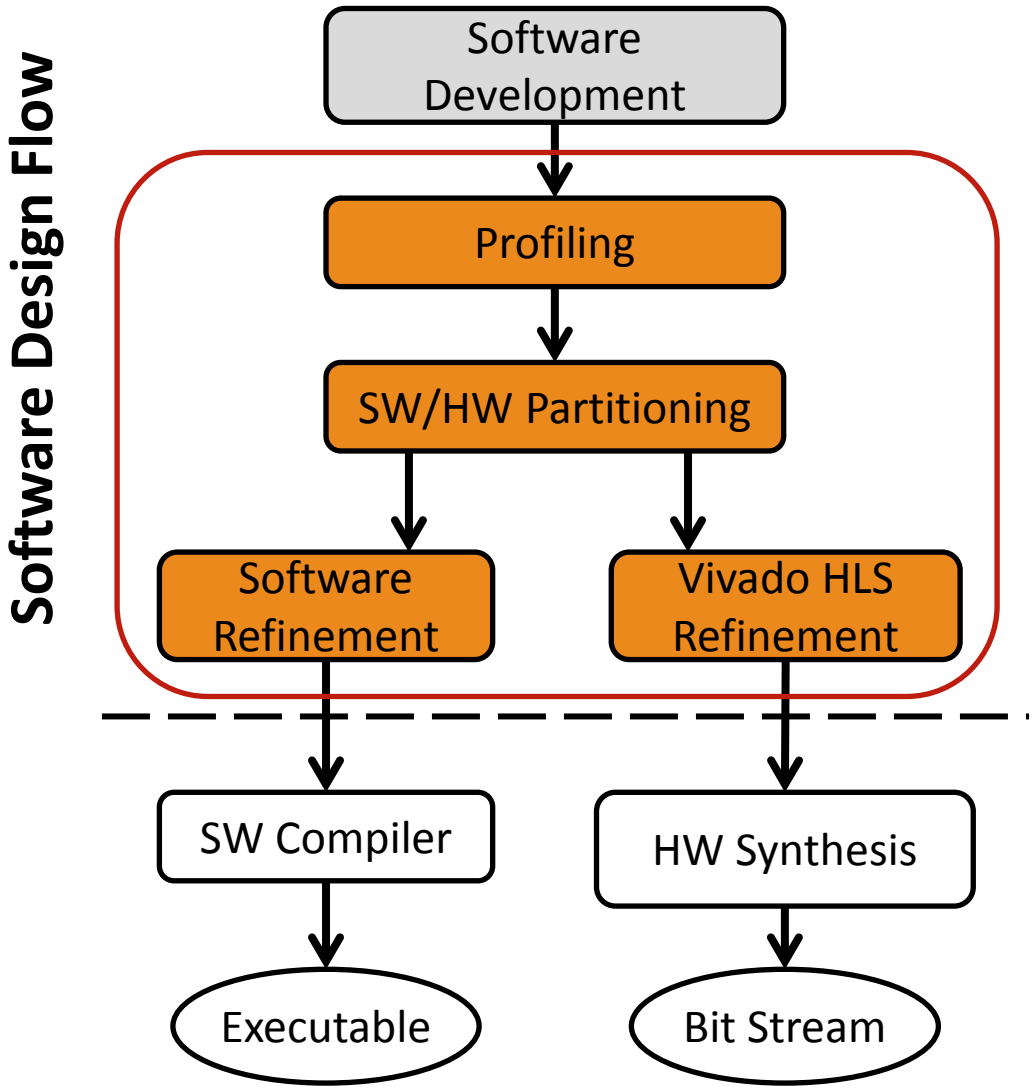

## Capabilities

- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management

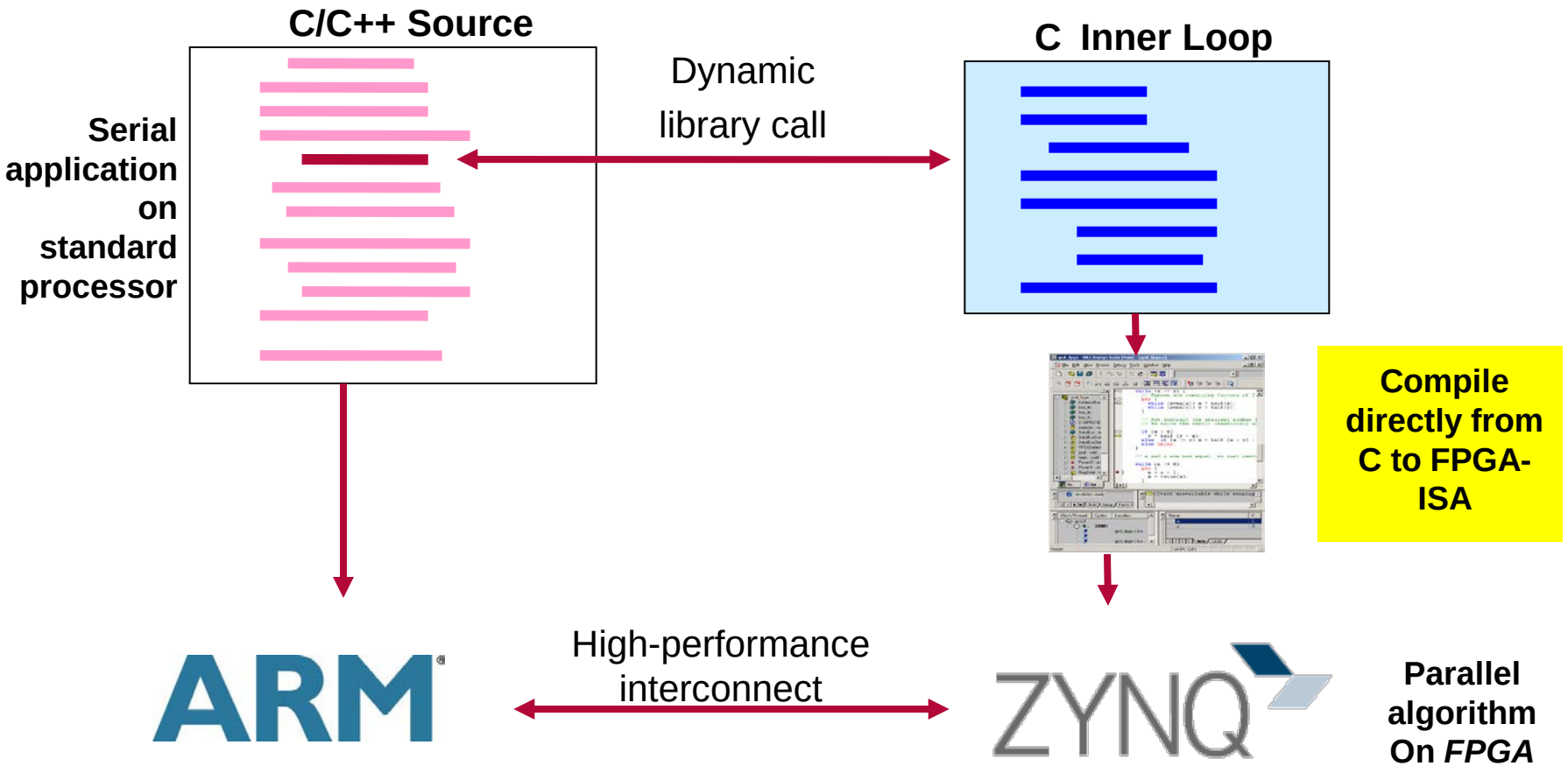
**Coherency Benefits:**

- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed

# Design Flow Overview

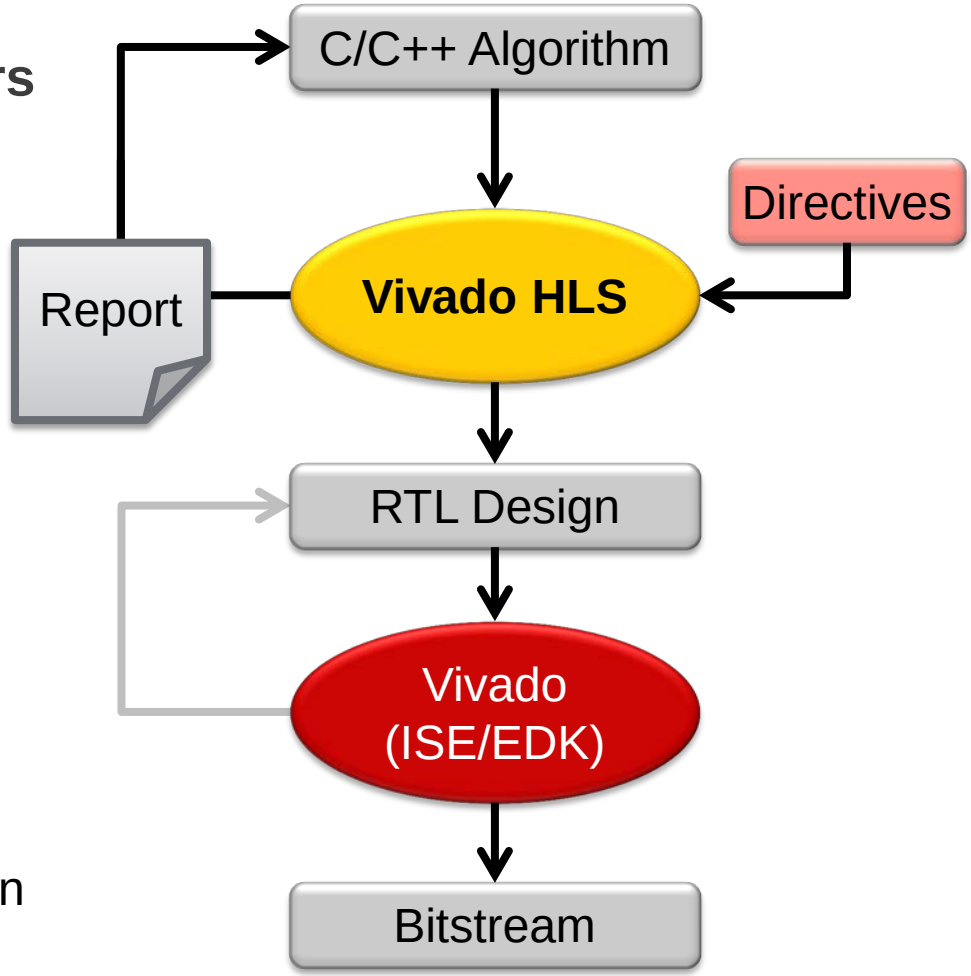


# Programming Accelerators from C/C++



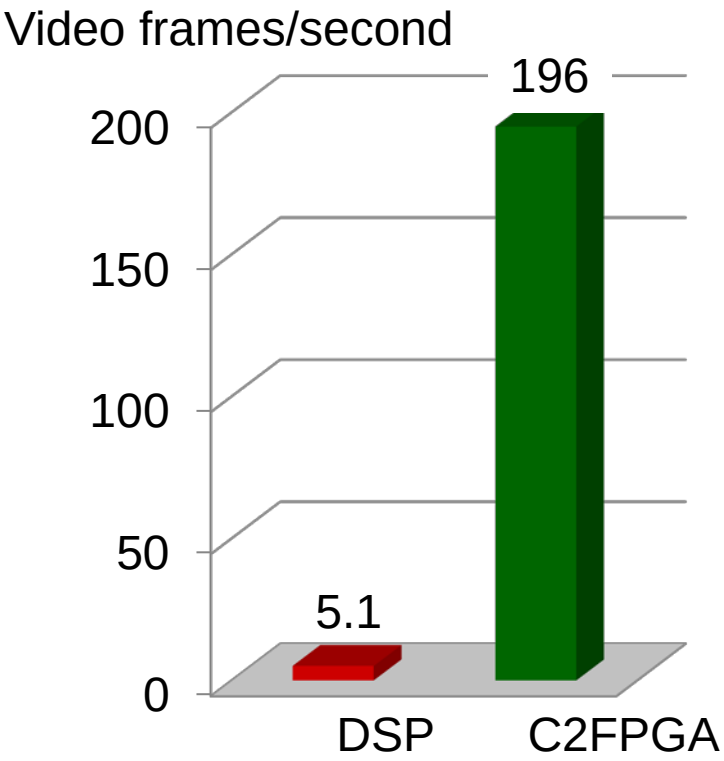
# Programming Accelerators from C/C++

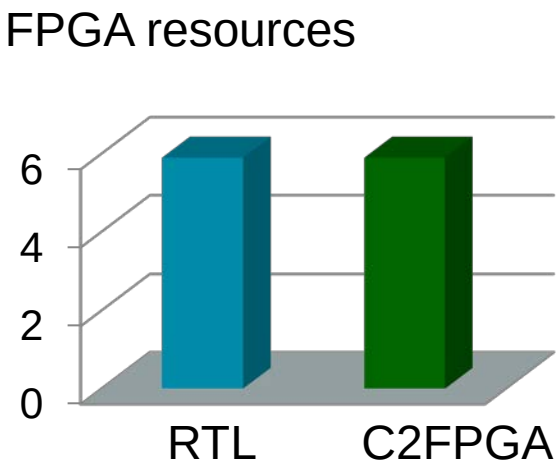
- **Enables software programmers to target Xilinx FPGAs**
  - Software-programmability
  - Portability: 7 series, Zynq
- **Delivers productivity increase for RTL designers**
  - C/C++ level verification and testbench reuse
  - Earlier area/latency reports
  - Software-driven design exploration




**More Turns Per Day (Verification and Architecture Exploration)**

# Quality of Results




**FPGA:** >38 times better performance than DSP video processor

**QOR:** C2FPGA equal to or better than RTL synthesis

**Ease-of-use**: C2FPGA 2x fewer lines of C code than DSP processor

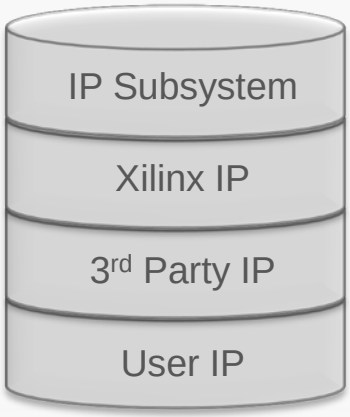
# Vivado IP Integrator

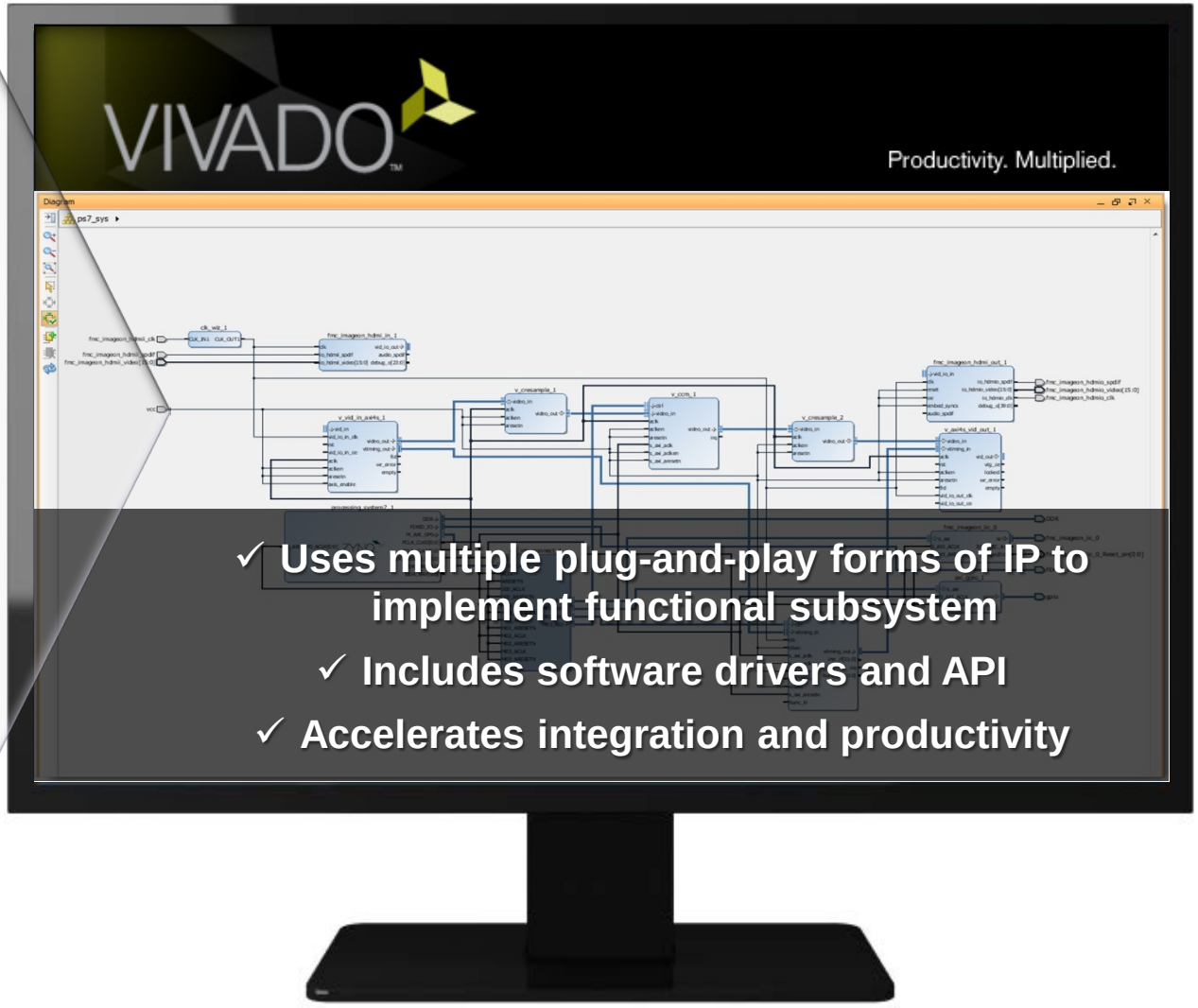
## Enabling Reuse and Delivering Fully Functional IP Subsystems

### IP Packager

- Source (C, RTL, IP)
- Simulation models
- Documentation
- Example Designs
- Test bench

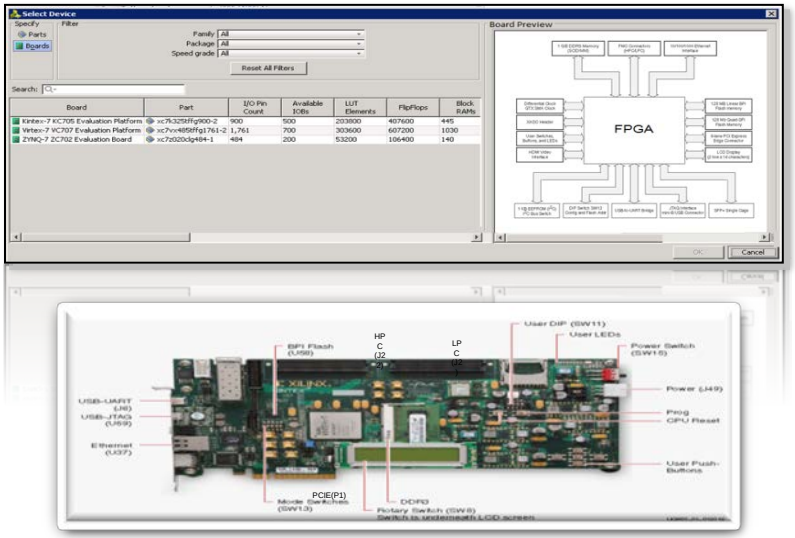
### Standardized IP-XACT



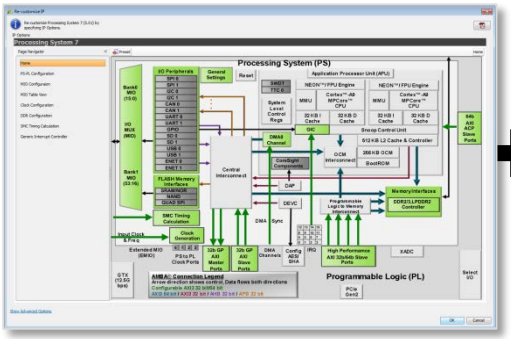
# Vivado IP Integrator

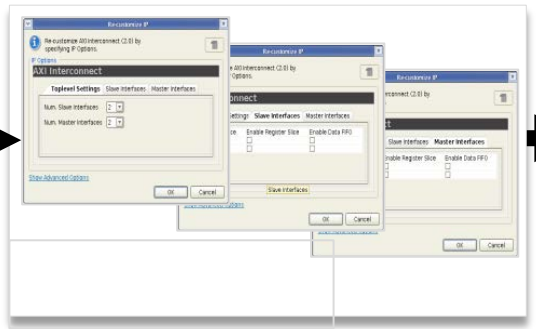
## Intelligent IP Integration

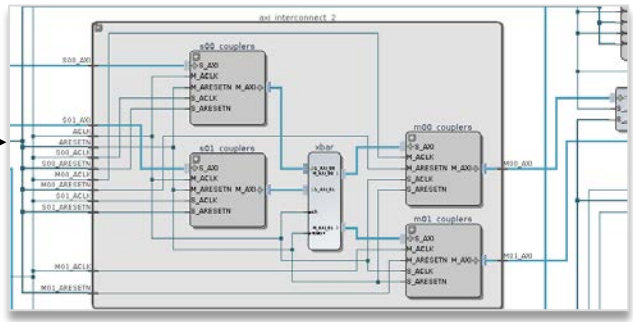



- **Co-Optimized for platforms**
  - Target platform aware
  - Supports All Programmable Zynq and 7 series kits

- **Co-Optimized for silicon**
  - IP aware automated AXI Interconnects for maximum performance or area
  - Automated interface, device driver & address map generation for Zynq and MicroBlaze

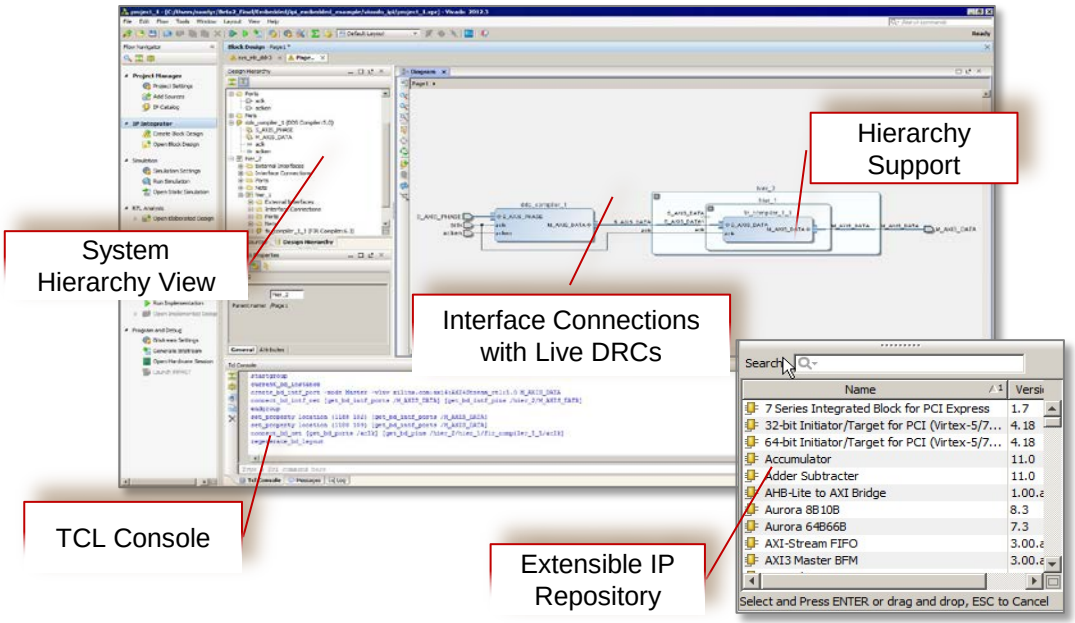


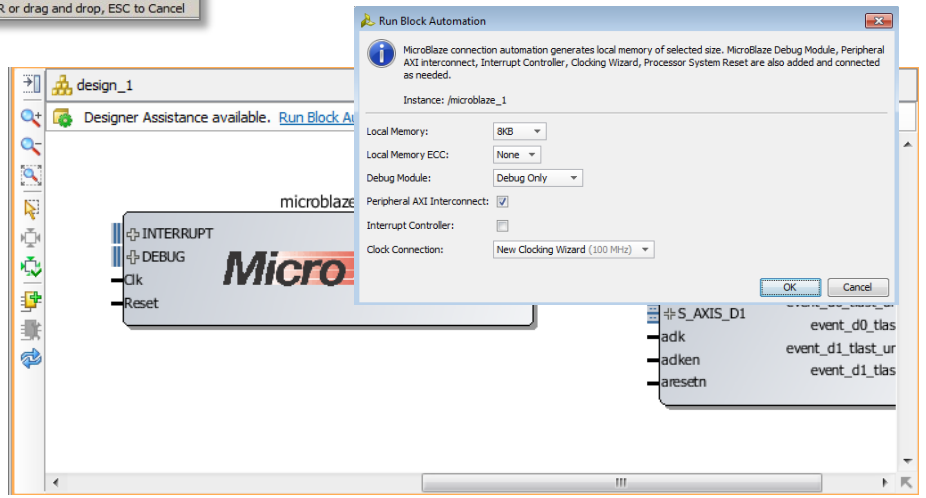
# Vivado IP Integrator

## Intelligent IP Integration

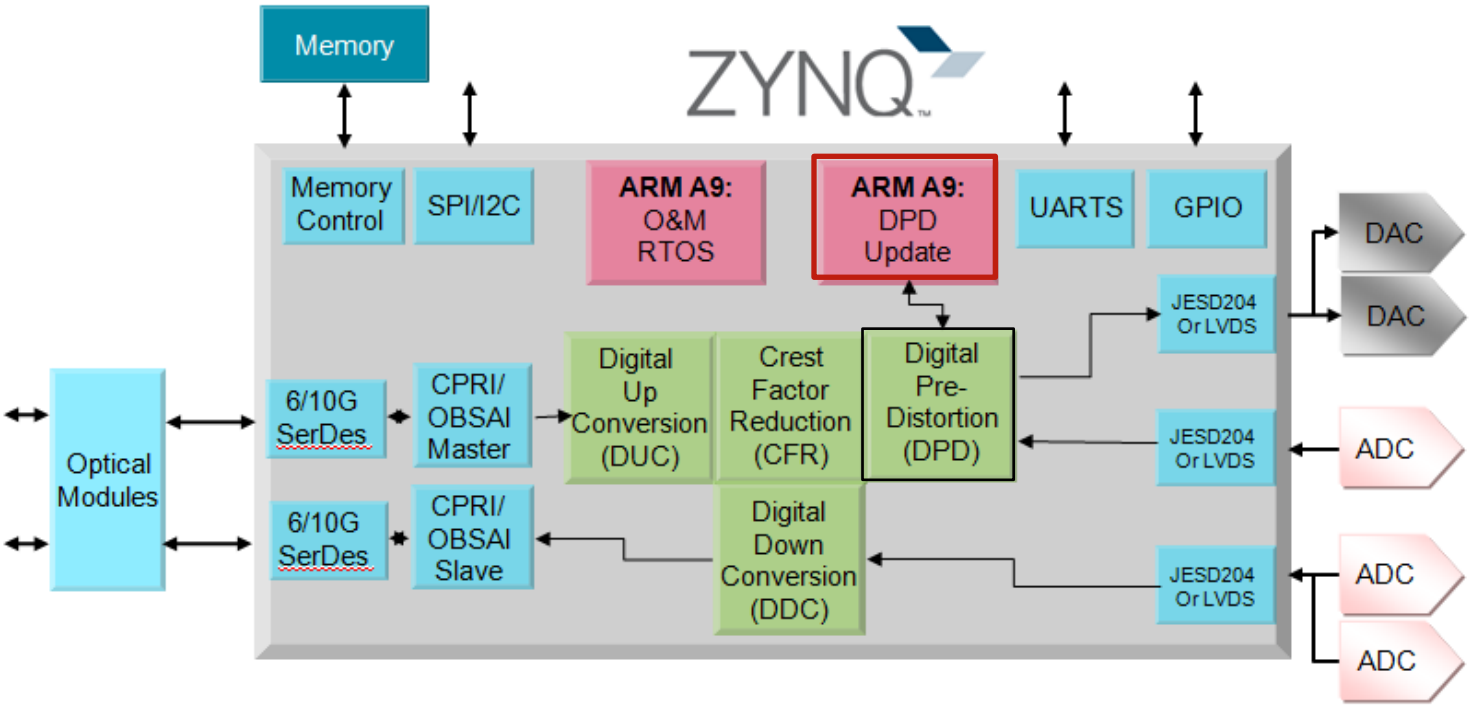



- **Correct-by-construction**
  - Extensible IP repository
  - Real-time DRCs and parameter propagation/resolution

- **Automated IP Subsystems**
  - Block automation for rapid design creation
  - One click IP customization

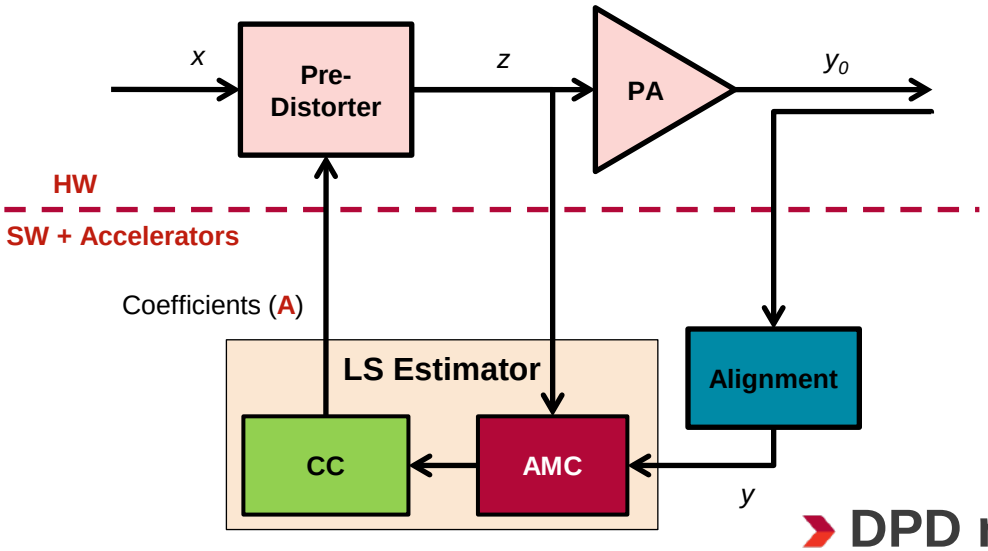


# Zynq in Wireless Digital Front End

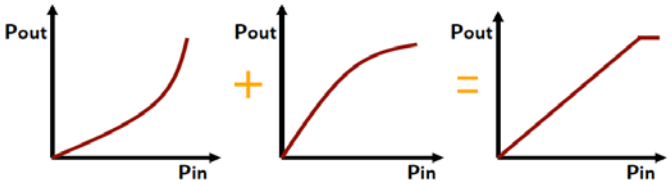



- Cost and power reduction by integrated solution
- Performance increase by exploiting the massive compute power of multi-core processors and programmable logic

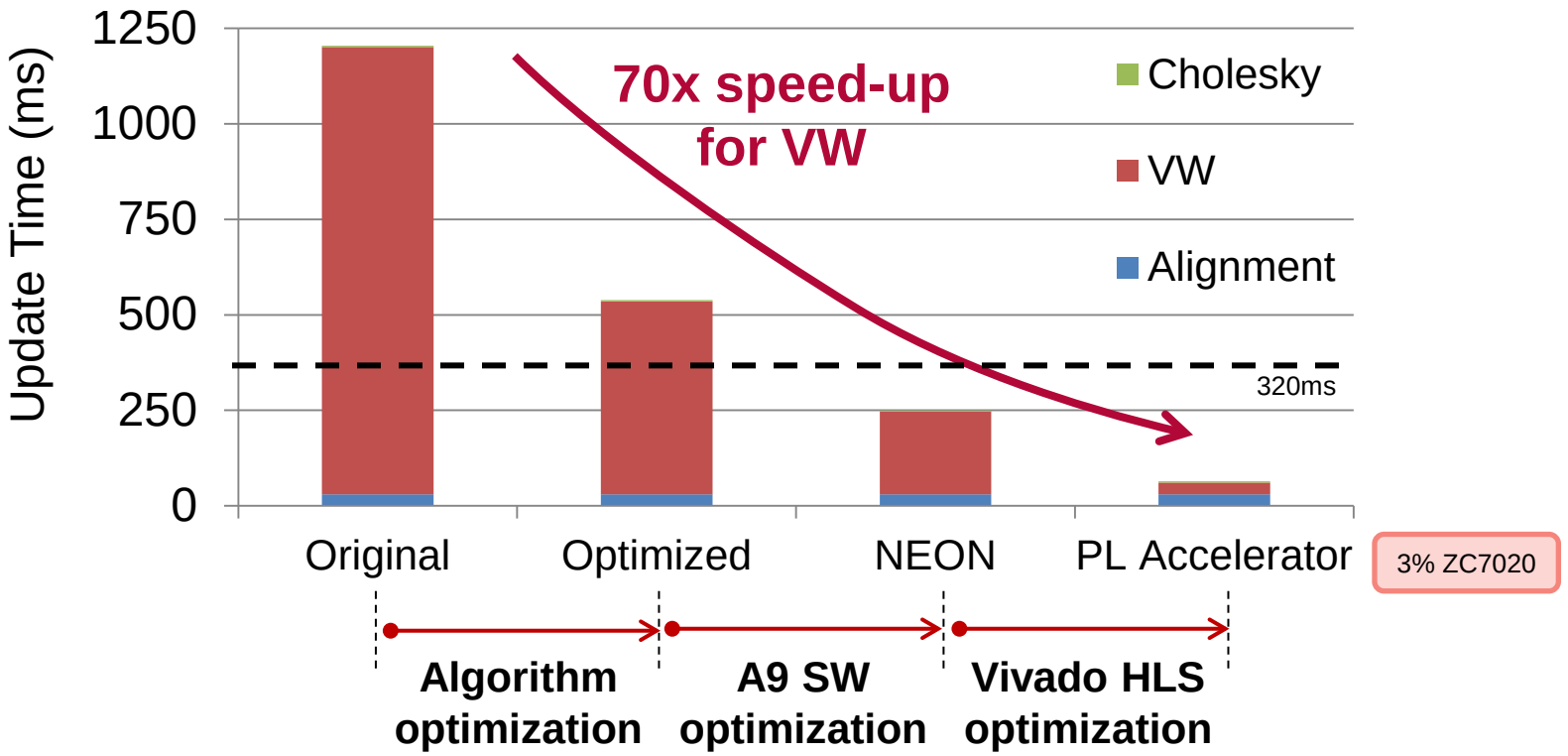
# Programmable Digital Pre-Distortion



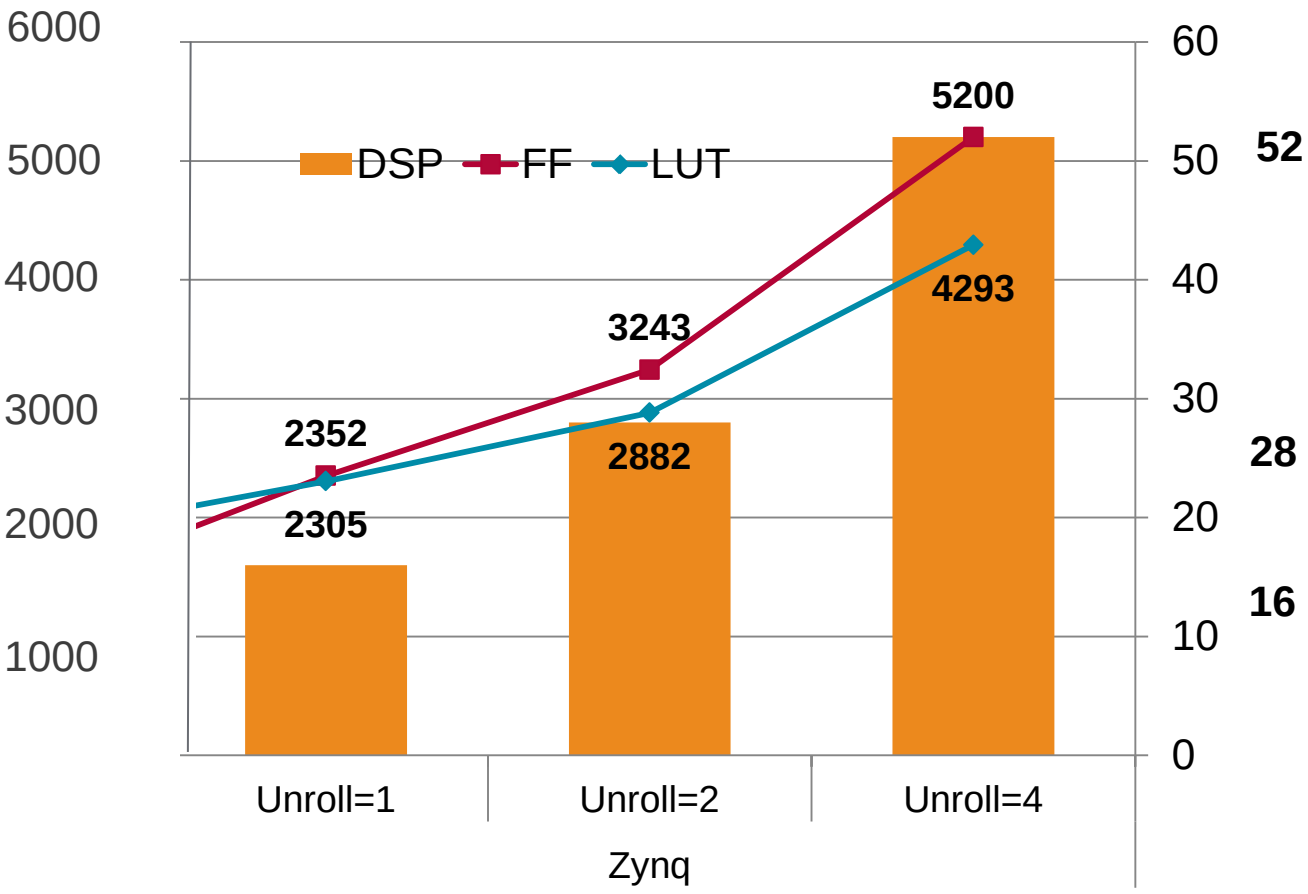

- **DPD negates PA non-linearity**
  - PAs consume massive static power
  - DPD improves PA efficiency by ~35-40%



# HW Acceleration

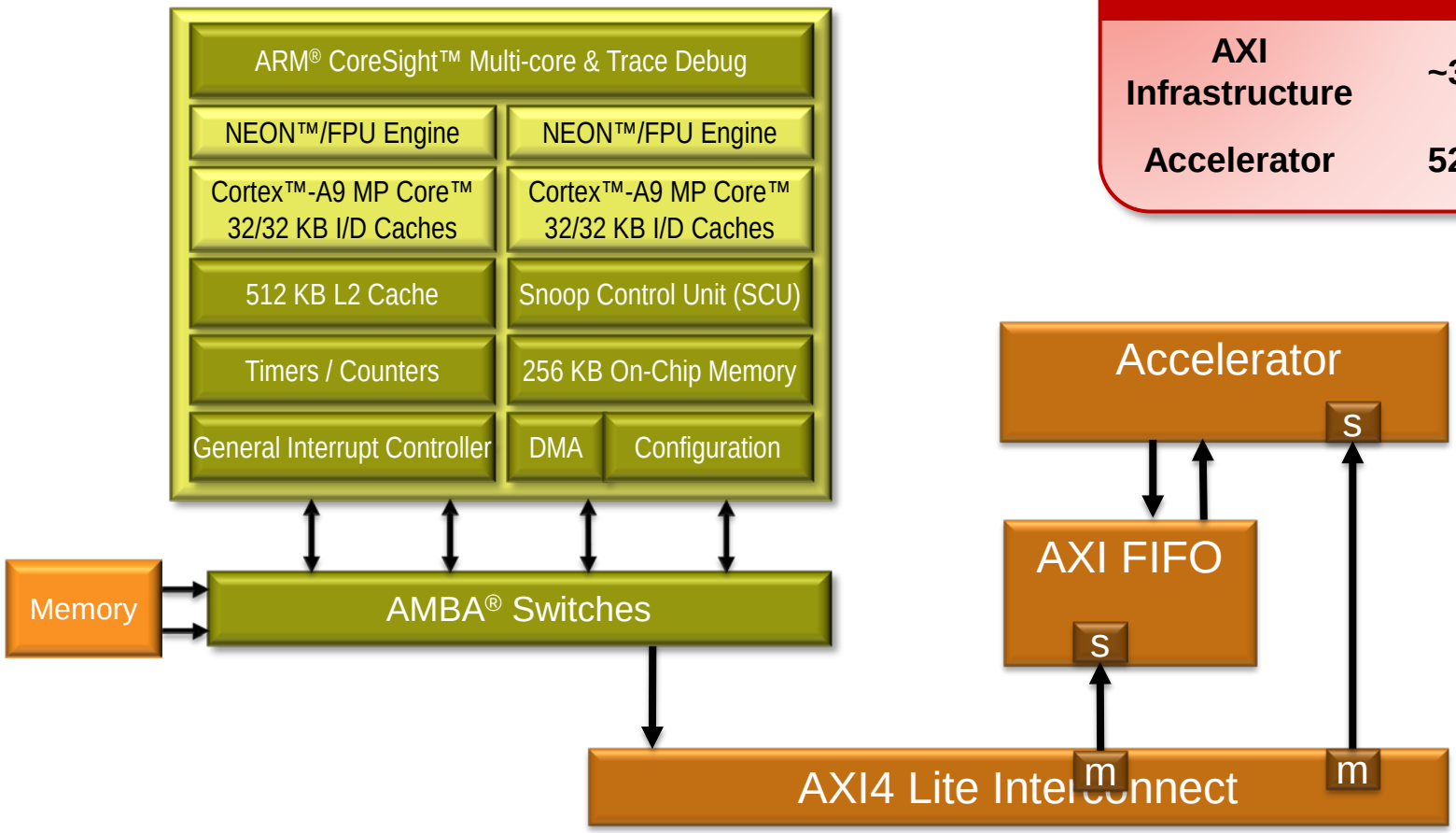


# HW Accelerator Resources



# DPD Architecture Data Movement

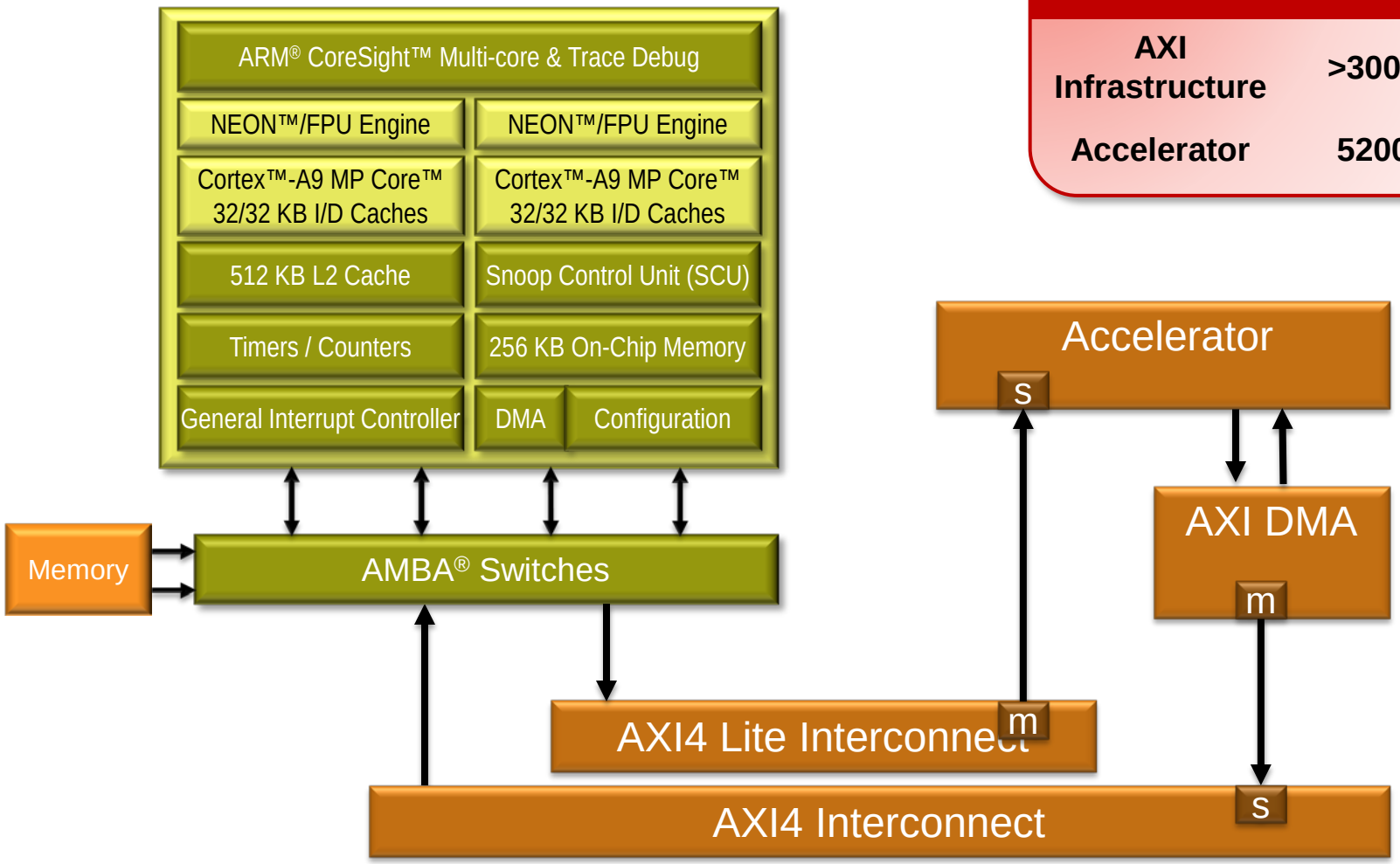
| | FF | LUT |
|---|---|---|
| AXI Infrastructure | ~300 | ~300 |
| Accelerator | 5200 | 4293 |




**Reduced Resources Because of AXILite Infrastructure**

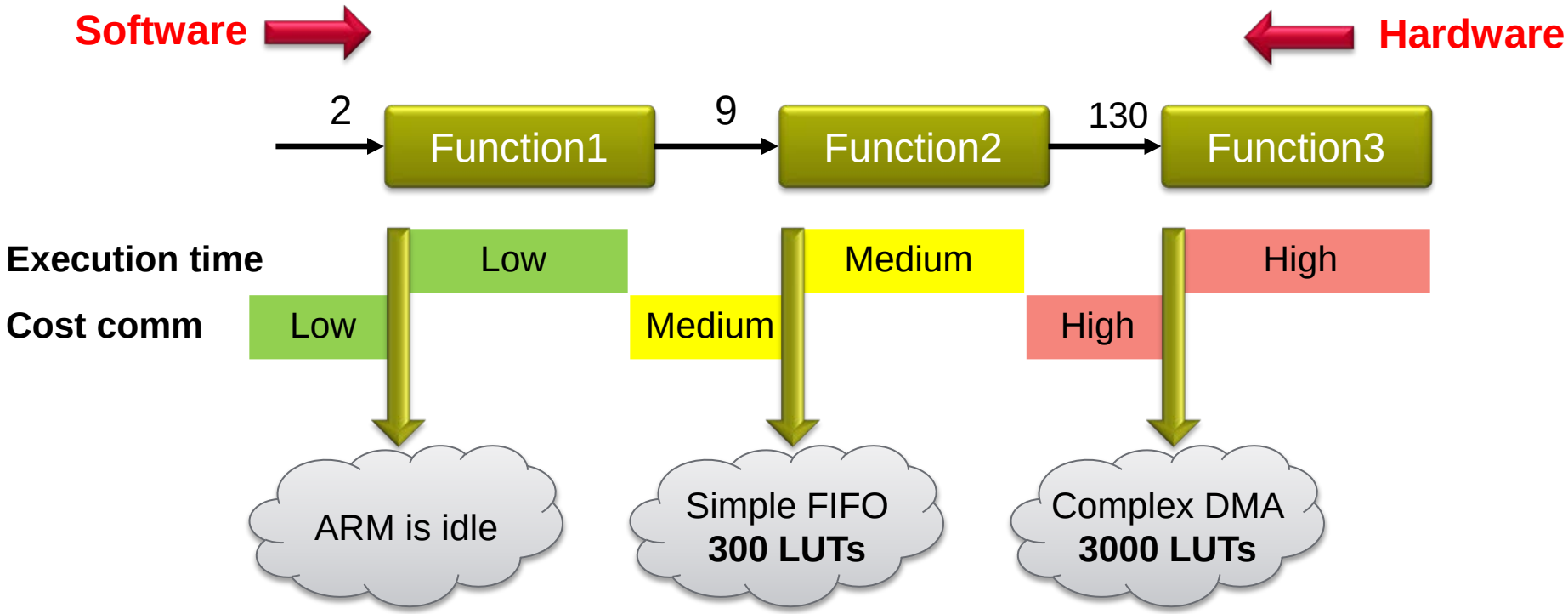
# DPD Architecture Data Movement

| | FF | LUT |
|---|---|---|
| AXI Infrastructure | >3000 | >3000 |
| Accelerator | 5200 | 4293 |




**High Throughput Because of DMA Infrastructure**

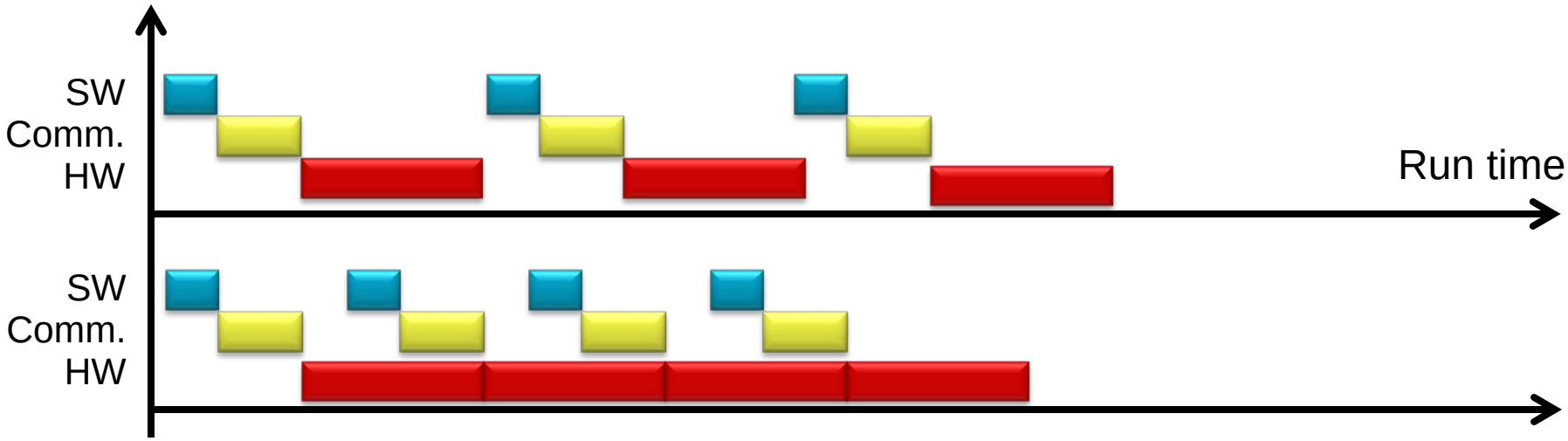
# Hardware/Software Boundary




- Optimal cut point depends on execution times and cost of communication
- Implement different cut points is a time consuming task

**Goal: Maximize Throughput and Reduce Area Resources**

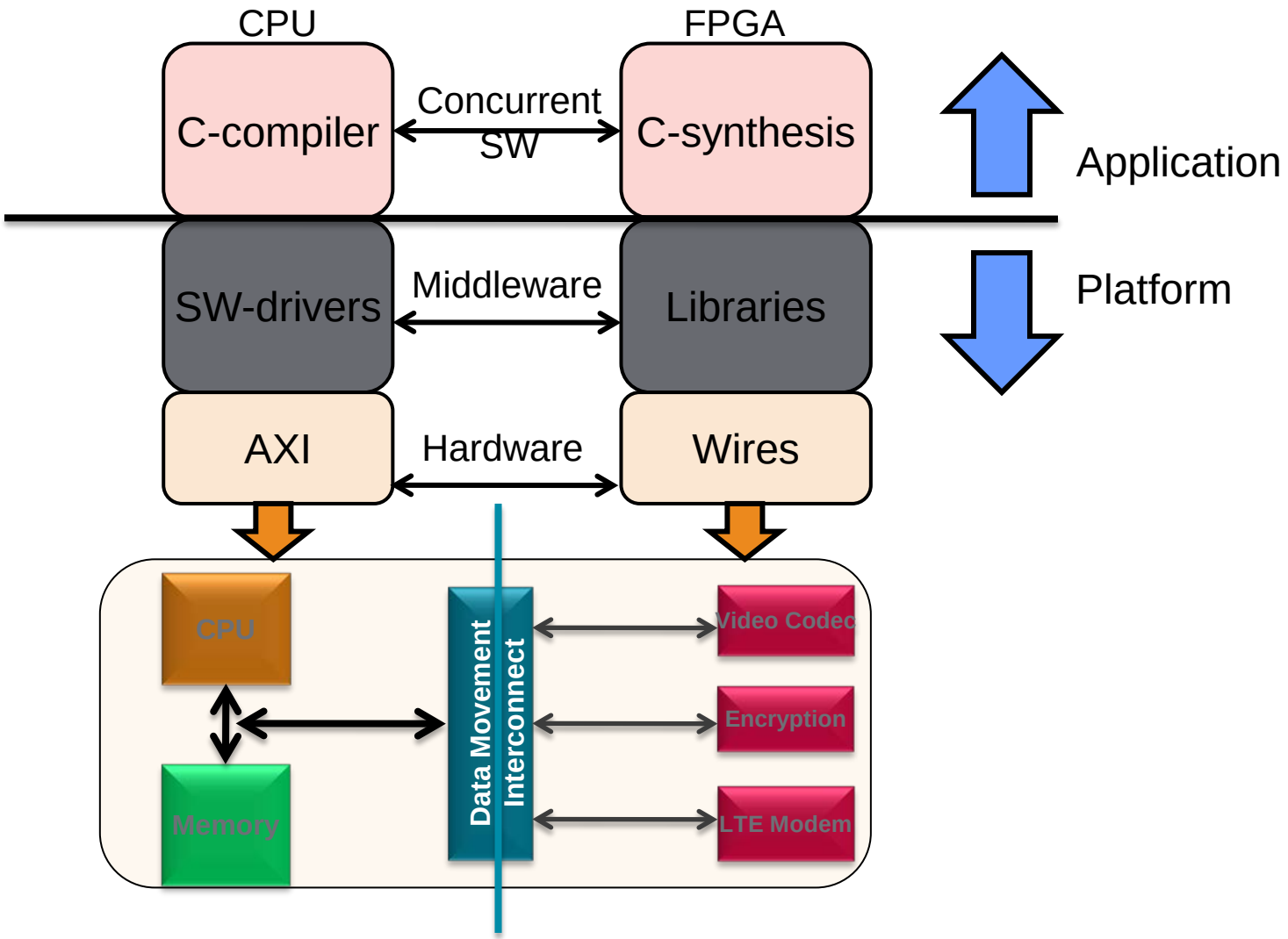
# Software Integration



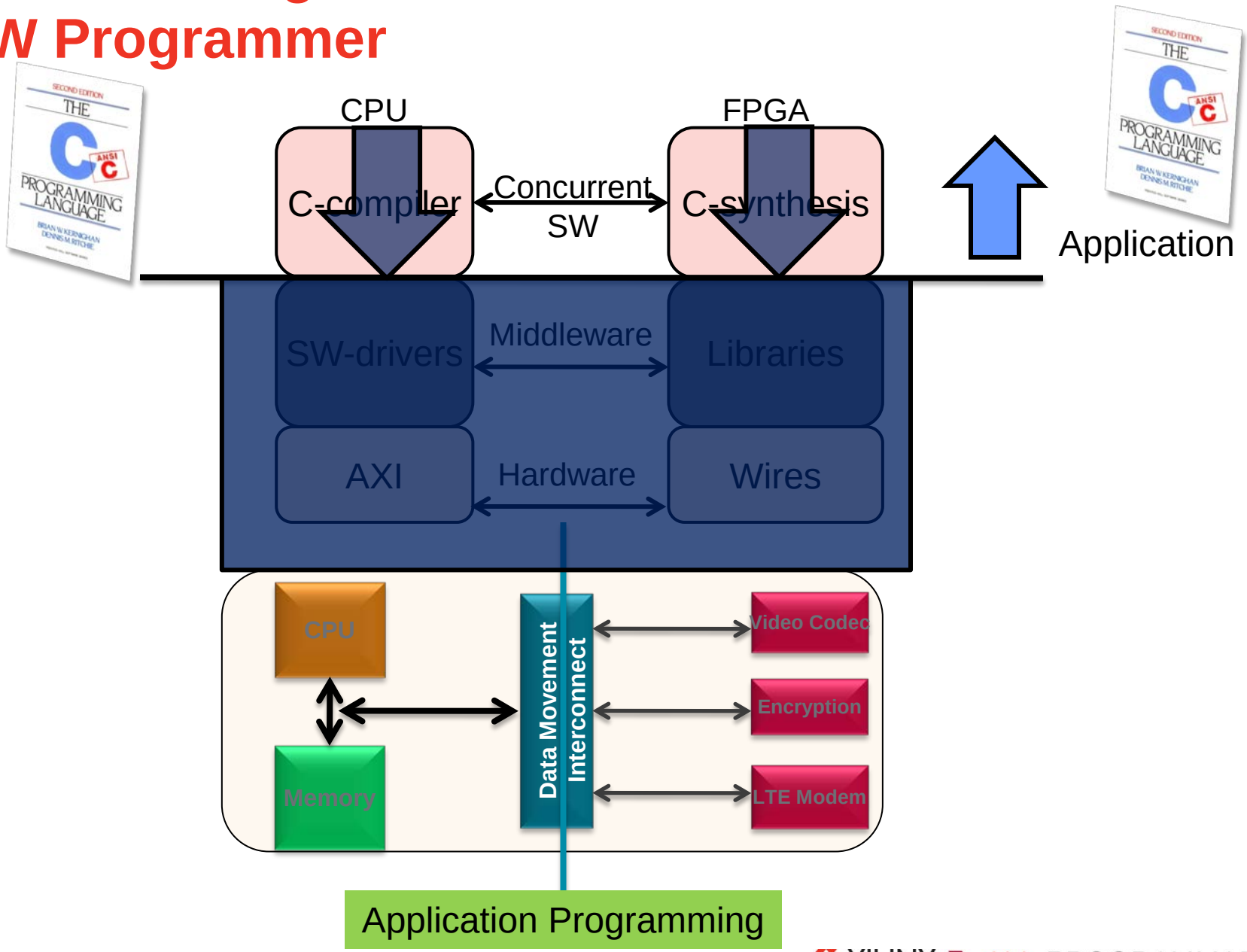

- Accelerator implementation
- Data motion network
- Optimal drivers

**Smart Software Driver is Necessary**

# HW/SW Design Flow

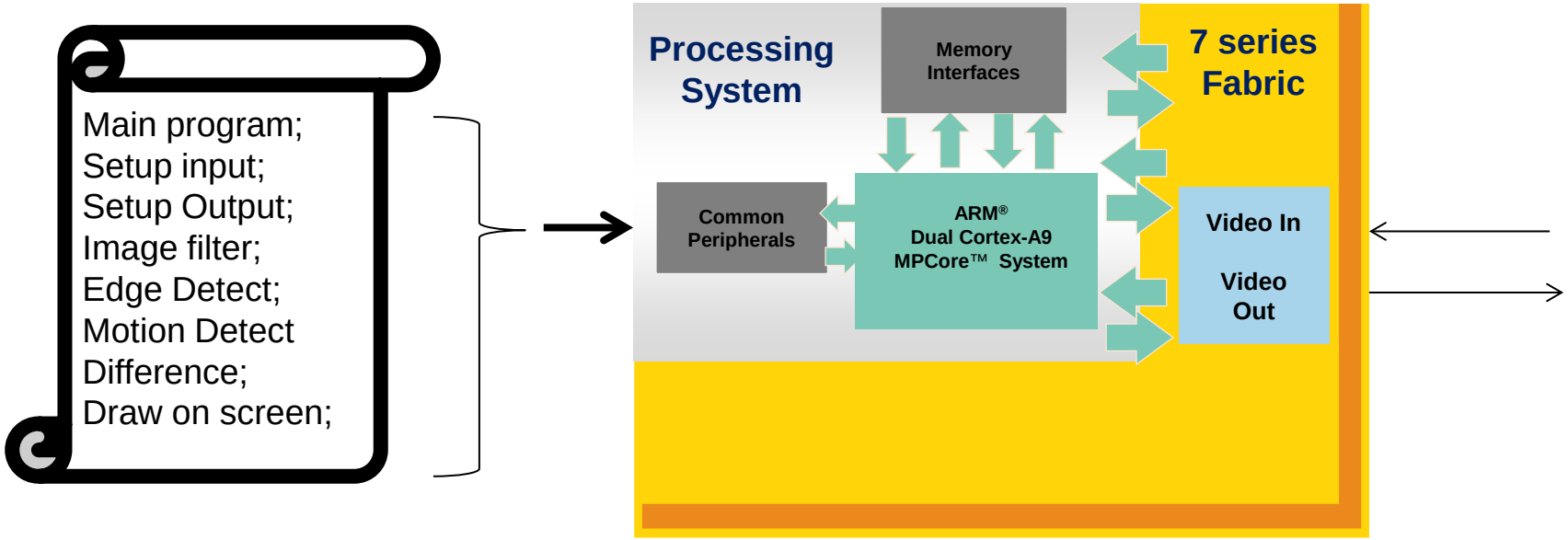


# HW/SW Design Flow: SW Programmer



# Video Acceleration

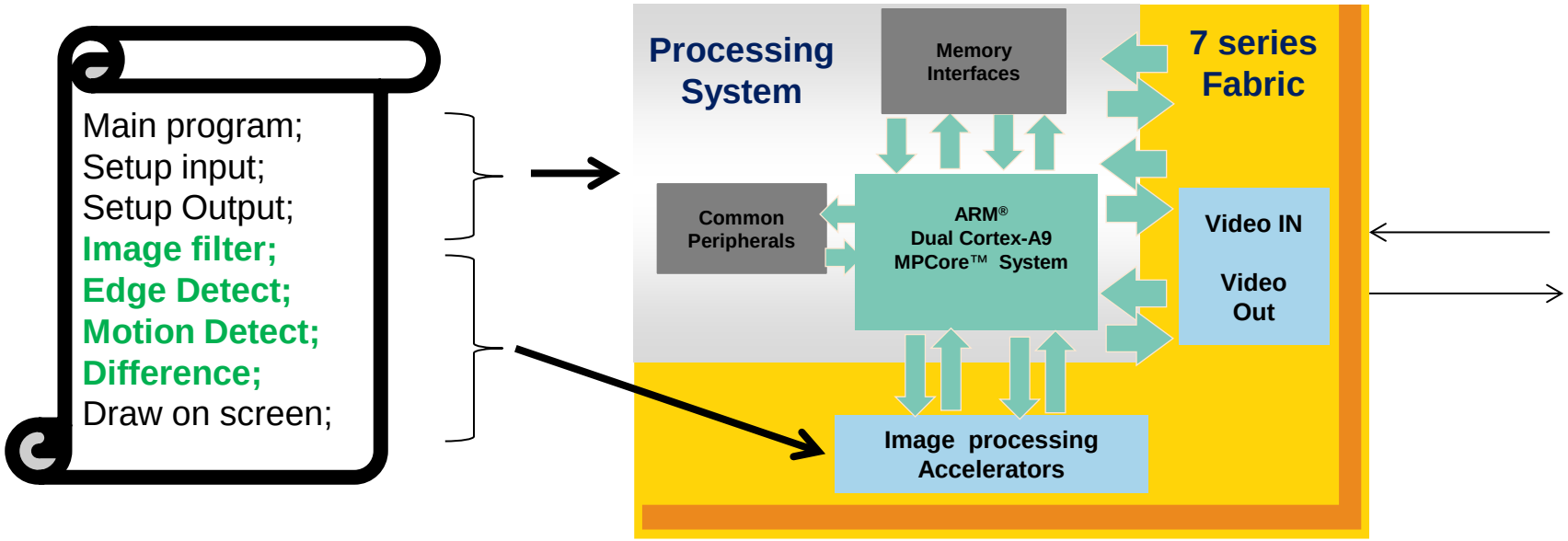
## C/C++ Software Program




1 frame per 13 seconds

# Processor + Fabric Solution on Zynq-7000 AP SoC

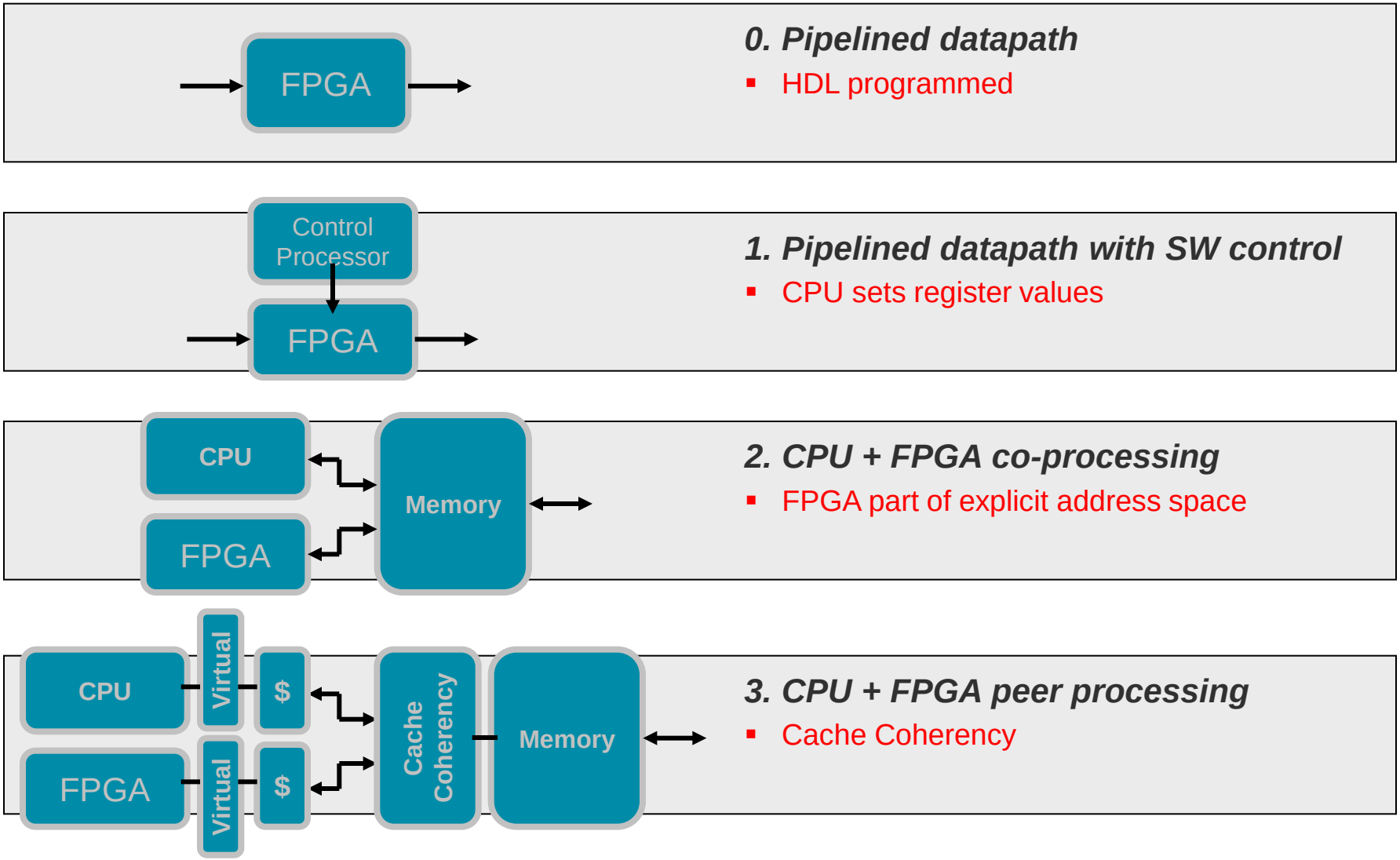
## C/C++ Software Program



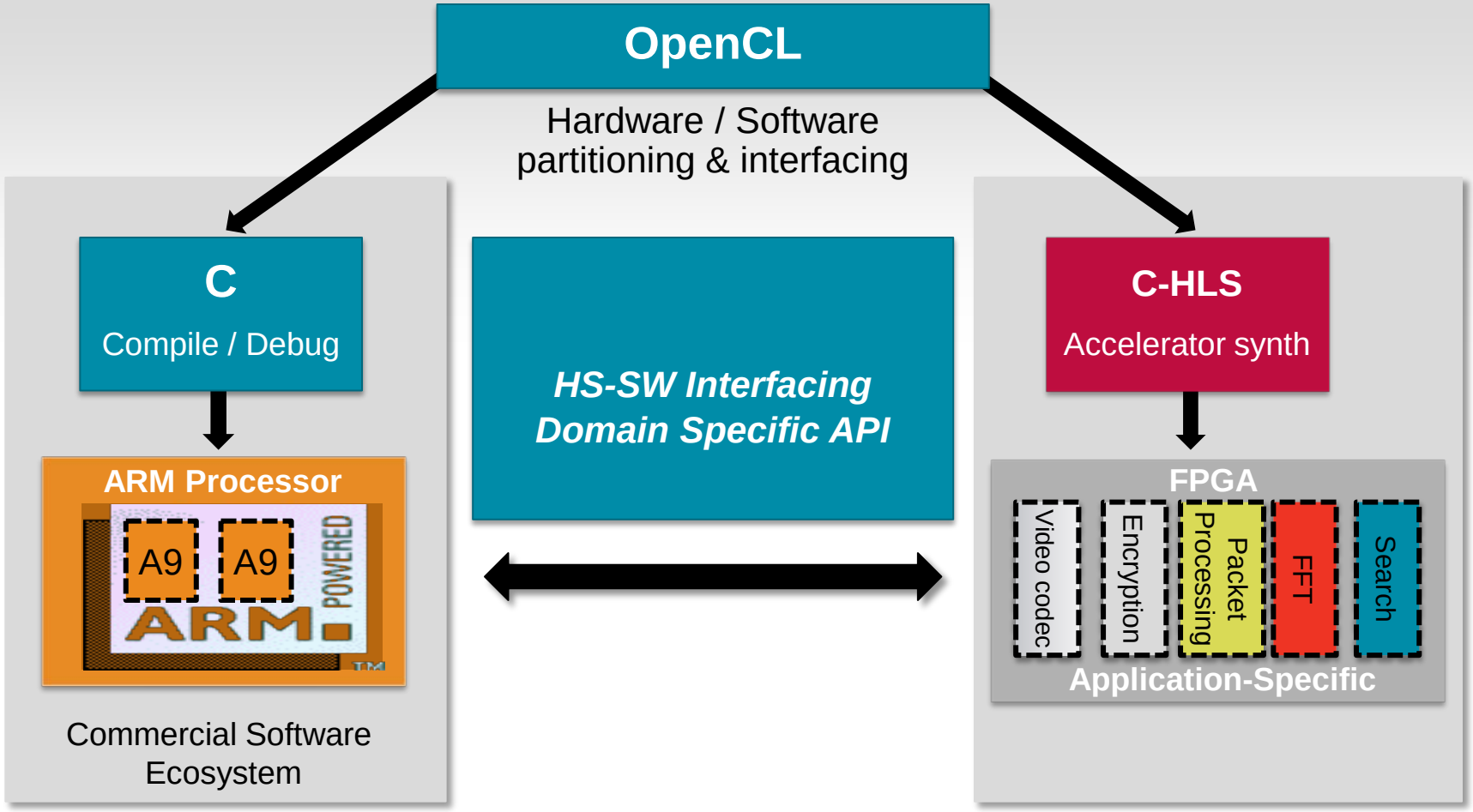

Software video processing functions compiled onto FPGA fabric

60 frames per second, 700x speedup

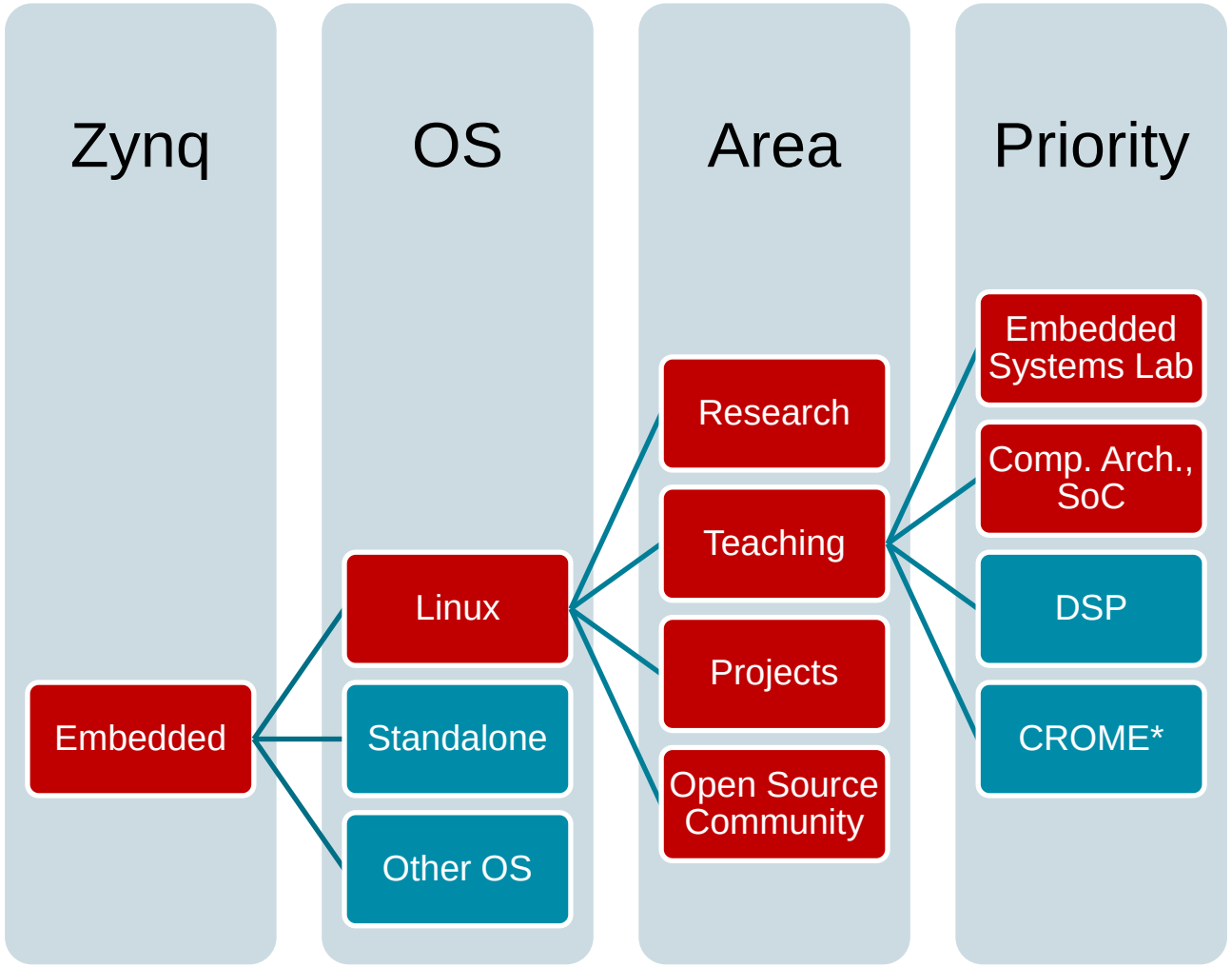
# FPGA/CPU Use Models



# Towards Heterogeneous Multi-core



# Opportunities for SoC Education

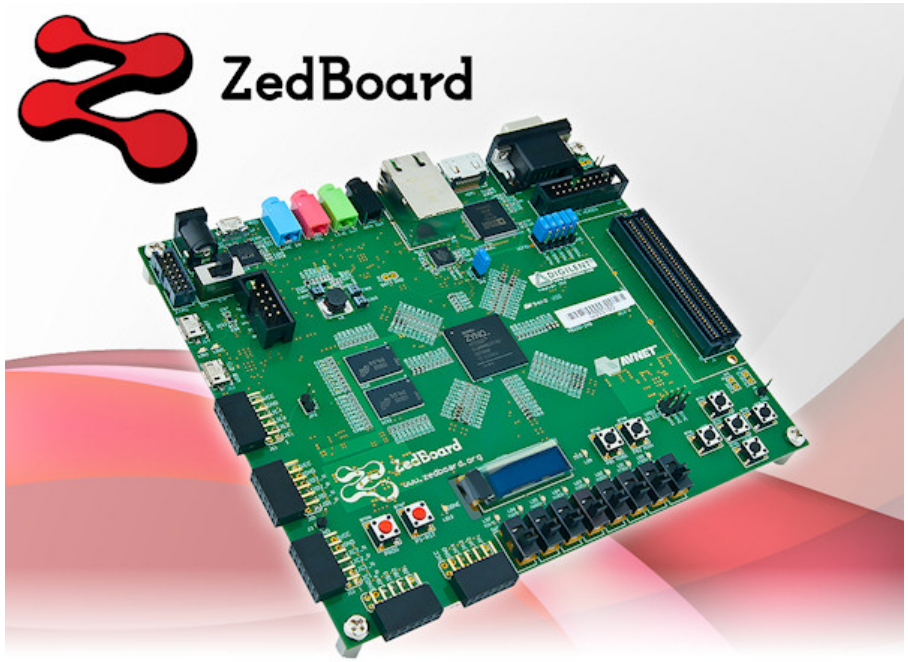



ARM + XILINX

*Controls, RObotics and MEchatronics

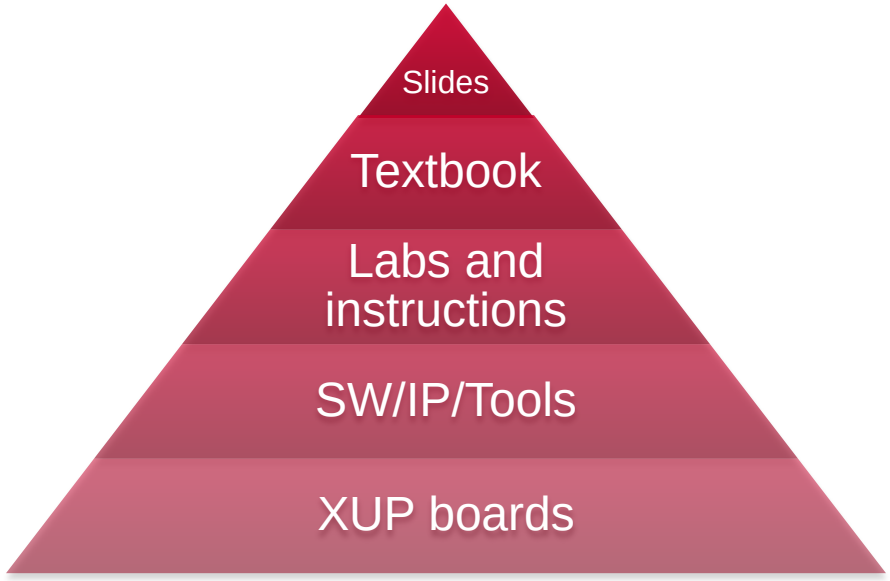
# ZED Board

- **ZED Board**
  - Zynq Evaluation and Development Kit
  - Low cost Zynq based community board  (XC7Z020)
  - Partnership between Avnet, Digilent, Xilinx
  - Digilent will fulfill academic market for Xilinx University Program
- **ZEDboard.org**
- **Open source SW and IP**
  - Linux
  - Eclipse based IDE
  - Vivado HLS: C to FPGA
  - Reference designs

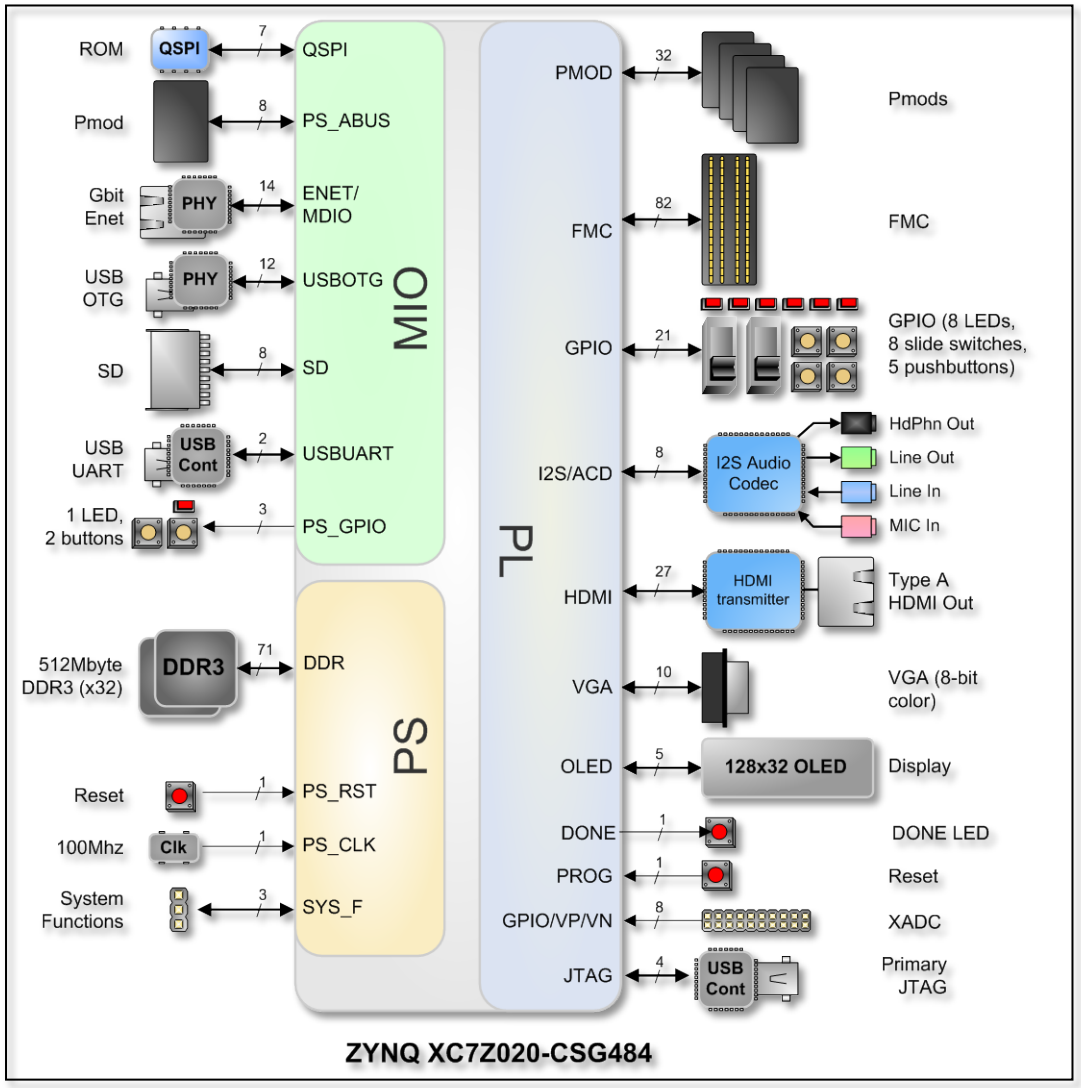


# Target Teaching Platform (TTP)

- **Turn key solution for teaching labs on**
  - Digital Logic
  - Digital Signal Processing
  - Embedded System Design
  - Principle of Microcomputers
  - Embedded Operating Systems
- **Xilinx updates the kit as and when required**



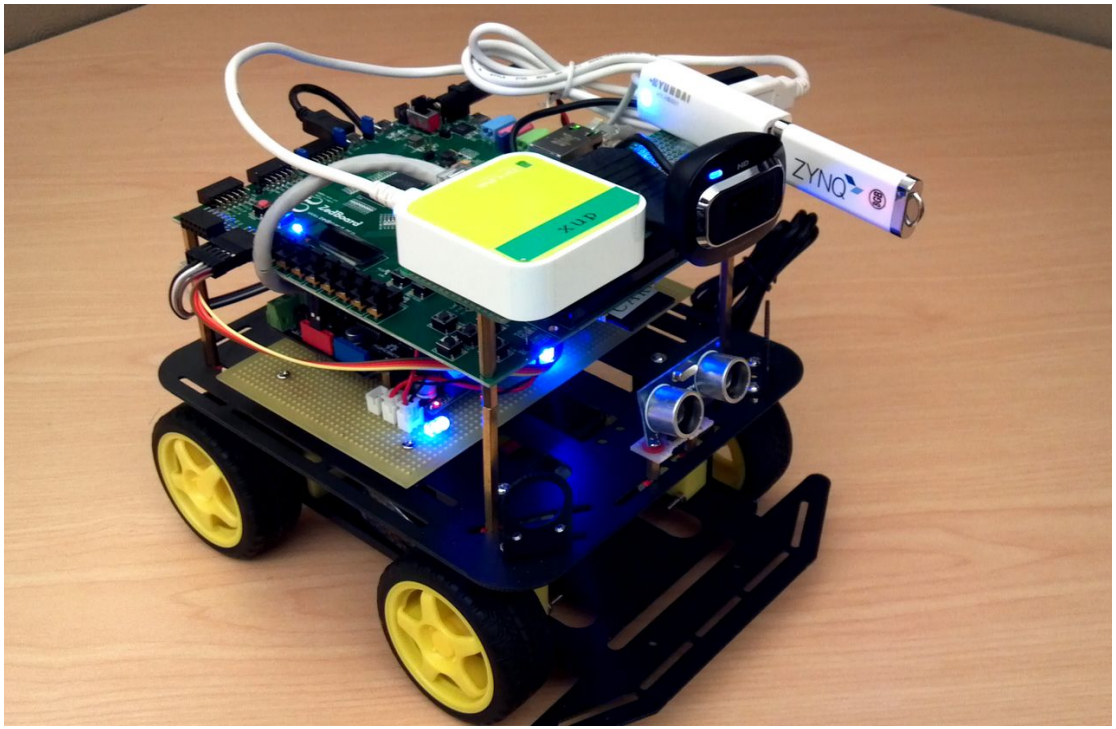

# ZED Block Diagram & Features



# Targeted Teaching Platform (TTP)

Initial version of the Smart Car TTP:

ZynqBot– Mark1




Controlled wirelessly
by Android cell phone app

# Conclusions

- Modern FPGA is an All Programmable SoC
- Software Centric Design Flow
- Unmatched Performance/Watt
- Towards Heterogeneous Multi-Core
- Targeted Teaching Platform