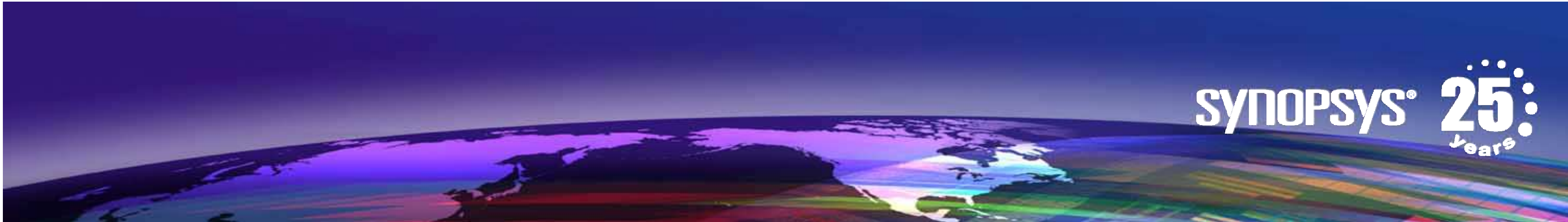


The Short-, Medium- and Long-term Path to the 3D Ecosystem

An EDA Vendor Perspective

EDPS 2012, Monterey, CA
April 6th 2012

Steve Smith
Senior Director
3D-IC Strategy and Marketing, Synopsys

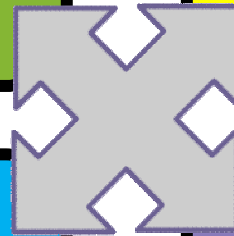
Near/Mid-Term Needs

Manufacturing & Test

- Thermo-mechanical-stress & reliability analysis
- DFM rules (TSV/microbumps)
- Foundry interposer DRM/PDK
- Microbump probing

System-level

- ESL power & thermal modeling/budgeting
- HW/SW co-design



IP

- Memory IP incl. BIST & repair
- SERDES

Implementation & Signoff

- Auto-routed interposer
- Parasitic extraction
- SI/inductance analysis
- Multi-die timing analysis
- Microbump alignment checks
- Connectivity checks
- Multi-technology SPICE

SYNOPSYS® 25 years

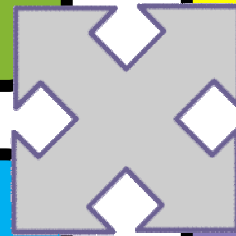
Long-Term Needs

Manufacturing & Test

- 3D Test standards
- KGD methods
- Packaging

System-level

- Architectural exploration
- Auto-partitioning
- Virtual prototyping



IP

- Die-level IP modeling within 3D environment → SI, noise isolation, M/S integration, etc.

Implementation & Signoff

- Multi-die CTS
- Optimization for PPA
- Multi-die variation
- Thermal planning
- Multi-technology power spec.

SYNOPSYS® 25 years

3D-IC @ Synopsys

Manufacturing & Test

Sentaurus Interconnect TCAD
- Thermo-mechanical stress & reliability analysis
- Electrical variation

DFTMAX/TetraMAX
- TSV connectivity checking
- IEEE 1149.1, 1500, P1838

System-level

Platform Architect
- SoC architecture performance analysis & optimization

Virtualizer
- Virtual prototype development

HAPS
- FPGA-based prototyping

Sort/Hard Die-Level IP

DesignWare
- Interface IP (USB, PCIe, DDR, SATA, HDMI, MIPI)
- Memory IP (SRAM, ROM,…)

STAR Memory System
- Memory BIST & Self Repair

Implementation & Signoff

IC Compiler/Custom Designer
- Physical implementation

StarRC/HSPICE
- Extraction / Multi-technology sim.

IC Validator/PrimeTime
- DRC/LVS, STA signoff