The Short, Medium and Long-Term Path to the 3D Ecosystem

Panel Discussion at EDPS

A Monolithic 3D-IC Perspective

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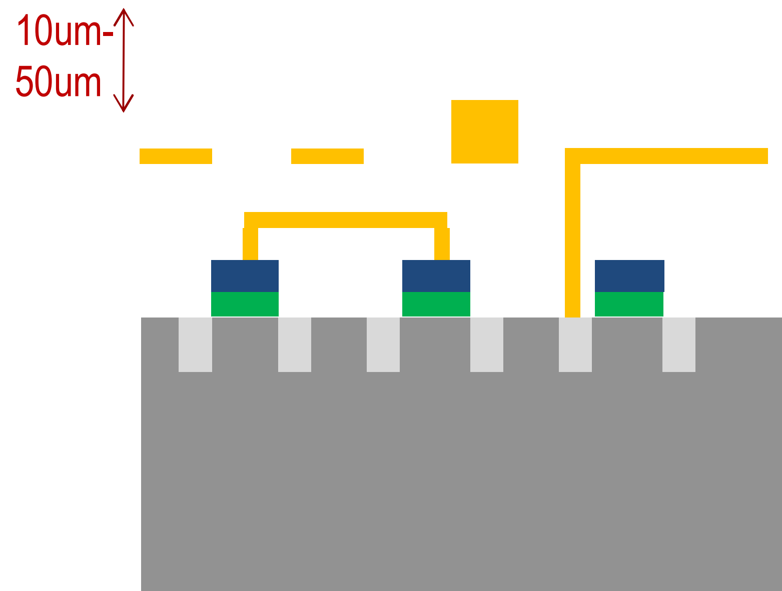
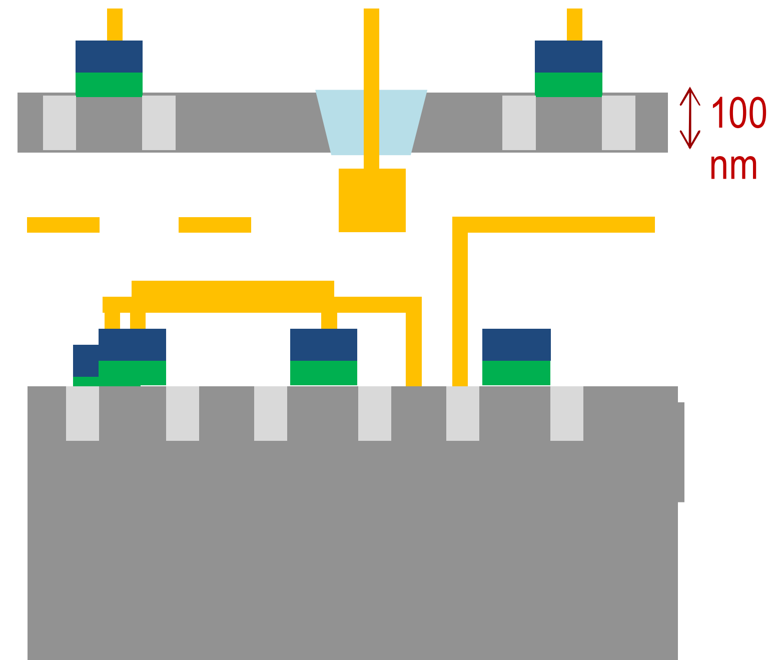
Two Types of 3D Technology

3D-TSV	Monolithic 3D
Transistors made on separate wafer @ high temperature, then thin + align + bond	Transistors made monolithically atop wiring (@ sub-400ºC for logic)



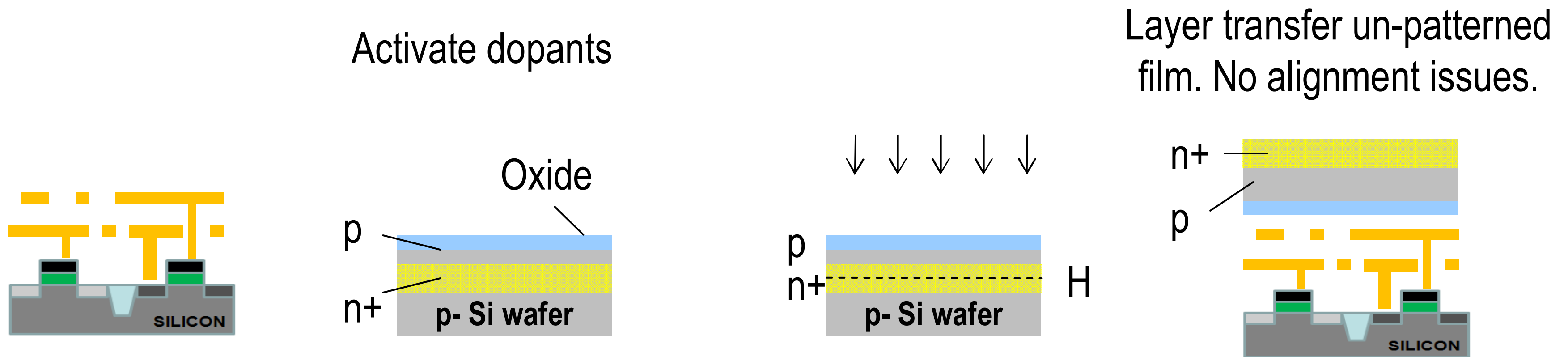


TSV pitch > 1*um**

TSV pitch ~ 50-100*nm*

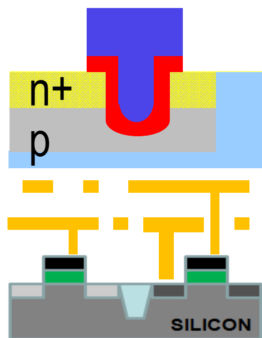
* [Reference: P. Franzon: Tutorial at IEEE 3D-IC Conference 2011]

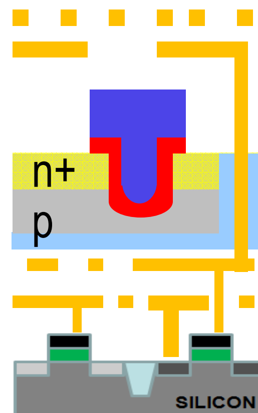
A Process Flow for Monolithic 3D: Recessed Channel Transistors with Activation before Layer Transfer



Well-aligned sub-400C RCATs Si thickness < 100nm

Min. feature size TSVs since low Si thickness, no misalignment issues





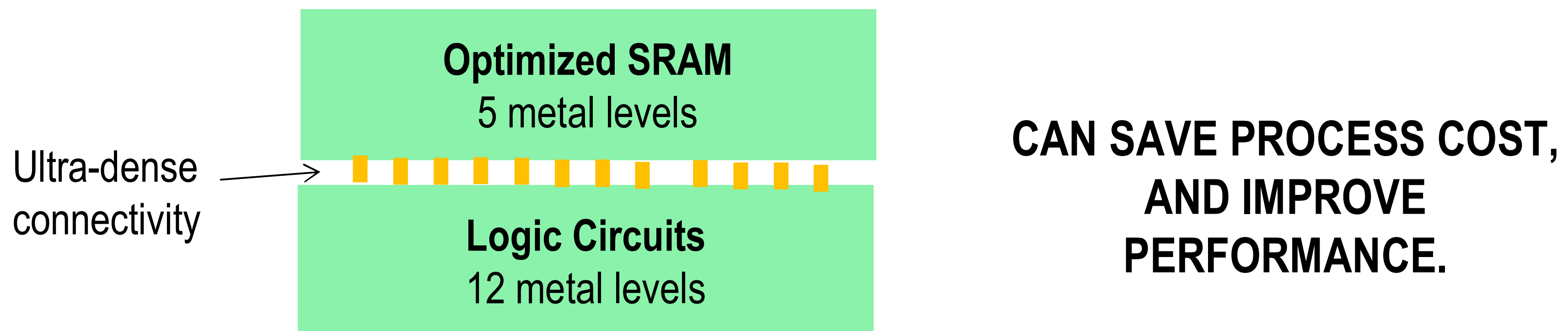
- **Steps atop Cu/low k < 400°C**
- **RCATs used in production DRAM since the 90nm node → Adoption easier**

[D. C. Sekar, Z.Or-Bach, “Monolithic 3D-ICs with Single Crystal Silicon Layers”, Proc. IEEE 3DIC Conference 2011 (Invited)]

SRAM-Logic Stacking

- **SRAM requirements different from logic today.**

  Different number of metal levels, V_t, L_{eff}...
- **Ultra-dense vertical connectivity needed, esp. for small size SRAMs within a logic core → good fit for Monolithic 3D**



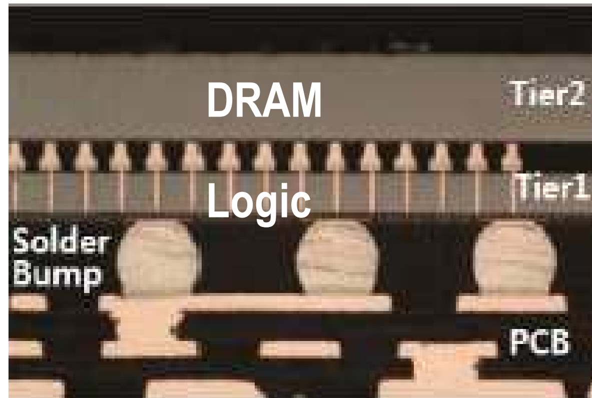
CAN SAVE PROCESS COST, AND IMPROVE PERFORMANCE.

EDA need: Tools to partition designs and stack the SRAM

Ref.: [D. Sekar, PhD Thesis, Georgia Tech]

Logic-Logic Stacking with High TSV Density

Today
"Pseudo-3D" EDA Tools



- Modify existing 2D tools slightly
- TSVs in whitespace or modify existing layout slightly for TSVs to stacked layer
- OK for today's 5um TSVs (low density)

Needed for Monolithic 3D
"Native-3D" EDA Tools

•3D routing, placement, floorplanning tools that work for TSVs close to min. feature size

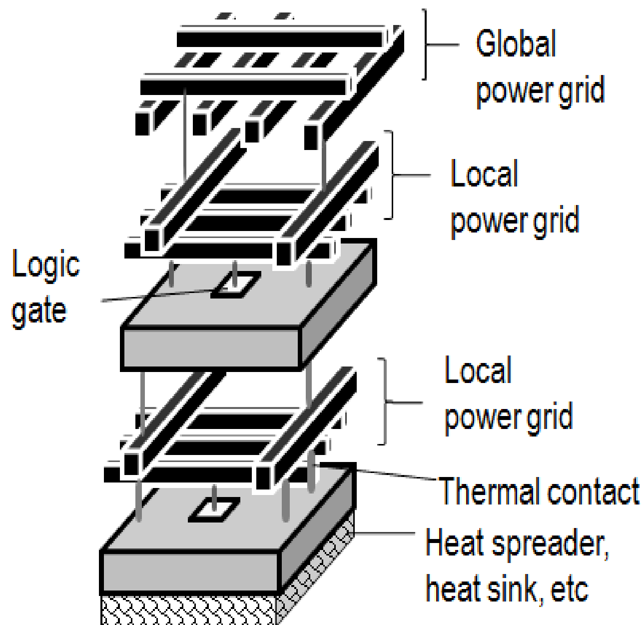
•Support for both block-level and gate-level partitioning

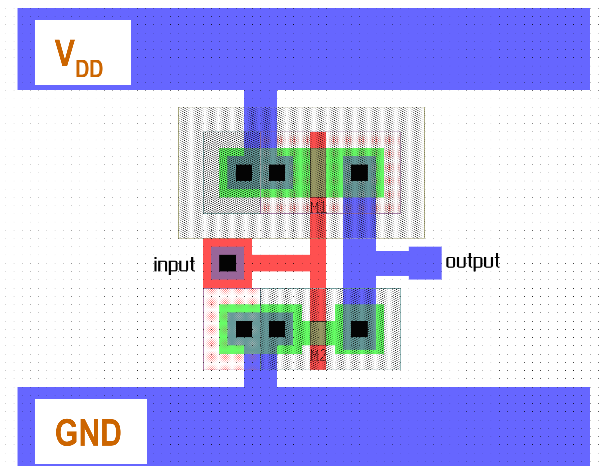
Thermal-Aware Place-and-Route Power Distribution Network Design = Good heat removal for monolithic 3D

- Most logic gates have V_{DD} and GND contacts

  Low (thermal) resistance power grids → low temp. drop between heat sink and stacked logic gate

- Promising simulation results

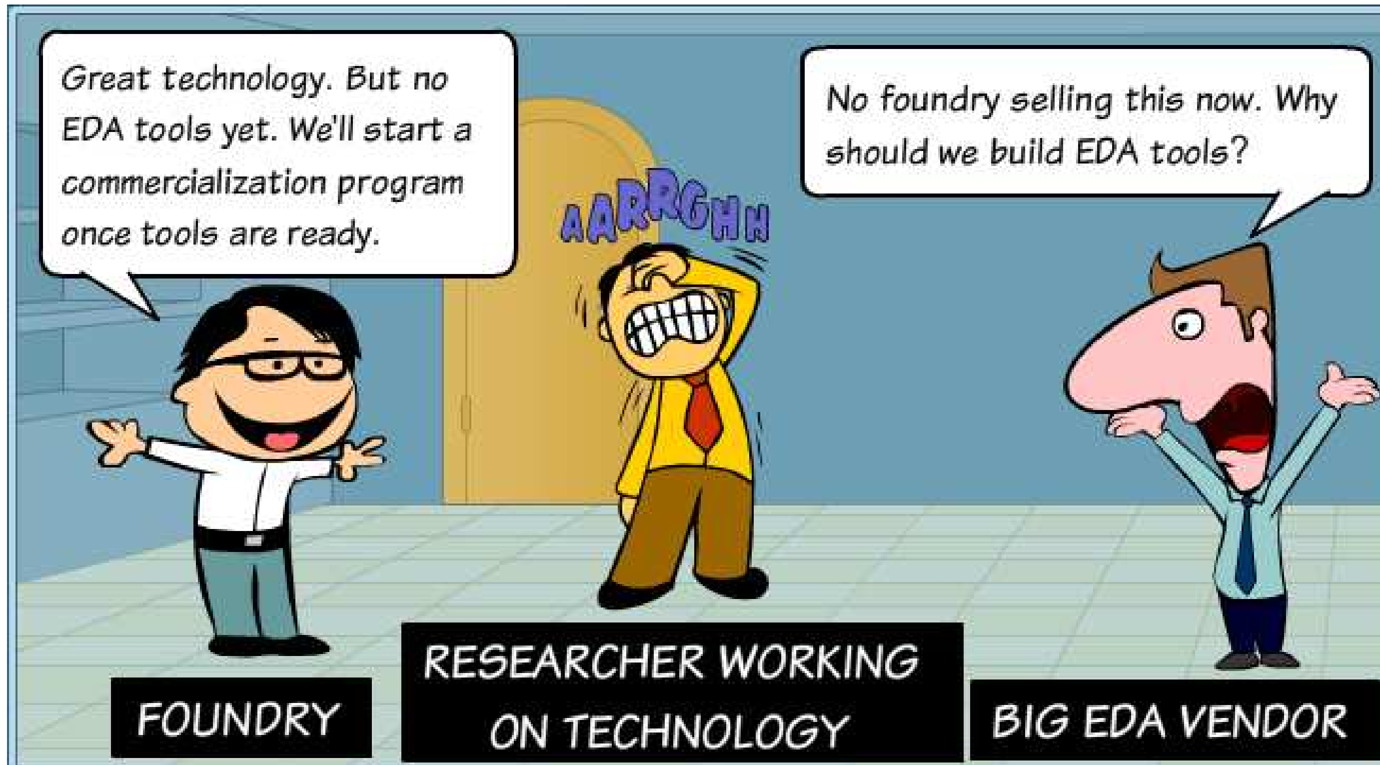




EDA need:
Integrate power distribution design with (thermal-aware) place-and-route for monolithic 3D

Ref.: [D. Sekar, Z. Or-Bach, US Patent Application #13/041,405]

How will monolithic 3D technology tackle this familiar problem?



<u>Suggestion to the EDA community</u>:

EDA tools for logic-logic stacking starting to be developed for um-scale TSVs.

Make sure your algorithms are scalable to nm-scale TSVs… they may happen sooner than you think!