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The Short-, Medium- and Long-term Path to the 3D Ecosystem

*There’s no such thing as a free lunch !!! **

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EDPS 2012, April 5 & 6, Monterey, CA

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* SOURCE: Milton Freeman, 1975

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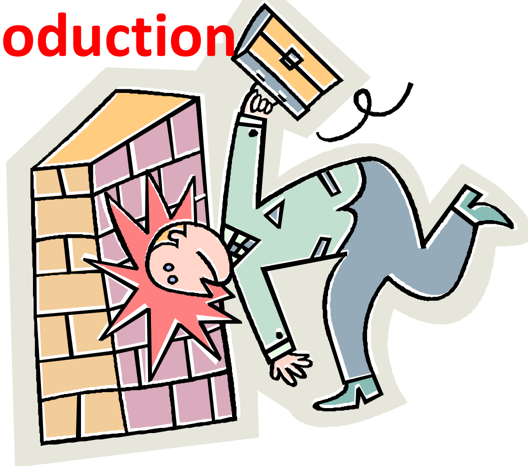
Short-term: **Memory Wall**

2012 2013 2014 2015 2016 2017 2018 2019 2020

Production



MARKET: "Memory Wall" limits latency and bandwidth between Logic and Memory chips

Memory vendors have already developed high-speed (Hybrid Memory Cubes) as well as low-power (Wide I/O) memory stacks

EDA needs to address **data exchange formats** and, e.g.:

- **Modeling** of new materials & equipment capabilities
- Functionality, **STA, PI and SI** across die, package & PCB
- **Design for** wafer-, partial stack- & final product **test**
- Thermal/mechanical die-pkg stress impact on **reliability**
- **Bottoms-up** planning & design tools for lowest unit **cost**

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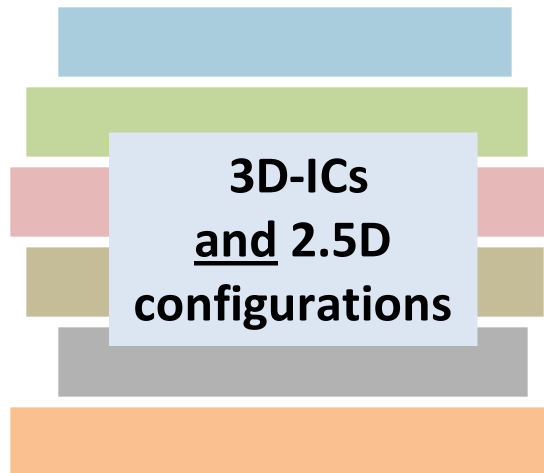
Medium-term: **Heterogeneity**

2012 2013 2014 **2015 2016 2017** 2018 2019 2020

Production



MARKET:

Logic & Memory

& Analog & FPGA

&: RF, HV, MEMS,

Fiber optics,…

MARKET:

14nm logic & 25nm Flash

& 180nm for analog,…

CMOS & SOI & GaAs

III-V channels on CMOS

In addition to the previous list, **EDA** needs to address, e.g.:

- **Models** of legacy **and 3rd party** (mixed-signal) **die-level IP**
- Methods for **parametric-testing during** wafer **probe**
- Tools for **temp., noise, magnetic,..** die-2-die interference
- **Design-for-redundancy & self-repair, …** to lower **cost**

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Long-term: **Complexity**

2012 2013 2014 2015 2016 2017 **2018 2019 2020**

Production

MARKET:

Billions of high-complexity MIDs sold every year.

Intelligent man-machine interfaces need logic,
memory, analog, RF, MEMS, image sensors,…

Terabytes of internet traffic/sec need routers

Petabytes of data stored in the cloud need SSDs

In addition to previous lists, **EDA** needs to address, e.g.:

- User-friendly, **top-down system-level** design challenges
- Methods for Hardware- & Software **co-design/verification**
- Tools for **nano-wires**, **self-assembly, monolithic 3D-ICs**
- Die-level IP libraries & "HL composition tools" to lower **cost**

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Is a bridge from EDA suppliers to semiconductor designers & -manufacturers

10 years old and always busy, because:

- Vertical disintegration makes changes more difficult (vs IDM)
- Earlier EDA support increases ROI for new manufacturing technologies and lowers NRE and unit cost for customers
  - E.g.: TSMC reference flow, PrimeTime sign-off wave, ASIC & FPGA design kits,...
- User education accelerates acceptance of new technologies
- Eco-system building minimizes risks and time-to-market
- De-facto and open standards help IC design & manufacturing
- 2,5/3D technology is a **major paradigm shift** and offers us many opportunities. However, it needs lots of coordination, communication and standards to be agreed upon across the entire ecosystem to become cost-effective and widely used!