# What Does it Take to Build a Complete Test Flow for 3-D IC?

Brion Keller, Bassilios Petrakis, Cadence
Thanks to : Sandeep Goel, TSMC
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# Acknowledgements


- TSMC
  - Ashok Mehta
- imec
  - Erik Jan Marinissen
- Cadence
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  - Vivek Chickermane,
  - Subhasish Mukherjee

# Purpose

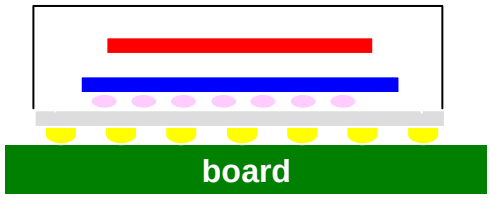
- 3D stacking of ICs is a hot DFT topic
  - Using TSVs as die interconnects has many advantages
- 3D DFT is needed to do modular testing of
  - Die internal logic
  - Die interconnects
- Presentation focuses on
  - Modular testing techniques of 3D stacking ICs with TSV
  - A tool flow for automatic insertion of 3D wrappers
  - Method can be extended to other interconnect types (e.g., interposers)

# Presentation outline

- Introduction
- 3D-DFT requirements
- 3D-DfT architecture
- 3D wrapper generation flow
- Results
- Conclusions

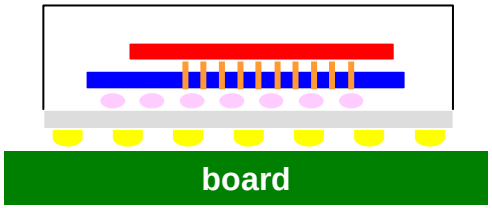
# 1. introduction – Through Silicon Vias (TSVs)

- 3D chip stacking with wire-bonds
  - Heterogeneous technologies
  - Dense integration, small footprint



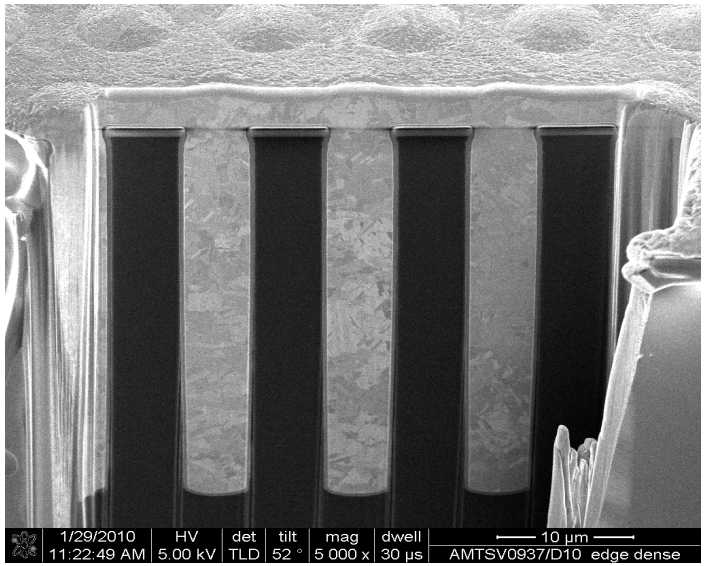

System-in-Package (SiP)

- Through-Silicon Vias
  Metal vias that provide interconnects from front-side to back-side through silicon substrate




TSV-Based 3D-SIC

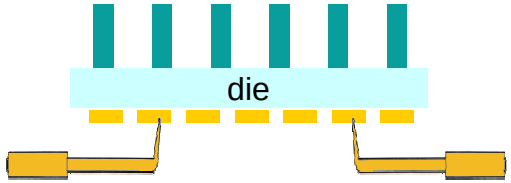
- TSV benefits
  - Even denser integration
  - High density, low capacitance
  - Increased bandwidth
  - Increased performance
  - Lower power dissipation
  - Lower manufacturing cost?



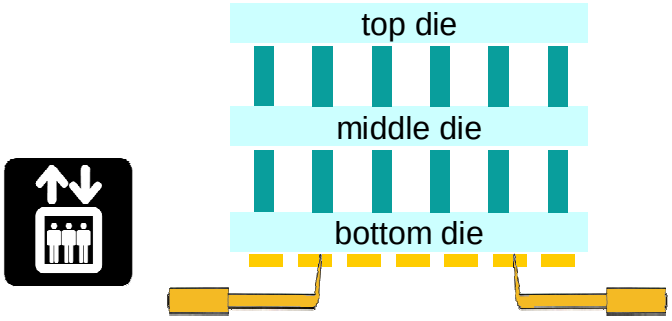
# 2. 3D-DFT requirements

## Test access distinctly different

- Pre-Bond Test
  - Focus on die-internal circuitry
  - Original thick or thinned-down wafer
  - Probe access at DUT
  - Probe on micro-bumps or dedicated pads

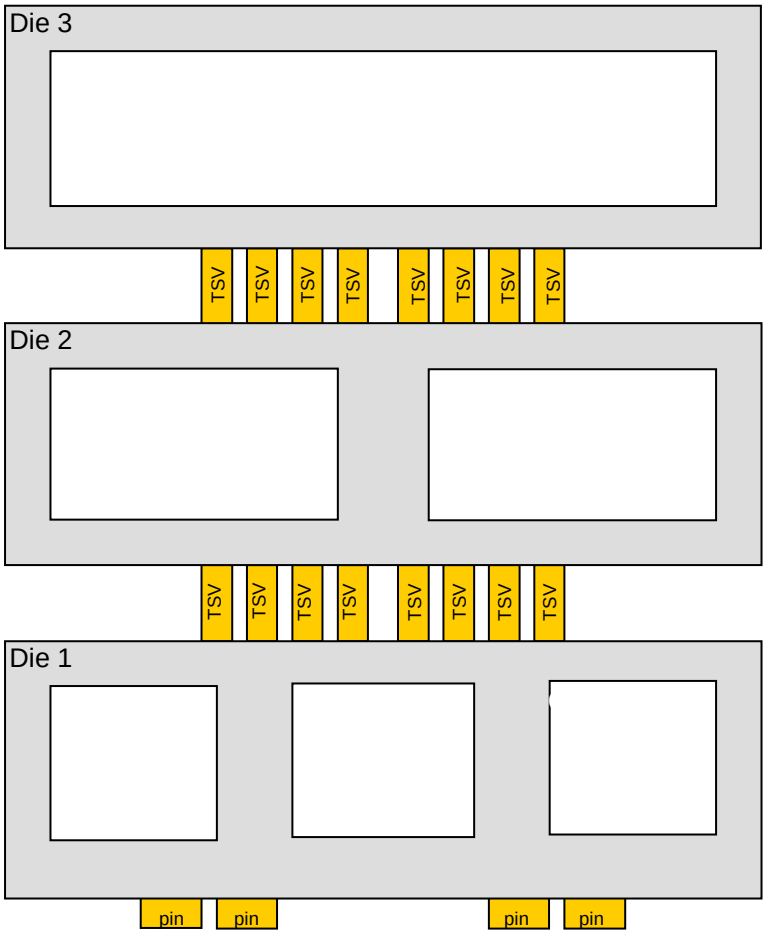



- Mid-Bond / Post-Bond / Final Tests
  - Focus on interconnects and die-internal circuitry
  - Test access (probe or socket) at bottom die
  - Require DfT to propagate test stimuli/responses up/down through stack
  - Requirements
    - Modular test: core, die, interconnect
    - TestTurn: test up till this die
    - TestElevator: test higher-up die



# 3. 3D-DFT architecture

- Example functional design
- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins



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# 3. 3D-DFT architecture

- Example functional design
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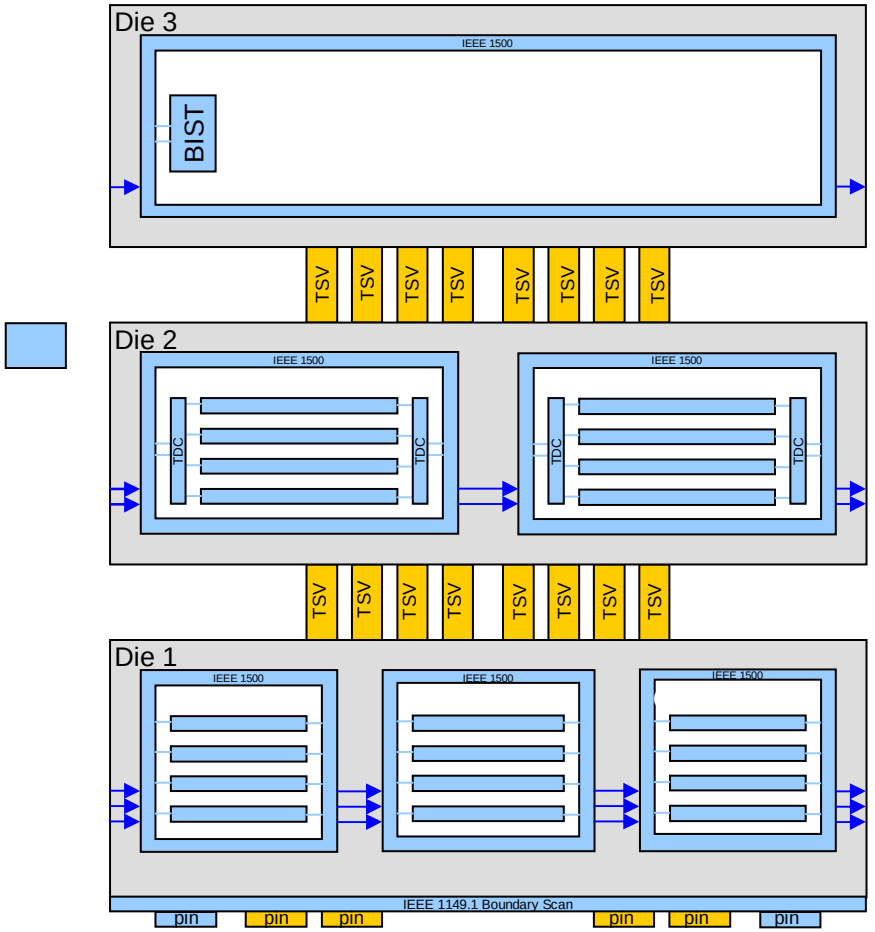
- Example existing design for test
  - Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMS
  - Stack product: IEEE std 1149.1



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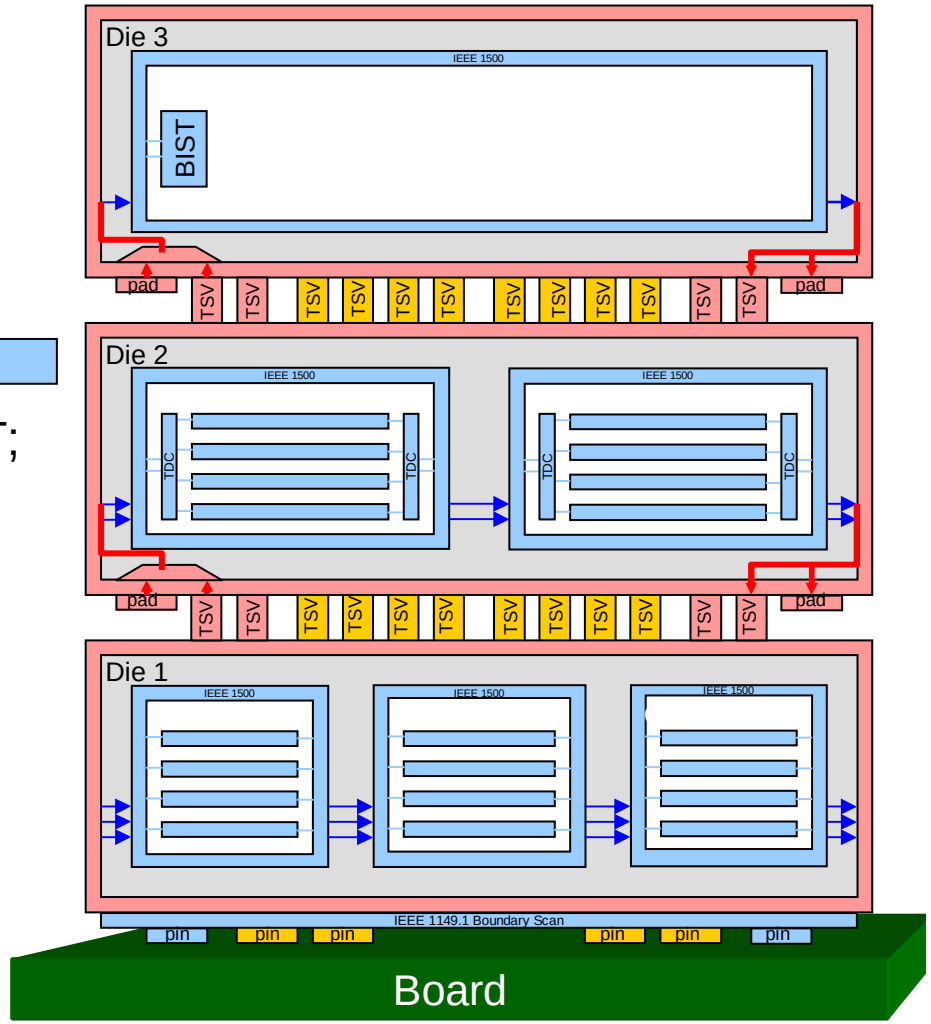
- Stack product: IEEE Std 1149.1

3D-DFT Architecture

Test wrapper per die

- Based on IEEE 1149.1 or 1500
- Two entry/exit points per die:
  1. Pre-bond : extra probe pads
  2. Post-bond : extra TSVs

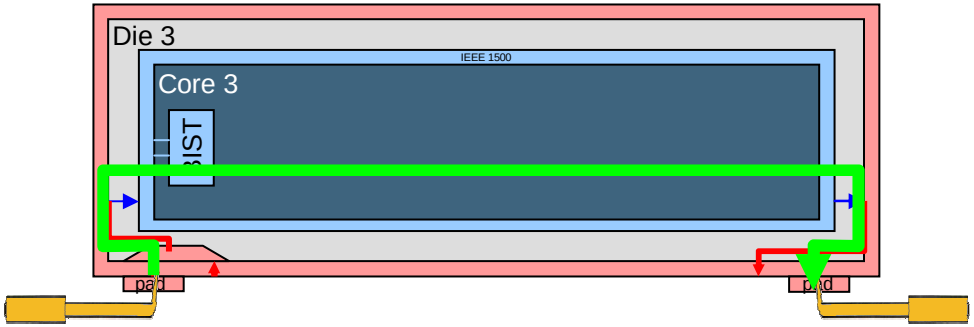
[Marinissen et al. – VTS'10 / 3DIC'10]



# 3. 3D-DFT architecture

## Modes of operation

- Pre-bond
  - Die test
- Post-bond
  - Die 1/2/3 test
  - Interconnect 1-2 + 2-3
- Post-packaging
  - Serial debug



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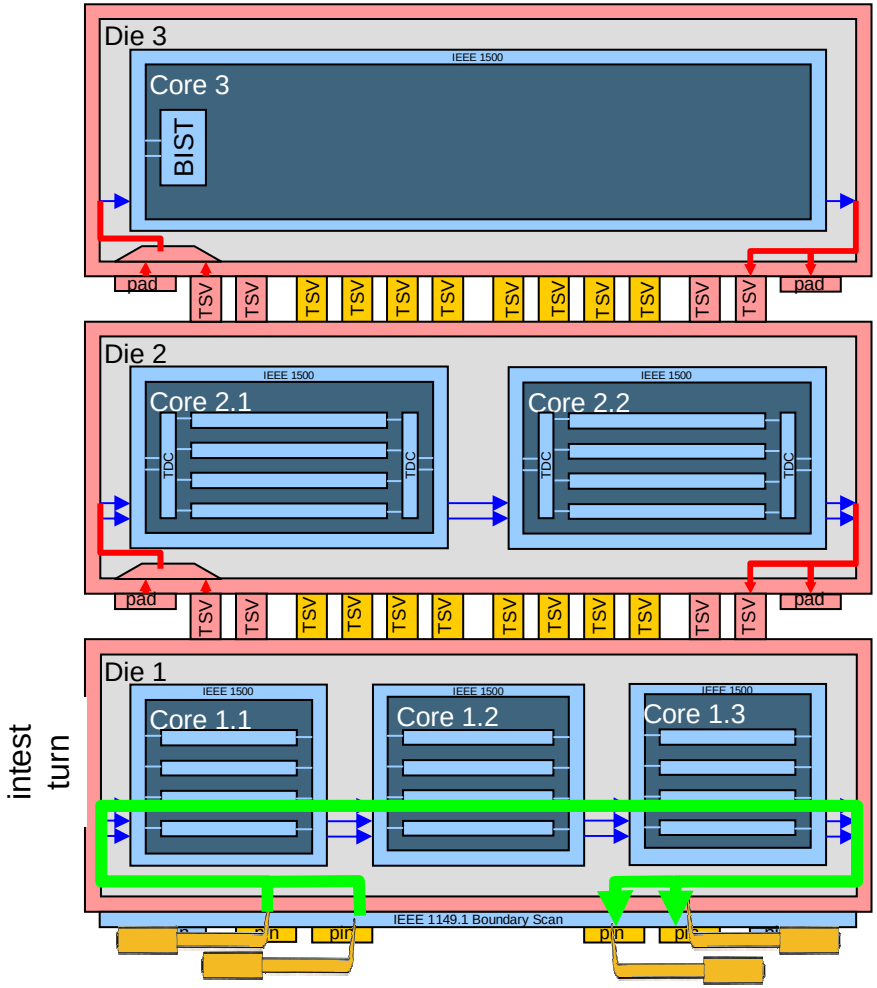

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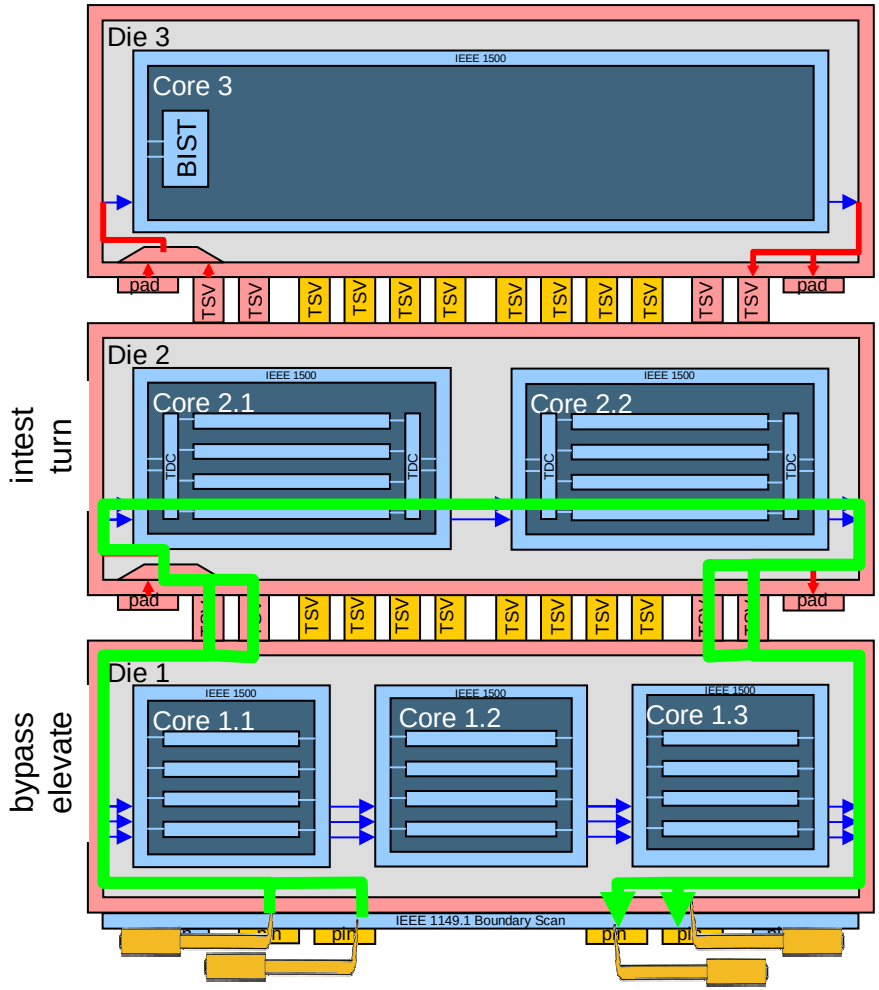





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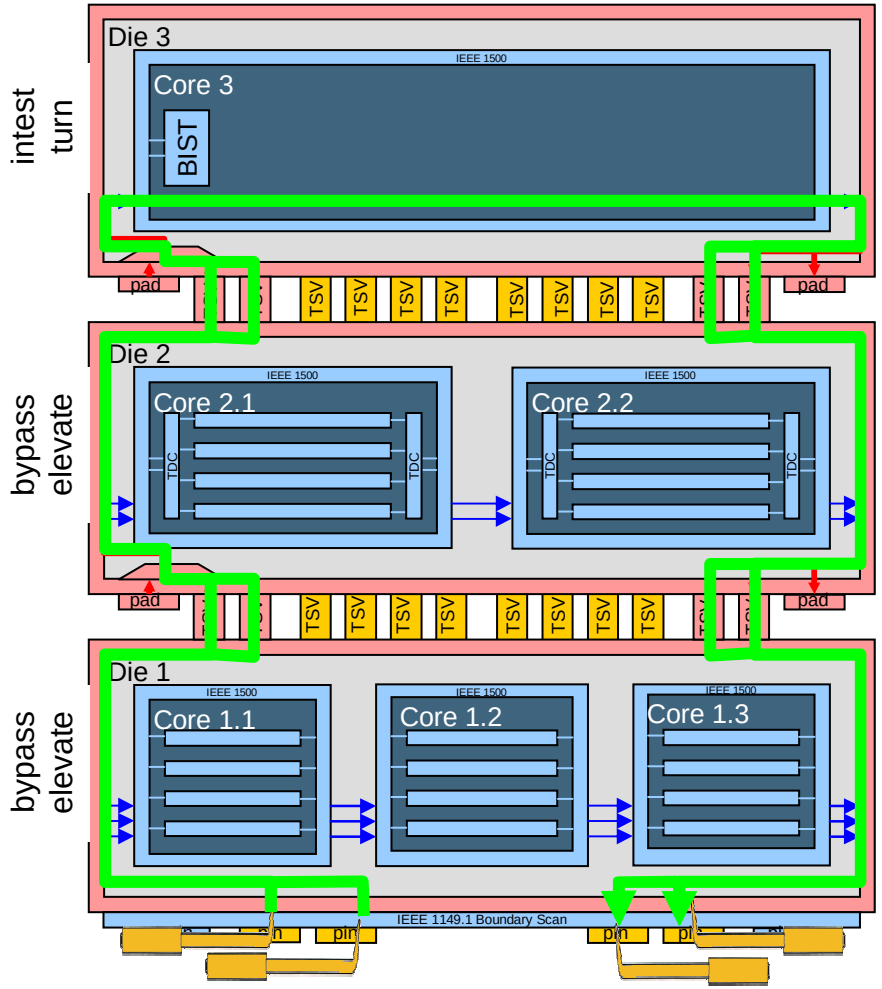





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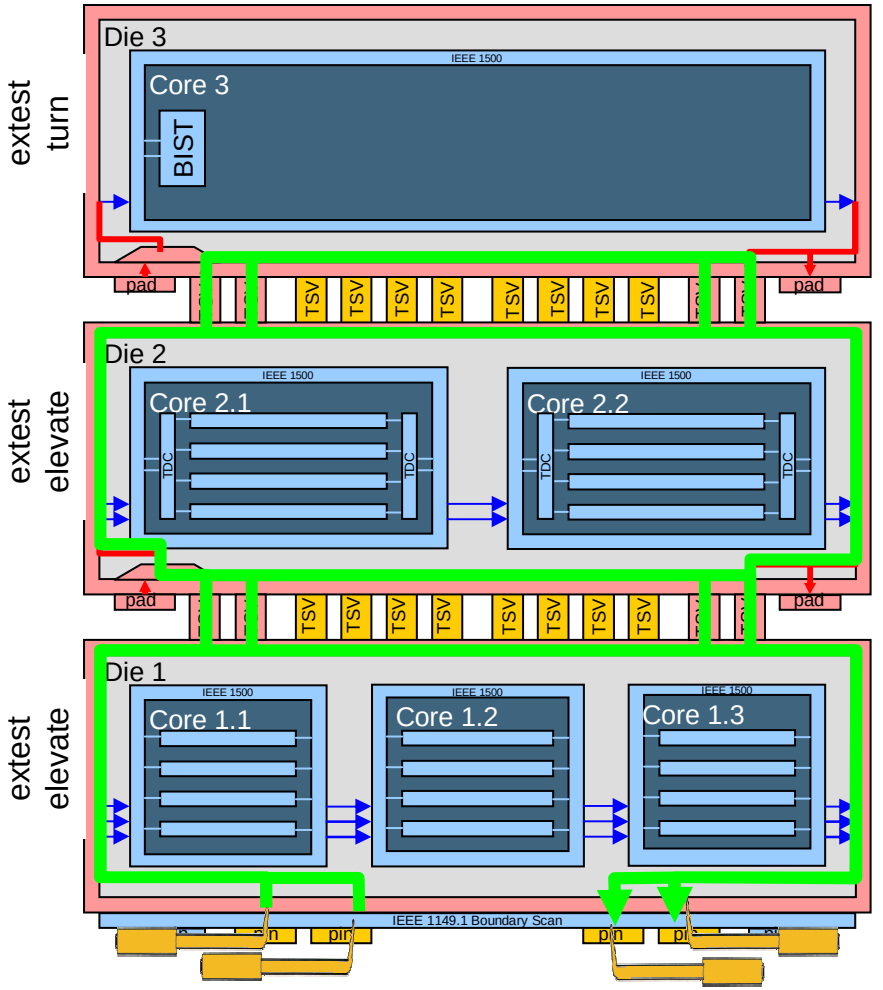





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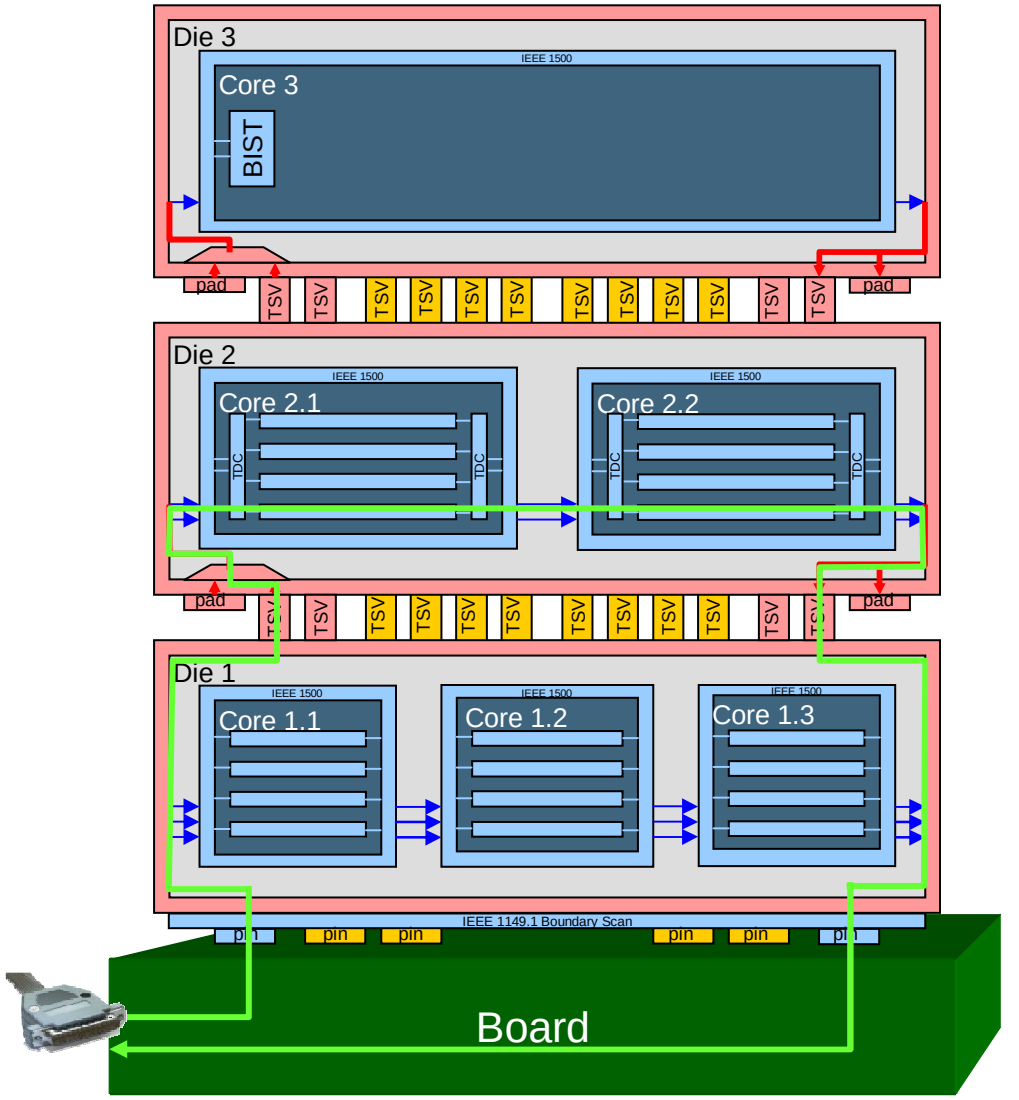
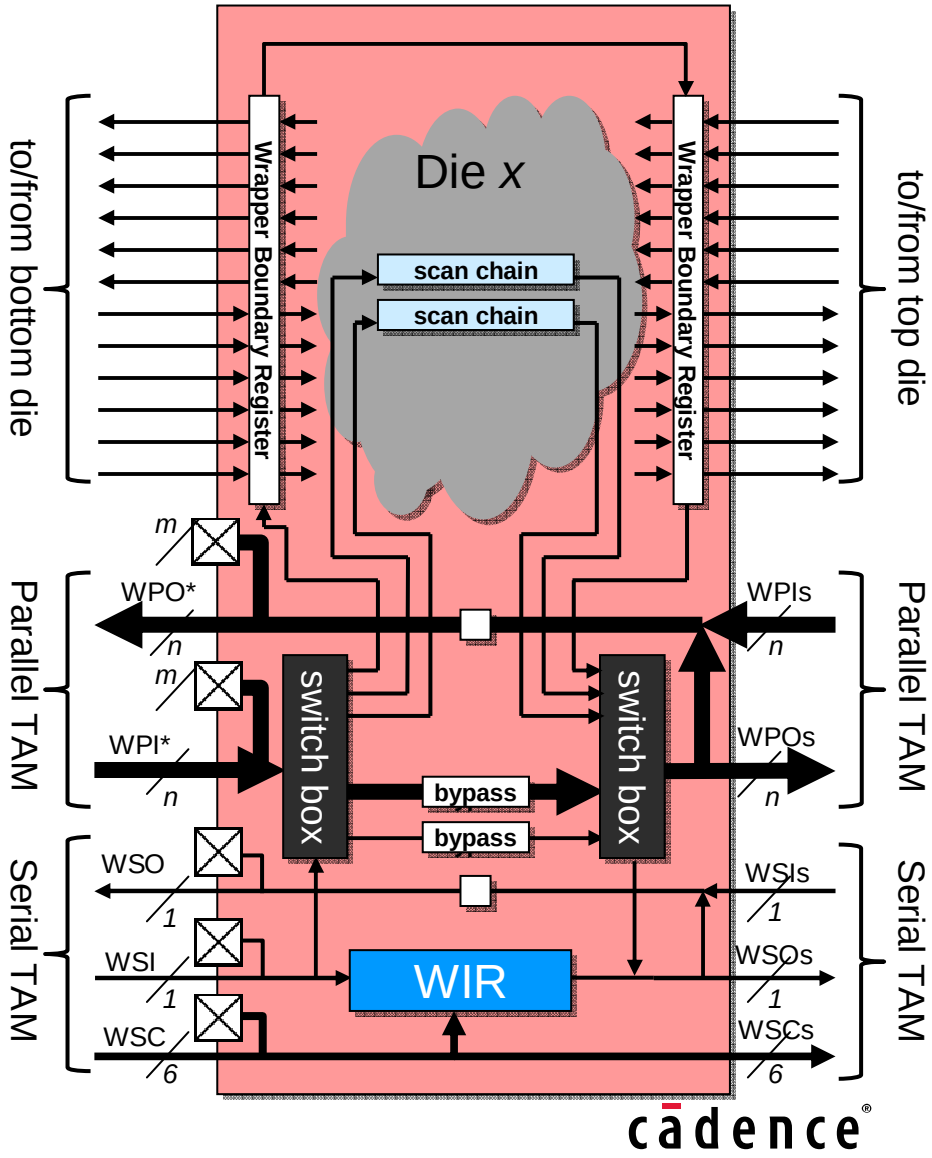


# 3. 3D-DFT architecture

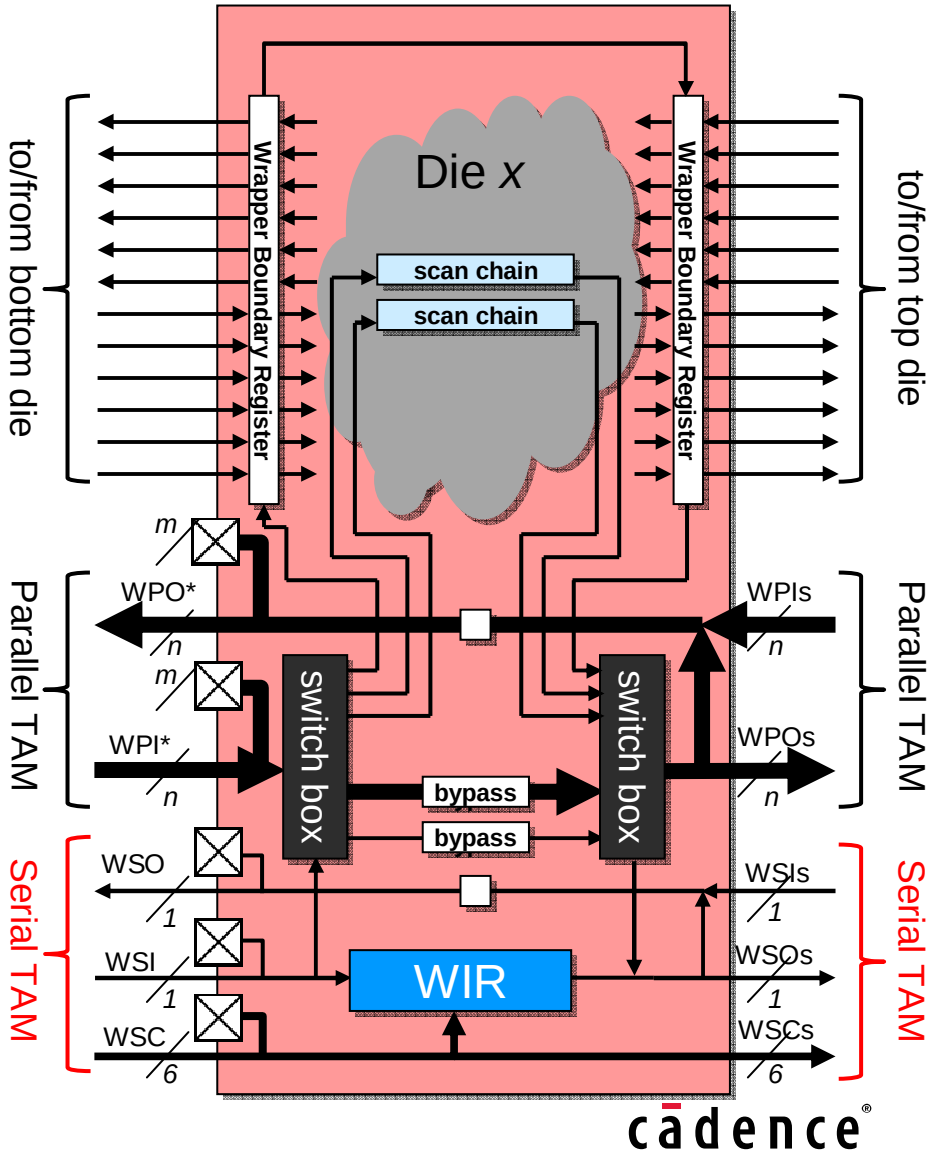
## Schematic view: wrapped die



# 3. 3D-DFT architecture

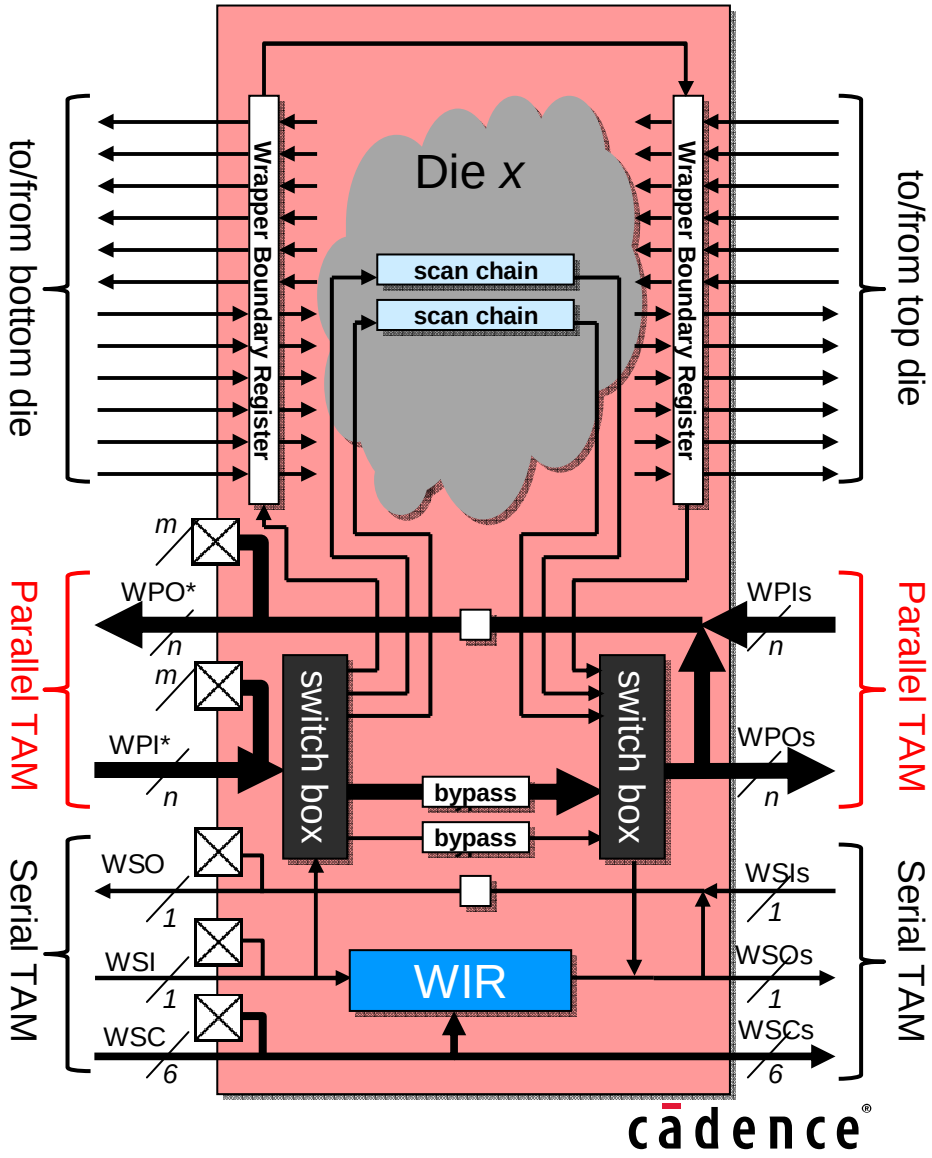
## Schematic view: wrapped die

- Serial Test Access Mechanism (TAM)
  - Instructions
  - Low-bandwidth test data
  - Typical usage: board-/system-level debug



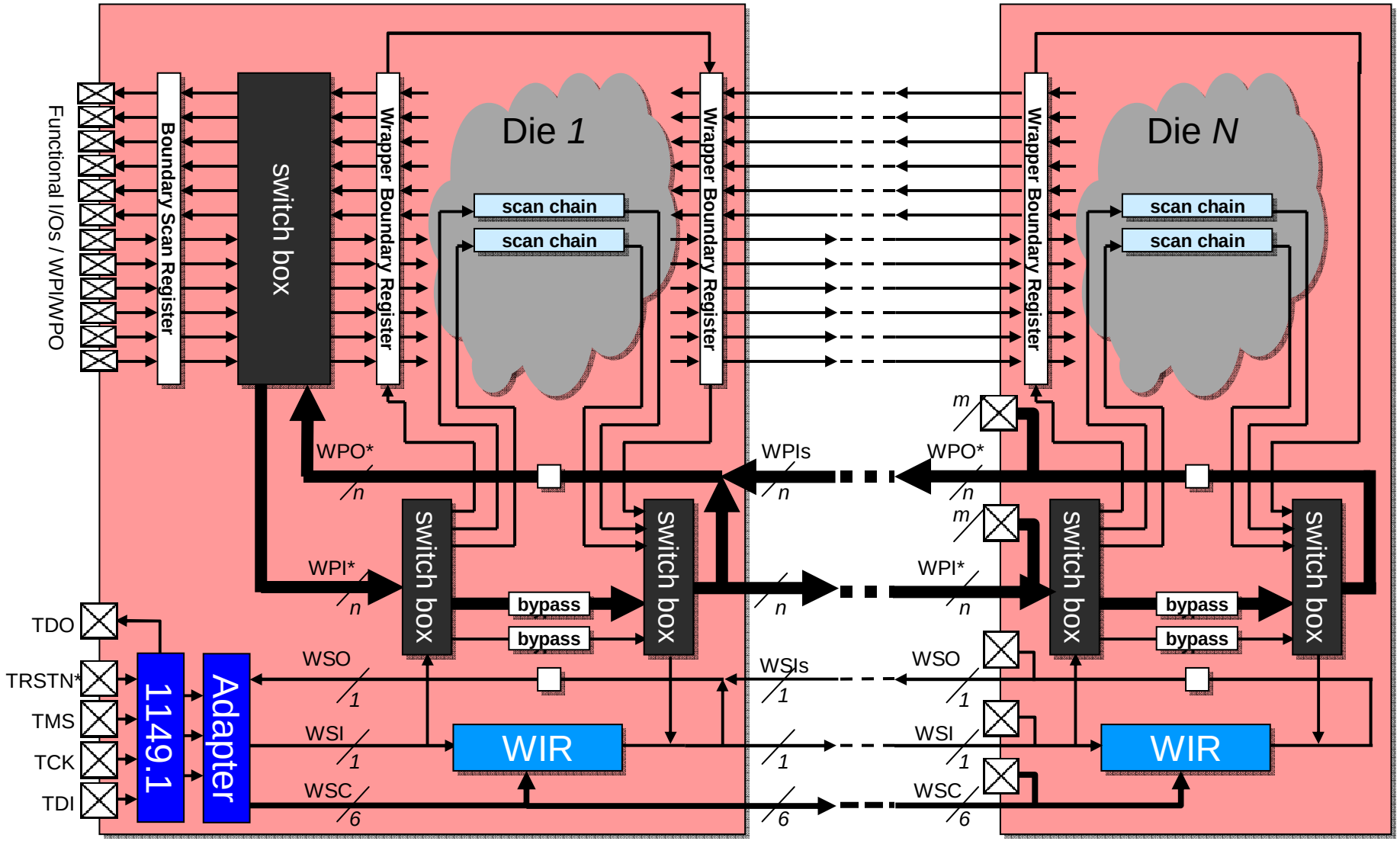
# 3. 3D-DFT architecture
# Schematic view: wrapped die

- Serial Test Access Mechanism (TAM)
  - Instructions
  - Low-bandwidth test data
  - Typical usage: board-/system-level debug
- Parallel TAM
  - High-bandwidth test data
  - Typical usage:
    - Volume production testing in semiconductor factory



# 3. 3D-DFT architecture

## Schematic view: stack







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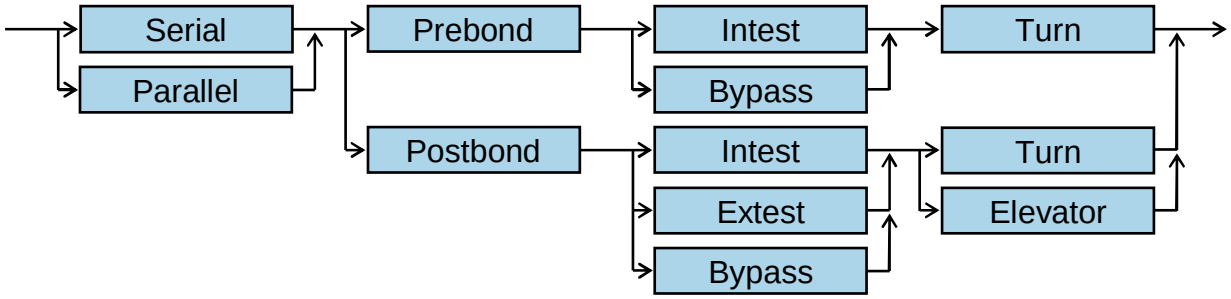
# 3. 3D-DFT architecture

## Flexible instruction set-up

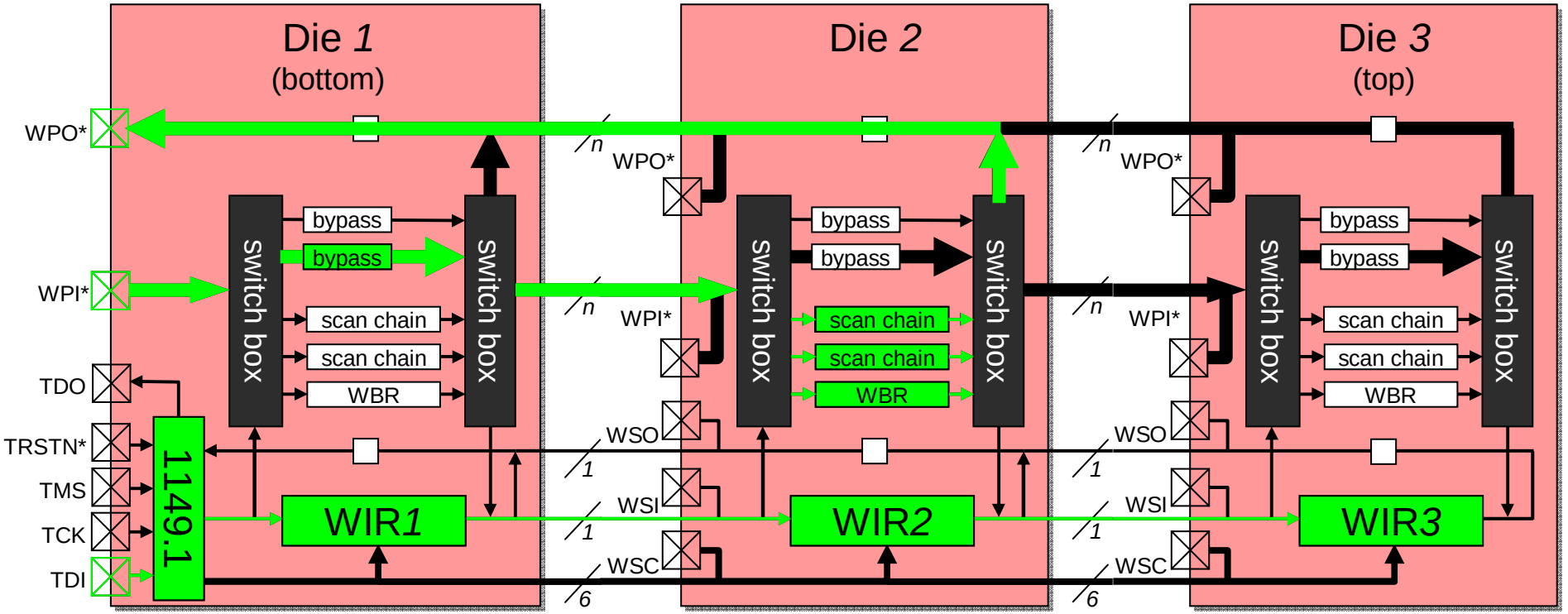
- Implemented instructions decided at design-time
  - Different instructions enable different test access paths




- Flexible test scheduling decided at test-time
  - Inclusion/exclusion of tests for different phases of test flow
  - Reordering of tests (reject-oriented analysis, abort-on-first-fail)

# 3. 3D-DFT architecture

## Test mode set-up example




ParallelPostbond BypassElevator

ParallelPostbond IntestTurn

ParallelPostbond BypassTurn

Note: Figure abstracts from functional circuitry and only shows DfT features

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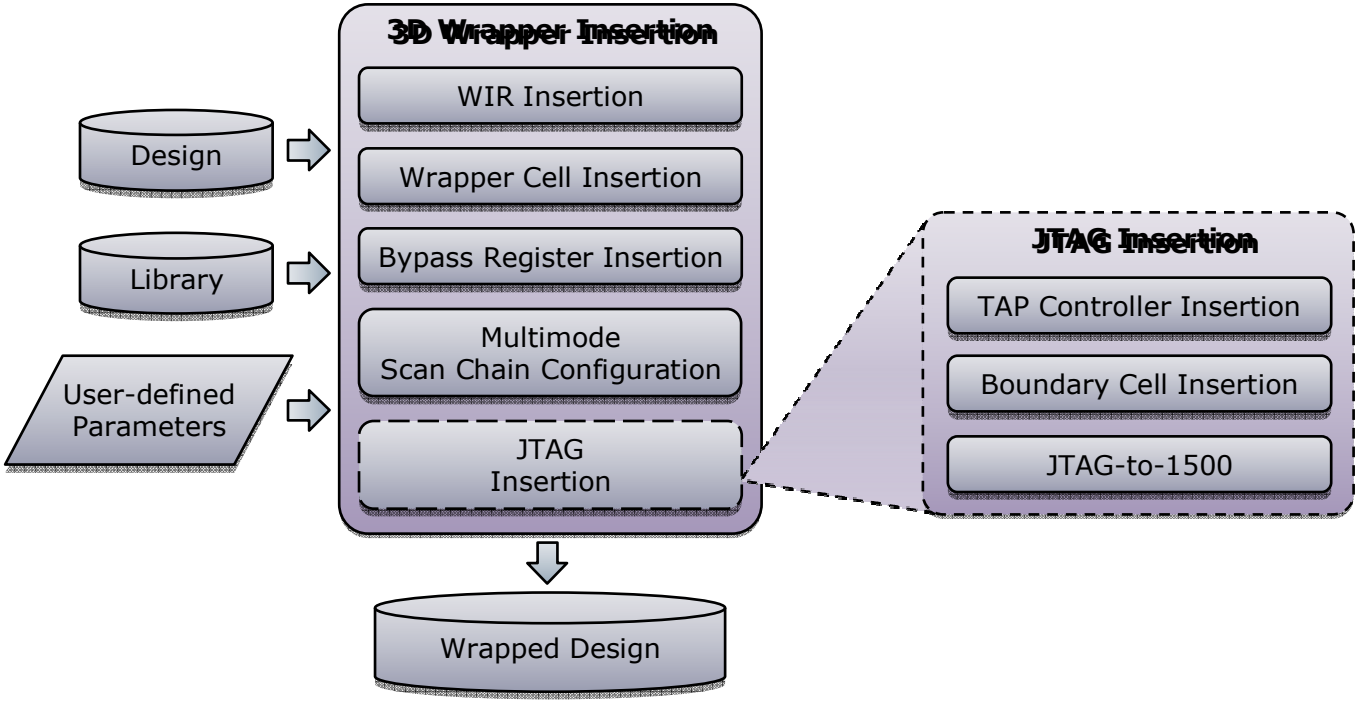
# 4. 3D wrapper generation flow

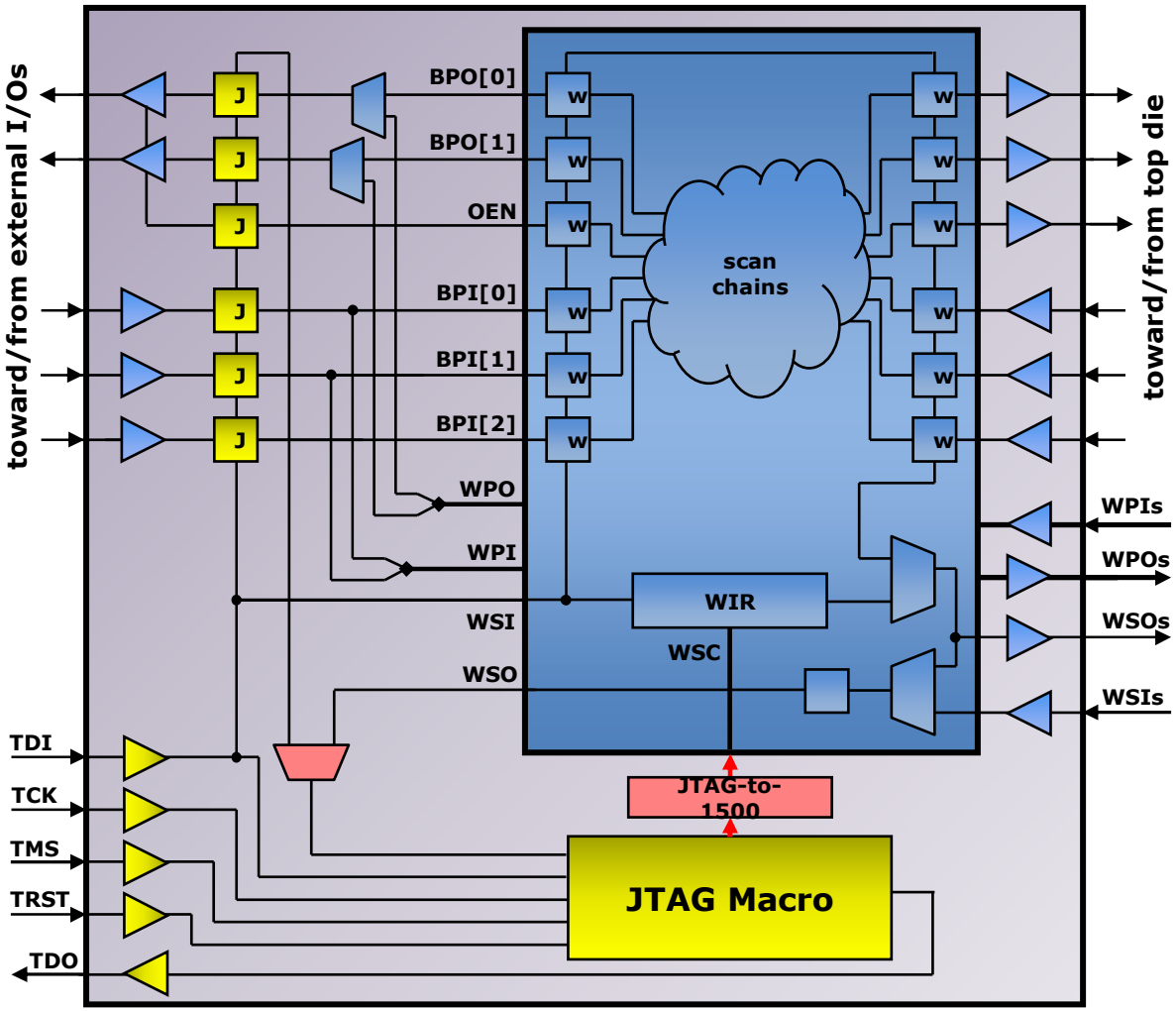
- DfT Insertion with *Encounter RTL Compiler*



# 4. 3D wrapper generation flow

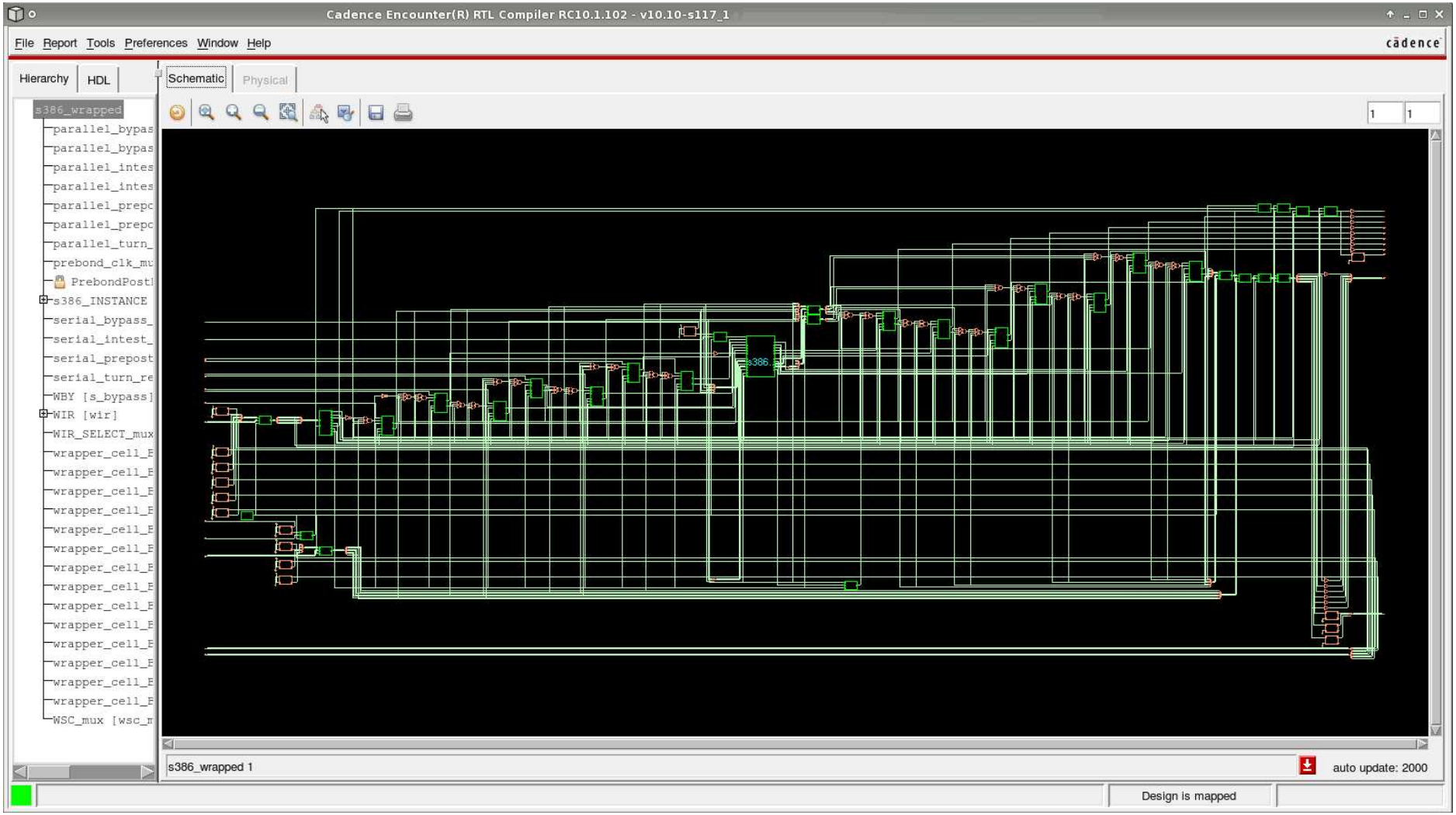
## JTAG insertion

- JTAG macro insertion (TAP controller, IR, decode logic)
- Boundary cell insertion at bottom I/Os
- JTAG-to-1500 (preventing pins)
  - Operation sequence
    1a. JTAG: “WIR Program”
    1b. 1500: WIR loading
    2a. JTAG: “scan”
    2b. 1500: scan
  - Requires JTAG-to-1500 adapter



# 4. 3D wrapper generation flow

## 3D wrapper schematic view



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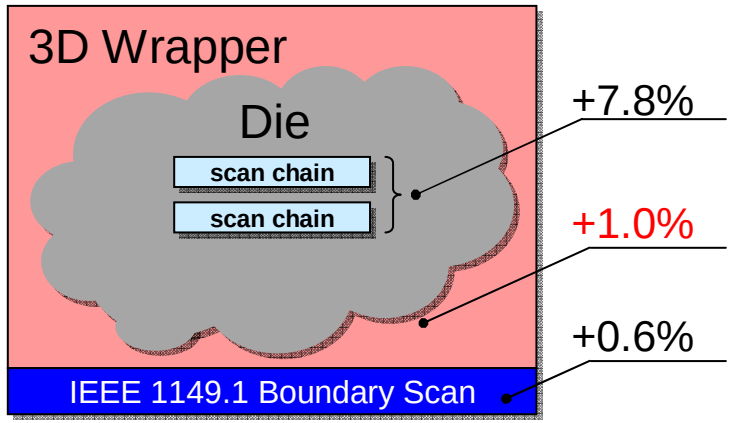
# 5. Results

## 3D-DFT wrapper and skin model

- TSMC test chip
- 65nm CMOS
- Functional design
  - 727 functional I/Os
  - 229,249 std. cells
  - 28,224 flip-flops
  - Area 2,070,536µm2
- 3D wrapper area:
  - 1.0% of the chip std. cell area
  - negligible for realistic designs

DfT Area:



# 6. Conclusion

## Summary: DFT for pre- and post-bond

- 3D chip stacking using Through-Silicon Vias has much potential
- 3D test challenges include pre-bond and post-bond testing
- 3D-DfT architecture
  - Test-only pads for pre-bond testing
  - Serial and Parallel test access mechanisms
  - TestTurns: to bypass upper dies in stack
  - TestElevator mode: for test paths to/from upper dies
- 3D wrapper insertion flow
  - Inserts 1500-style wrappers and 1149.1 for bottom die
  - Generates input to run ATPG
- Industrial case study: negligible area costs of 3D wrapper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