3D-IC is Now Real: Wide-IO is Driving 3D-IC TSV

Samta Bansal and Marc Greenberg, Cadence
EDPS
Monterey, CA
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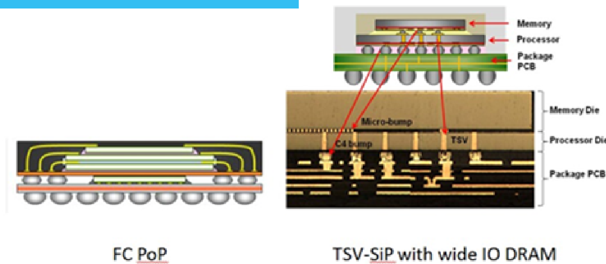
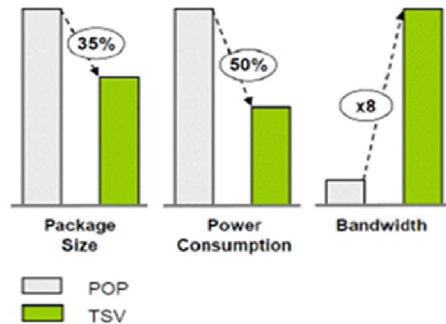
What the fuss is all about …

* Source : ECN Magazine March 2011

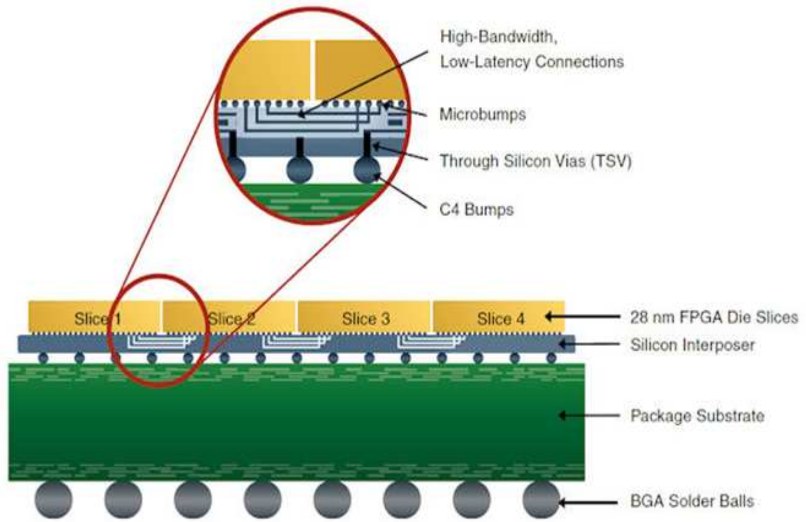


	Conventional 3D Package (FC-PoP) with LPDDR2	TSV-SIP with Wide IO memory
Memory I/O Power Consumption	176 mW	44 mW



Comparison of package performance: wire-bonding PoP vs wide IO interface with TSV (Courtesy of Samsung)

Samsung Wide-IO Memory for Mobile Products - A Deeper Look



* Source : EDN Magazine Sep 2010

Enables 100x Improvement in Die-to-Die Bandwidth Per Watt
2-3x Capacity Advantage Over Monolithic Devices

Xilinx brings 3D interconnect to commercialization phase in digital FPGA world

Faster, Denser, Low-power Chips Using 3D-IC TSVs

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What and Why: Wide-IO and TSVs?

Customer drivers in the industry

Performance, power and area (PPA) enables end-product differentiation

Mobility is Key: Faster, Denser, Low-power Chips

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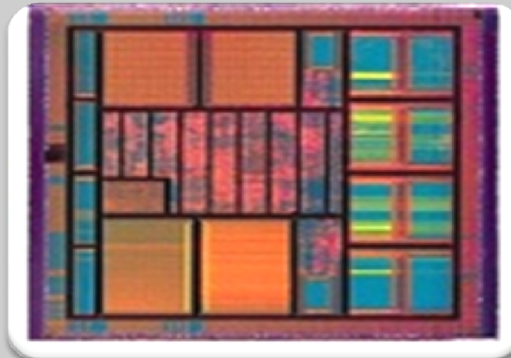
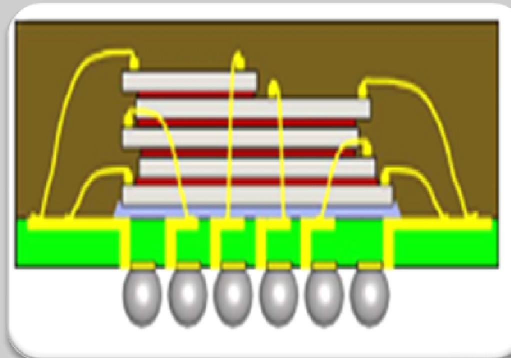
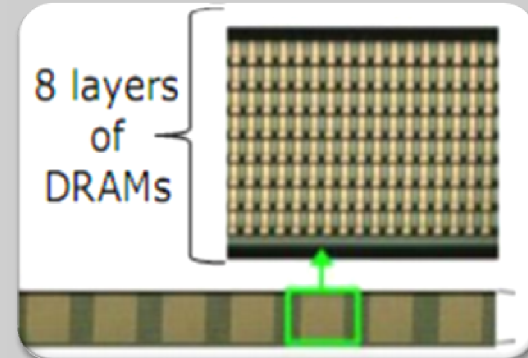
Paradigm shift from 2D SOCs to 3D-ICs

Achieving the PPA goals within shorter time-to-market







SOC: One Large Die

- PROS
  - Most common today
  - Strong ecosystem
  - Cost effective for very high volume production
- CONS
  - Long development times
  - "Bet-the-farm" tape-outs
  - NREs and yields < 22 nm?
  - One process for Logic, Memory and Analog?
  - HW difficult to customize

SiP: Multi-Die Wirebonded

- PROS
  - Production-proven
  - Mix different processes
  - Build a system quickly
  - HW easily customized
  - Short development time
- CONS
  - Bonding needs I/O rings
  - Wires add RLC parasitics - limited power savings
  - Limited speed gains
  - Limited number of layers

3D-IC TSV: Multiple Die Through Silicon Vias

- PROS
  - Densest implementation
  - Low power, high speed
  - Ideal for high complexity
  - Easy to mix processes
  - 1000s of TSVs possible
  - Die- / wafer level-stacking:
  - Flexibility versus unit cost
- CONS
  - Ecosystem emerging
  - Volume production ramping
  - Thermal Issues?

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CPU to DRAM

Existing inter-die connection methods

Parallel Connection across a PCB

- Most common CPU/SoC-to-DRAM connection today
- Well understood and extensible
- Many pins required for high bandwidth
  - ~60 signal pins for a 32-bit LPDDR2 interface (2012 low-mid range smartphone)
  - ~120 signal pins for a 2-channel LPDDR2 interface (2012 mid-high end smartphone)
  - ~300 signal pins for a 3-channel 64-bit DDR3 interface (2012 PC)

Serial Connection Across a PCB

- Fewer pins than parallel connection
- Common for PCIe and other SerDes-based standards
- Can provide data transfer over longer physical distances if needed
- Potential latency and power considerations
- Not commonly used for DRAM at present; future solution?

Pin Count, Power, Latency Concerns?

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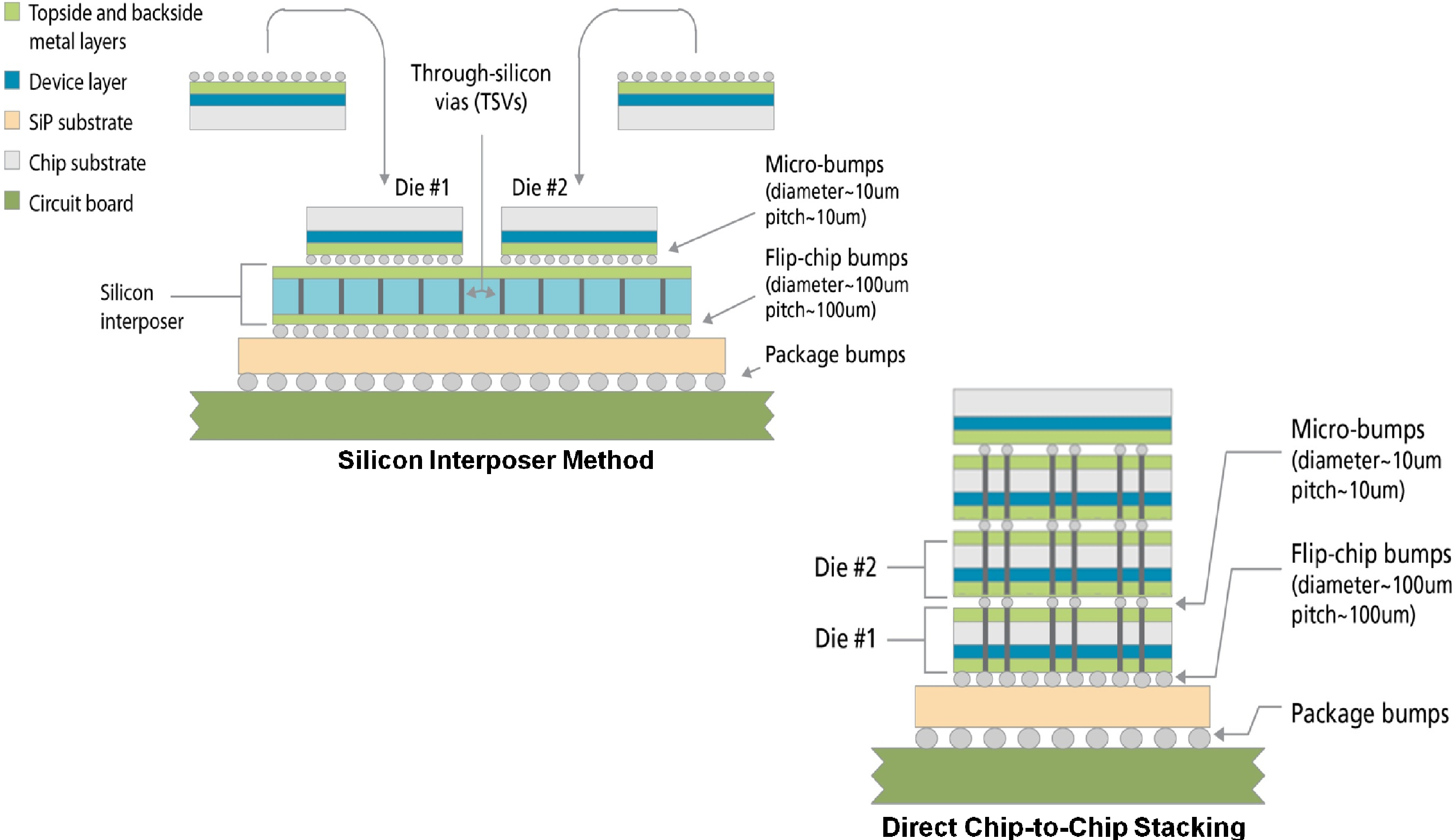
New inter-die connection method: TSV



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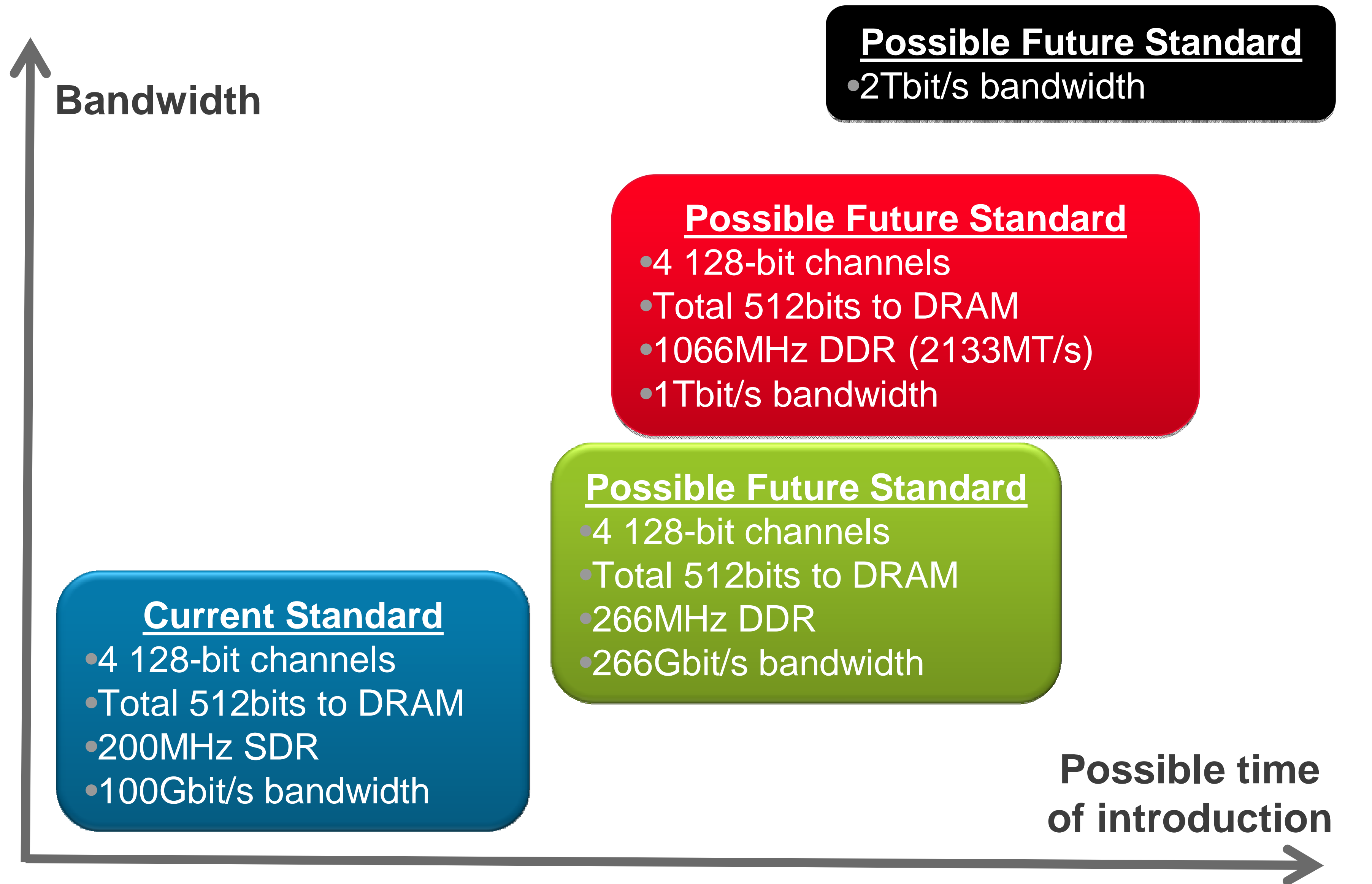
What is Wide-IO DRAM?



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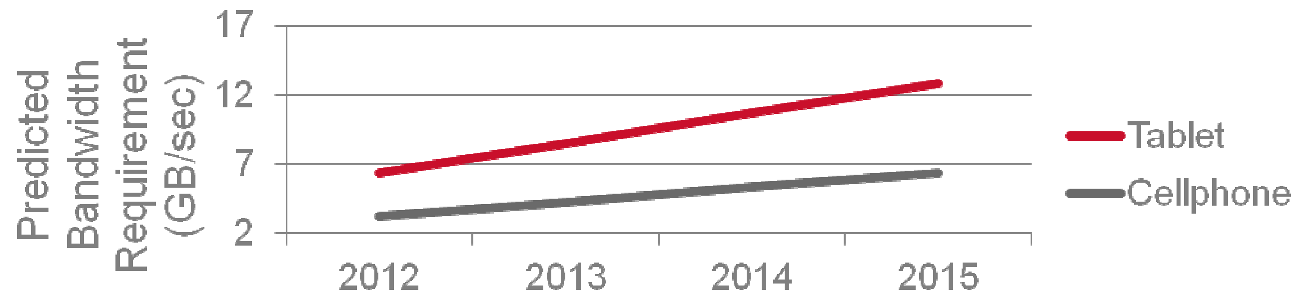
Why do you need Wide-IO DRAM?



Solutions	LPDDR2 533 MHz		LPDDR3 800 MHz		WideIO 200 MHz	
	Single Channel	Dual Channel	Single Channel	Dual Channel	Single die + LPDDR2	Cube
Density (2014)	2x 4 Gb	4 x 4 Gb	2 x 8 Gb	4 x 8 Gb	2 x 8 Gb	4 x 8 Gb
Bandwidth	4.25 GBy/s	8.5 GBy/s	6.4 GBy/s	12.8 GBy/s	17.1 GBy/s	12.8 GBy/s
Power (burst read)	330 mW	660 mW	430 mW	860 mW	730 mW	540 mW
Power / Bandwidth	78 mW/GByps		67 mW/GByps		43 mW/GByps	42 mW/GByps
Cost (2014)	N/R	1	N/R	1.1	1.2	1.4

➔ WideIO provides 2x power efficiency compared to LPDDR2/3

- The initial JEDEC proposal is providing 12.8GBytess bandwidth. Increasing DRAM frequency to 266MHz and implementing dual data rate transfers will provide eventually more than 34GBytes/s.

RTI Conference – 13th Dec 2011
A Three-Layers 3D-IC Stack including WideIO and 3D NoC 18

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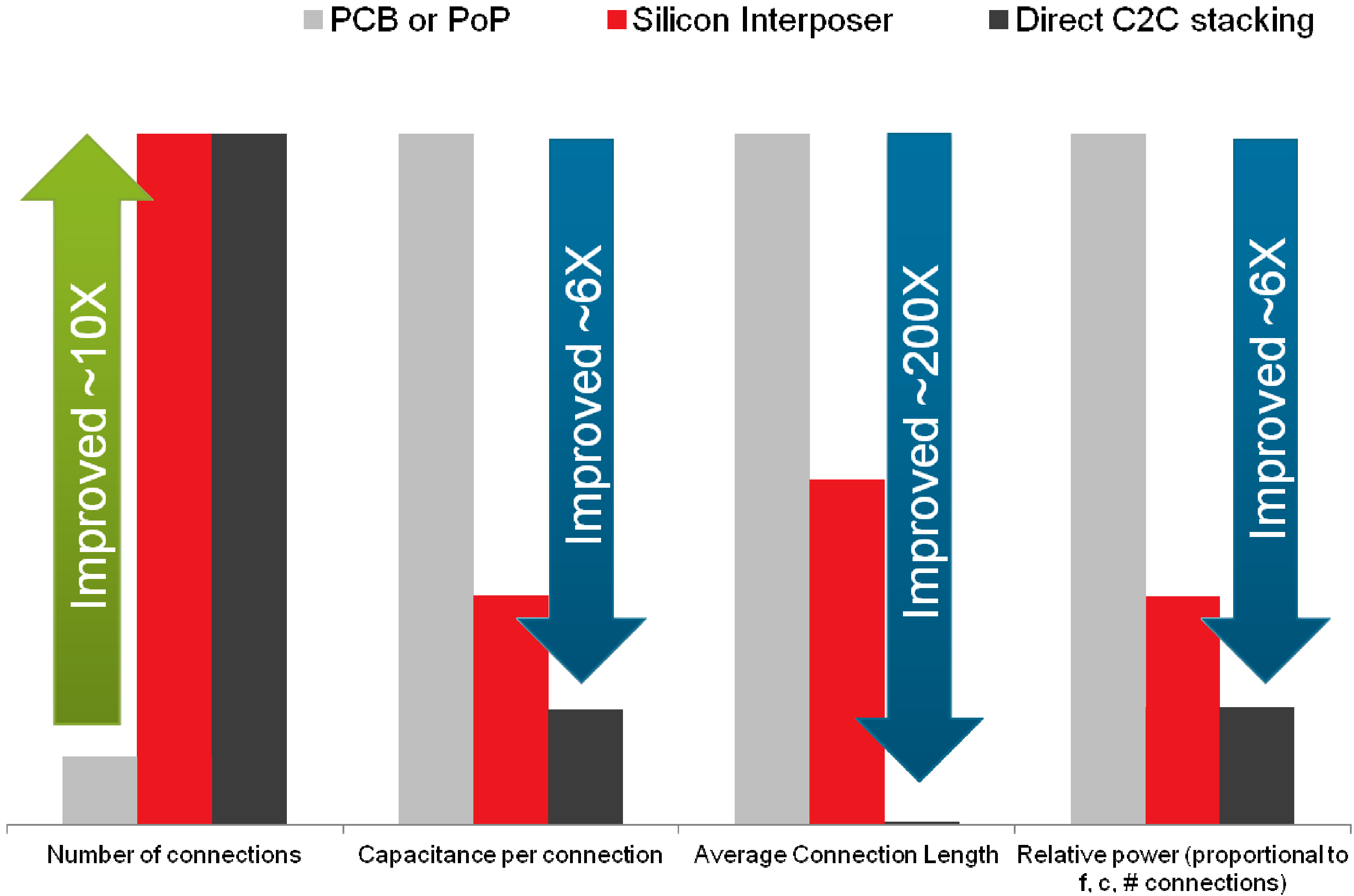
General benefits of TSVs



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Why Wide-IO is driving TSV

DRAM is the ideal candidate to drive TSV technology

- Usually manufactured on a non-logic process
- Requires high bandwidth connection between CPU and DRAM
- Uneconomic or impossible to place large capacity (Gbits) of DRAM on same die as CPU
- Low power connection between dies desirable
- Possibility of different memory configurations using the same CPU die

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Implementing Wide IO and TSVs

Real chip, real example walkthrough

Wioming test chip program

Same SoC addressing several schemes of 3D integration

Wioming

High speed CMOS techno
70mm²
2000 TSVs
1000 bumps
500 balls

	Proof of concept for: Technology	Architecture	Design Flow
Wide IO demonstrator: DRAM on Wioming	❑ Die to Die ❑ Face to Back ❑ TSV middle ❑ Cu Pillar bumps and micro-bumps	❑ Wide memory data bus (512-bit) ❑ High bandwidth (>10GBps) memory interface ❑ Multi-channel memory controller ❑ Test for 3D Memory interconnect	❑ 3D floorplanning ❑ 3D routing (signal & power) ❑ 3D Test ❑ Verification ❑ Power analysis ❑ Thermal analysis
3D NoC demonstrator: Wioming on Wioming	❑ Die to Die ❑ Face to Back ❑ TSV middle ❑ Cu Pillar bumps and micro-bumps	❑ 3D NoC router ❑ 3D serial link ❑ Test for 3D NoC interconnect ❑ TSV Fault Tolerance scheme	
3 Layer demonstrator: DRAM on Wioming on Wioming	Combination of all above techniques		

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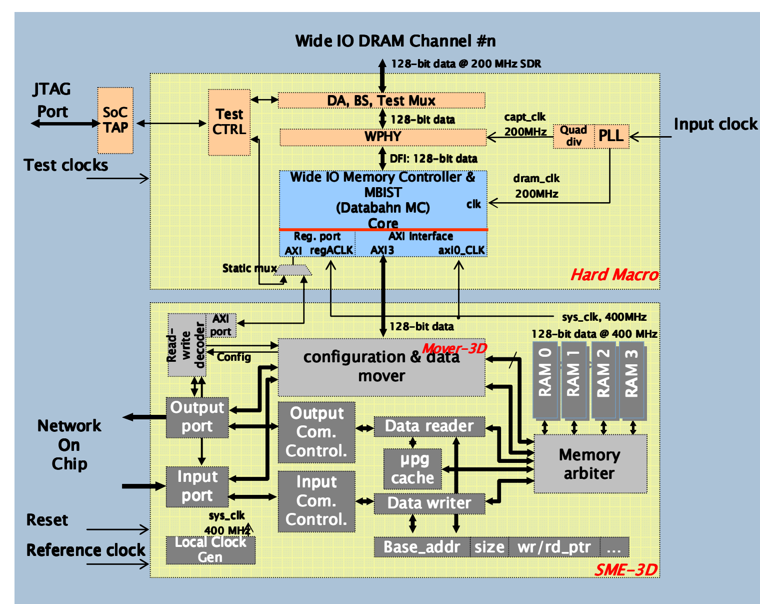
Wide IO SME architecture overview

- Wide IO Memory Controller (Cadence DENALI)
  - Compliant with DRAM specification for Wide IO from JEDEC (http://www.jedec.org/)
  - High performance, and advanced low-power features
  - First deliveries to 3D-IC Wioming ST-Ericsson/LETI project
- Wide IO PHY Interface
  - 200MHz,128 bit ,SDR
  - ~1200 TSVs, µbuffers and µbumps
  - Also integrates ESD protections for DRAM
- Specific Design for Wide IO Testability Integration
  - Boundary scan, direct access, stuck-at, memory bist, PLL test
- Smart Memory Engine
  - Data transfer handling between Wide IO, SRAM and ANoC
  - Integration within ANoC
  - Up to 3.2GB/s data bandwidth



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Cadence Wide-IO DRAM controller

Challenges	Solutions
Merge existing and new technology	• Start with extensible, high performance, low-power base architecture (Supports DDR1, DDR2, DDR3, LPDDR1, LPDDR2 and now DDR4) • Re-add SDR support • Add new Wide IO feature support • Create DFI extensions for Controller-PHY connection
New testing requirements	• Extend BIST engine to test for new classes of error
Verification	• Create memory model of Wide-IO device in Cadence VIP tools • Extend existing configurable verification environment for Wide IO

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Overview of tool and methodology

3D Technology & Design Kit

- Target technology
  - Uses ST-Microelectr
  - Uses TSV middle (∅
  - Is a Flip-Chip packa
  - Is a Face2Back, Die
- Back End kit
  - Virtuoso tech file ad
  - EDI Techno file & ca
  - DRC & LVS « 3D » a

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A Three-Layers 3D-IC Stack including Wide

EDI 3D-IC Stack Design Implementation & Analysis

- Cadence **Encoun** implementation is collaboration with advanced system
- Supports a comp for both impleme
  - Different types o bump, cupper p backside metal l
  - Multiple set of m
- Supports multiple design implemen
  - Silicon interpose
  - Vertical stack.
  - Mixed stack.
- EDI Design meth are proven with s

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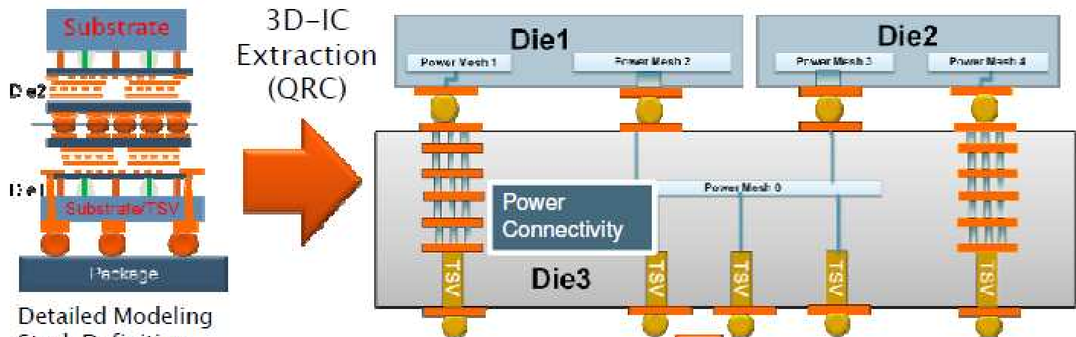
A Three-Layers 3D-IC Sta

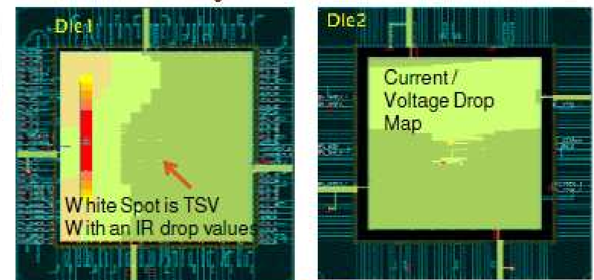
EDI 3D-IC Analysis Methodology



Detailed Modeling
Stack Definition

Encounter Timing
System (ETS)

Encounter Power
System (EPS)



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A Three-Layers 3D-IC Stack including WideIO and 3D NoC

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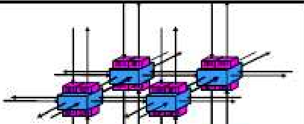
Overview of tool and methodology

3D-ANoC TSV Floorplanning



- 3D-ANoC TSV c
  - Symetrical 3D NoC conn
  - 3D NoC matrix also con
- EDI 10.1 tool fl
  - Use automated TSV crea
    - *– set die to botto*
    - *– Create the TSV*
    - *– Assign TSV + b*
    - *– save TSV & bac*
    - *– set die to top*
    - *– create front Bu*
  - Then, use semi-automa
    - PG connections b
    - µ- Buffer cell plac
    - PG routing within
    - ESDs, etc ...

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3D-IC : Power & IR drop analysis

- Using Encount
  - Currently using
  - No sign-off mod
- Power analysis
  - Top chip power
  - according to tar
- 3D IR-Drop ana
  - Bottom Die
  - => supplied from th supplies
    - 0.02 mV m
  - Top Die
  - => supplied from th
    - 0.2 mV ma

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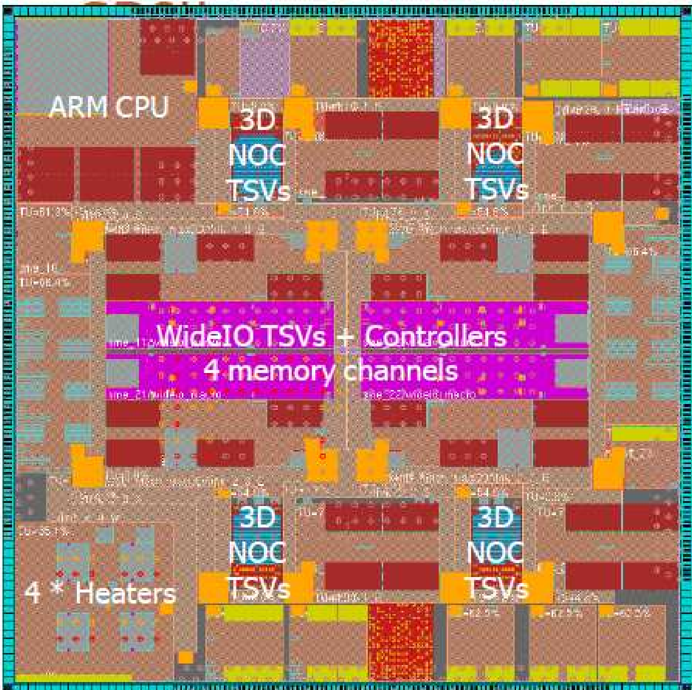
Wioming Final



Circuit Technology
- High speed CMOS TSV middle process
- Face2Back, Die2Wafer, Flip-Chip 3Dassembly

Main features
- WideIO memory controllers
- 3D ANOC
- 3GPP LTE multi core CPU backbone
- ARM host CPU

Circuit numbers
- 125 Million Transistors
- 400 Macros
- 270 pads
- 1980 TSV for 3D NoC
- 1250 TSV for WideIO memory
- 985 Bumps for flip chip

Circuit performances
- WideIO 200MHz / 512 bits
- Units in the [350 - 400] MHz range
- Asynchronous NoC ~ 550 MHz

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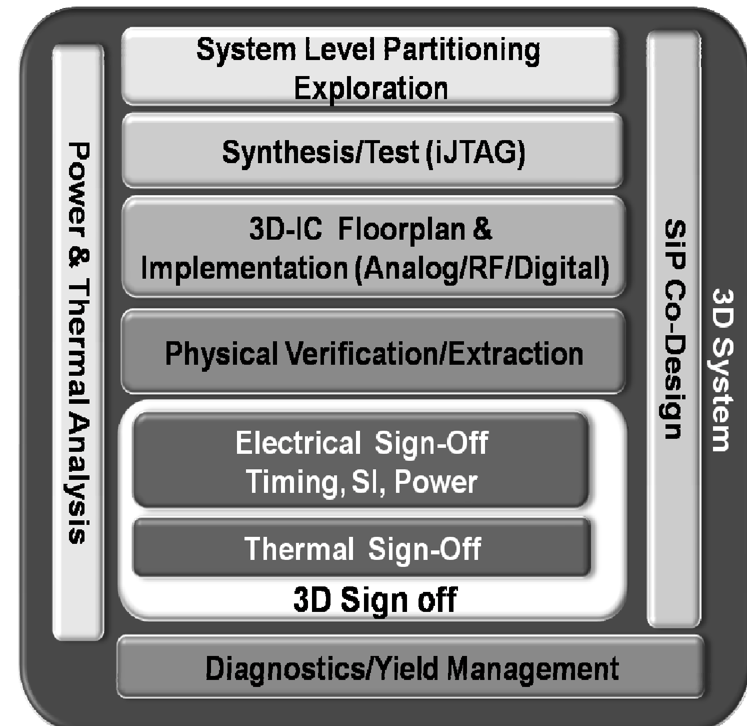
Cadence silicon-proven 3D-IC solution

Plan➔ implement ➔test ➔verify

- Allows heterogeneous integration to offer power, performance in smallest form factor
- **Cadence is technology leader providing complete and integrated 3D-IC solution**
  - Plan->implement->test->verify
  - 1st to market wide I/O memory controller
- **Developed in close partner-collaboration** for past 5 years with leading foundries and customers
- **Multiple 3D-IC tapeouts**
  - Multiple testchip experience: Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  - Production design tapeout in mid-2010



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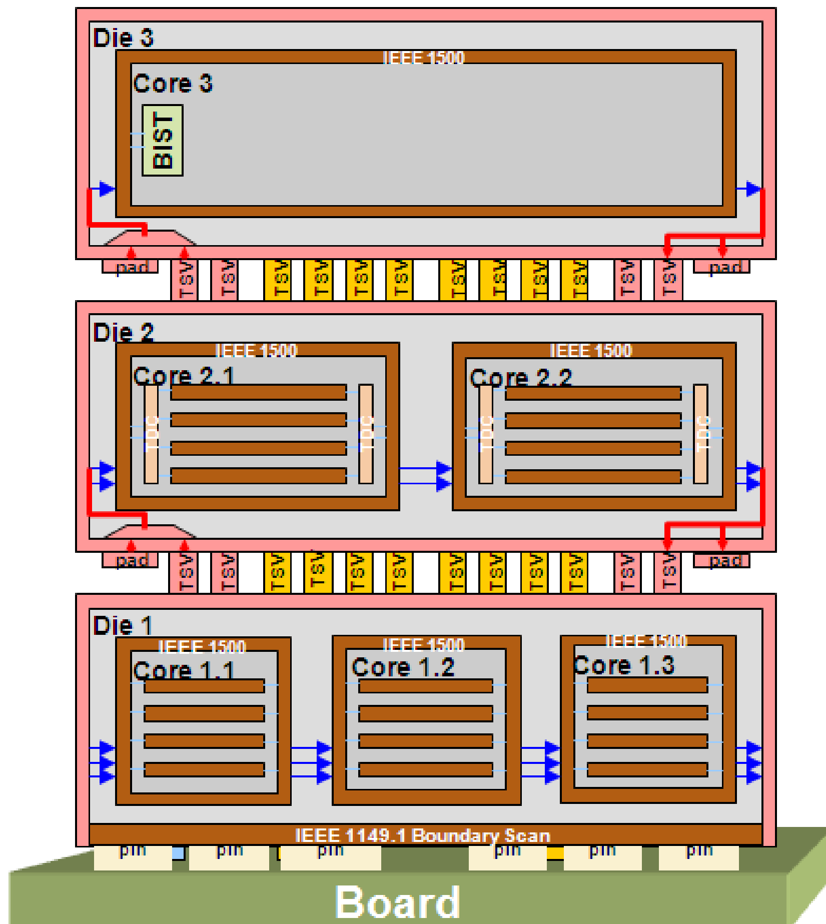
SiP DFT /3D package test



3D DFT on Die-Level

- Insertion of 3D wrapper
- Creating Test patterns
- Verification and Simulation

Testing Die Interconnects

- ATPG for die interconnects

Testing Die in a Stack

- Modular Test approach
- ATPG-on-top test approach

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Challenges in Implementation: Wide IO and TSVs

What are the challenges?

- Manufacturing Wide-IO DRAM and assembly:
  - Test memory wafer after production using FC bumps
  - Thin the wafer to ~50-100um thickness
  - Form TSVs and fill with metal
    - Requires elevated temperatures – extra anneal step
  - Apply backside metal and bumps
  - No opportunity to test here
    - Backside metal bump pitch too fine for most tester heads
  - Handle dies while avoiding mechanical damage
    - They are now the approximate aspect ratio of a postage stamp
  - Attach dies (and interposers, if present) together
  - Does it still work?

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What are the challenges?

- Thermal Issues:
- Where does the heat go?

- Ecosystem Issues:
- How many parties involved in stack production?
- How are responsibilities divided?
- How are liabilities divided?

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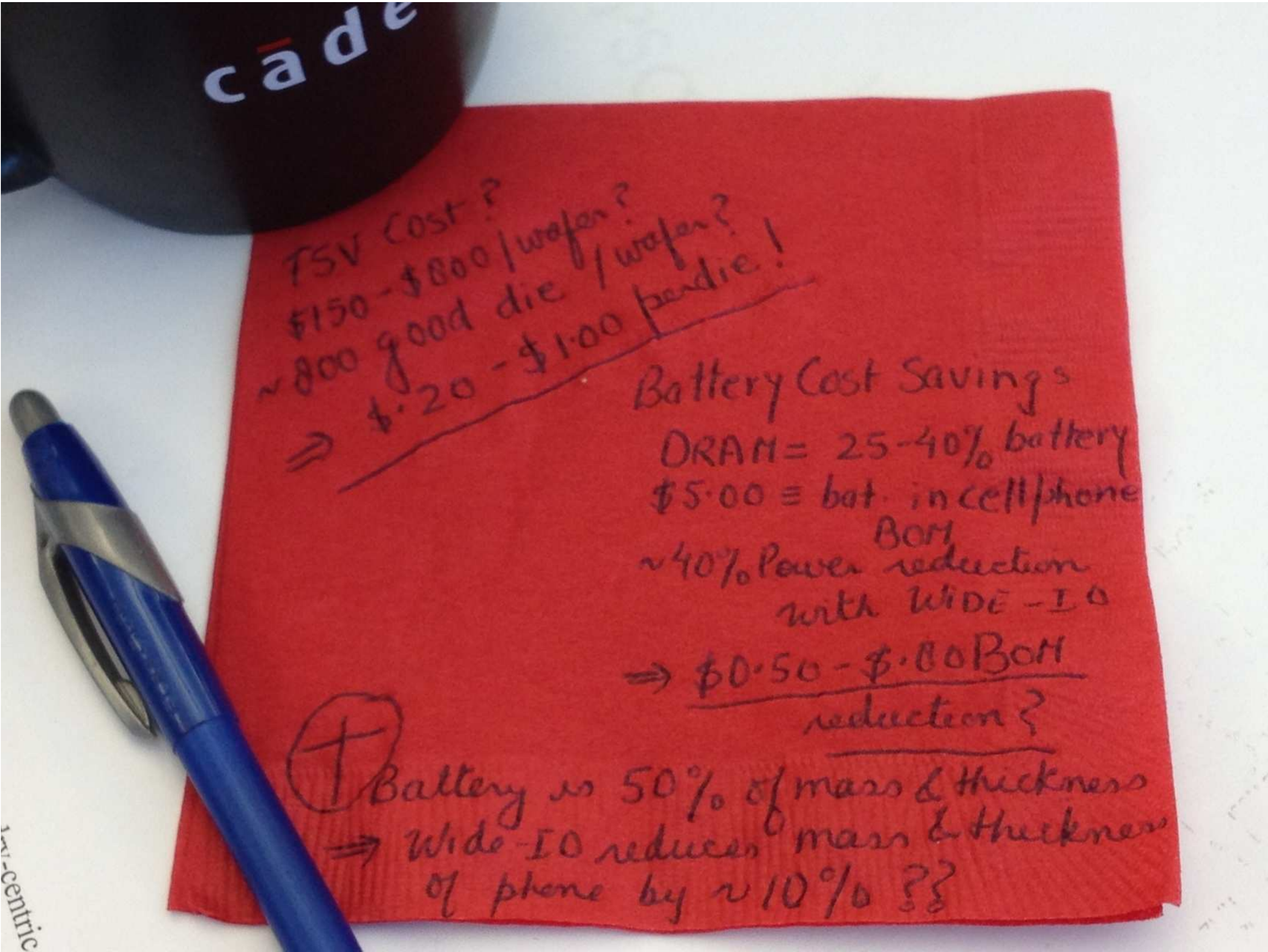
Cost !!!

Back of the napkin calculation



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Conclusion

- Wide-IO and TSV are real
- Cadence believes that Wide-IO DRAM is the technology that will drive adoption of TSV
- Cadence stands ready with EDA tools and IP to enable your TSV designs with real experiences and partnerships with ~8 testchips and 1 production chip already completed.

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