EDA Needs for FPGA

EDPS 2012 April 5th, 2012

Arif Rahman, Karthik Chandrasekar,
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Outline

- Overview
- Desired EDA flow
- Altera’s Needs
- Future Directions

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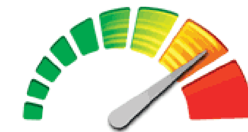
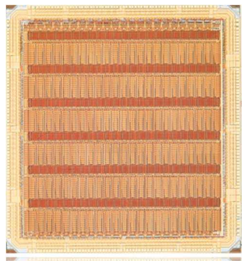
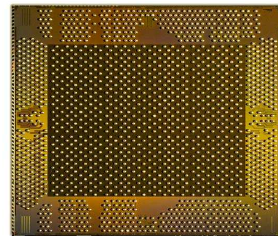
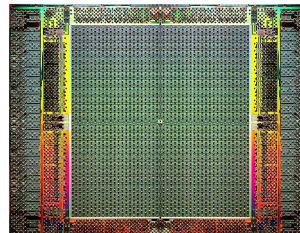
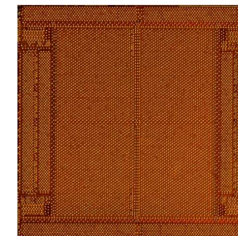
Times Have Changed

SOPC Builder



OpenCL

1990s **2010s**

Glue Logic	Heterogeneous Capabilities	High Integration/ Bandwidth	Hardened Subsystems	Cortex-A9 MPCore
				
Flex 6000 30μ process	Stratix I 130nm process	Stratix IV 40nm process	Stratix V 28nm process	SoC FPGA 28nm process

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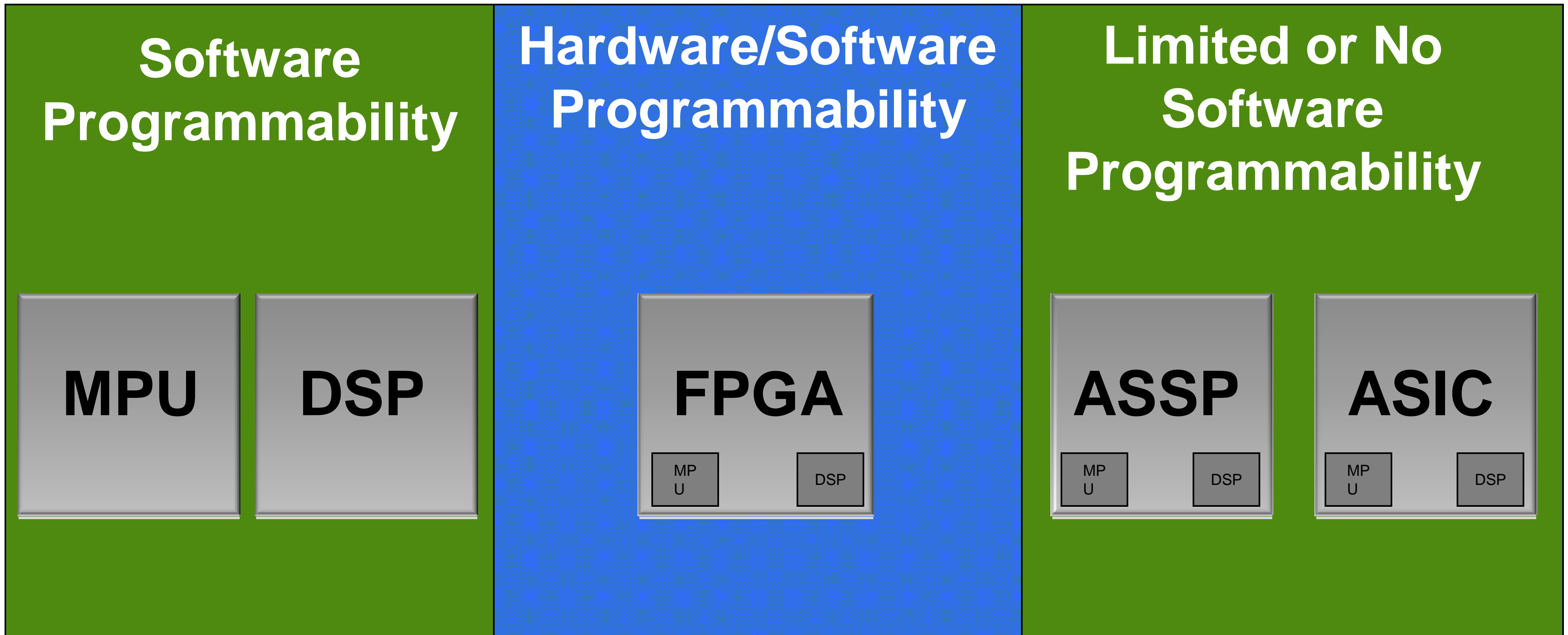
Silicon Convergence



FPGA Platforms Ideally Positioned for Convergence

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Silicon Convergence Laying Foundation for 3D

- Bandwidth expansion
  - High-bandwidth chip-to-chip interface (JEDEC wide IO interface)
  - Optical interconnect
- Additional processing capabilities
  - Memory enhancement
- Product feature set expansion and time-to-market
  - Derivative products
- Energy efficiency
- Integration
  - Fewer components

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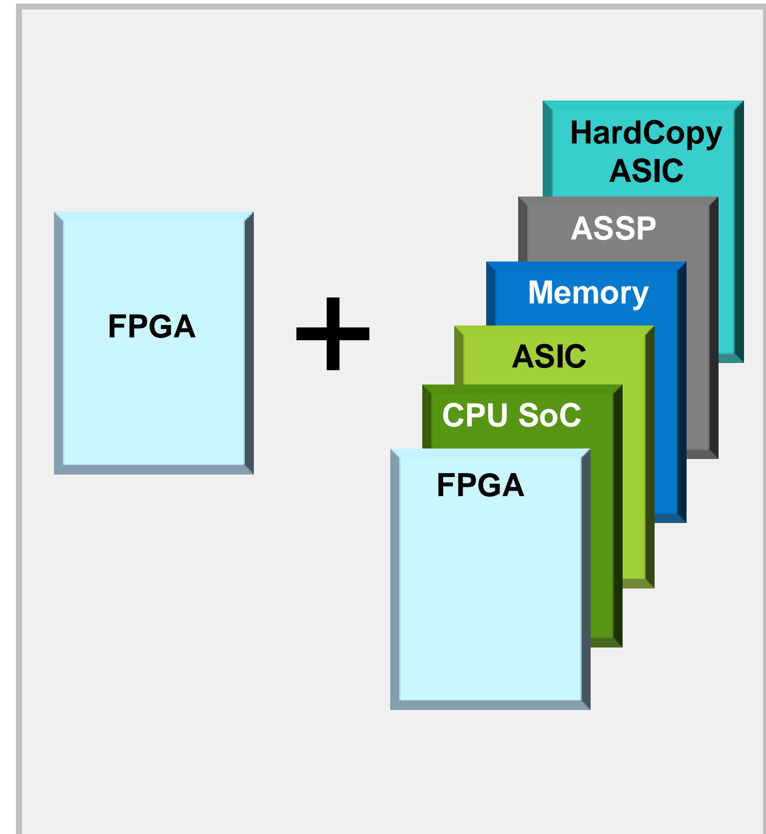
Altera's 3D Silicon Vision

- Customer & application driven heterogeneous system integration in package
  - Mix and match silicon IP
  - Integrated design flow
  - Integrated system test methodology
- Maximum system performance
- Minimum system power
- Smallest form factor
- Reduced system cost



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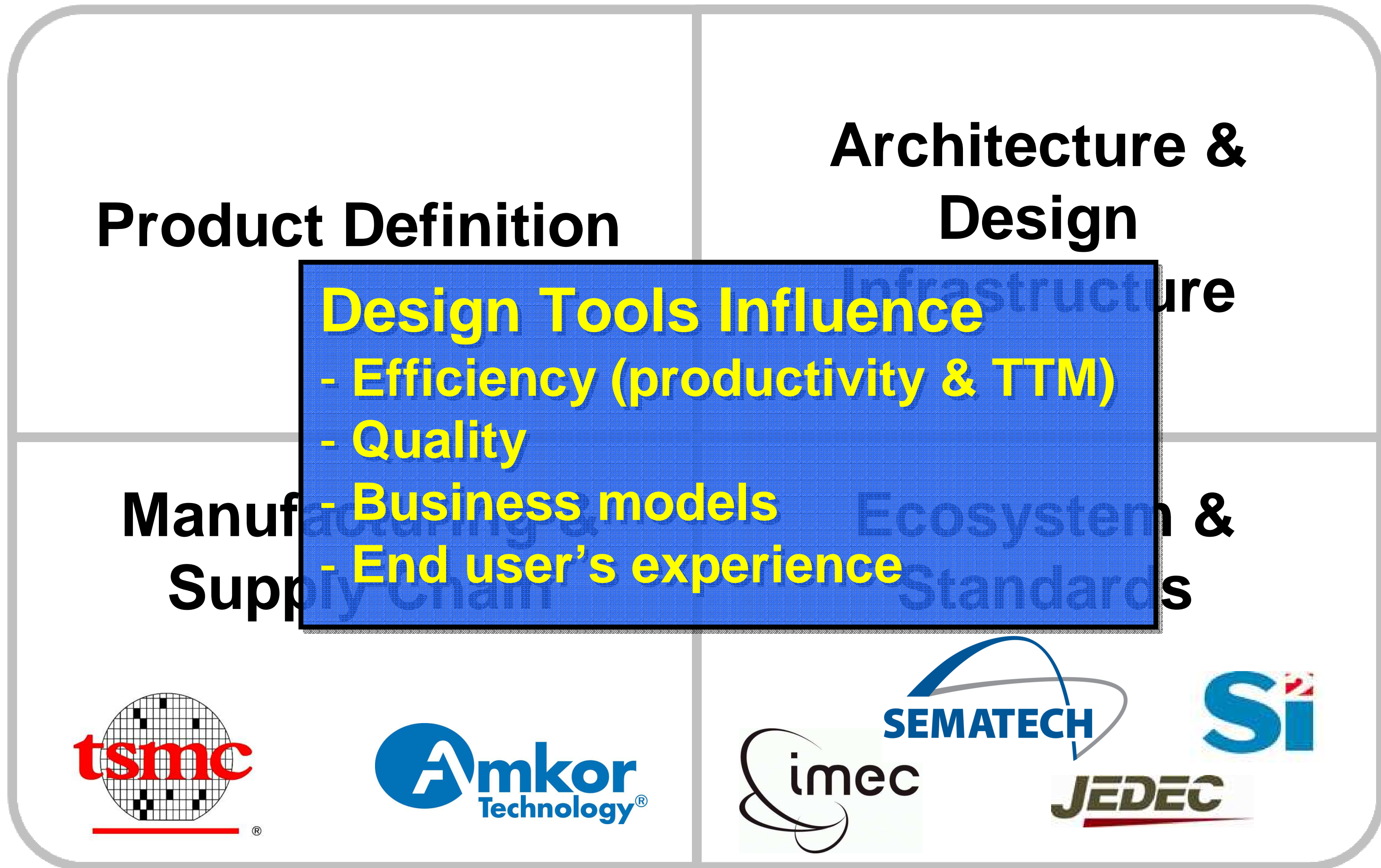
Altera’s Product Development Strategy



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Altera and TSMC Jointly Develop World's First Heterogeneous 3D IC Test Vehicle Using CoWoS™ Process

Altera Leveraging TSMC's CoWoS Manufacturing and Assembly Process for Development of Next-Generation 3D Devices

San Jose, Calif., and Hsinchu, Taiwan, March 22, 2012—Altera Corporation (Nasdaq: ALTR) and TSMC (TWSE: 2330, NYSE: TSM) today announced the joint development of the world's first heterogeneous 3D IC test vehicle using TSMC's Chip-on-Wafer-on-Substrate (CoWoS) integration process. Heterogeneous

CoWoS: Chip on Wafer on Substrate

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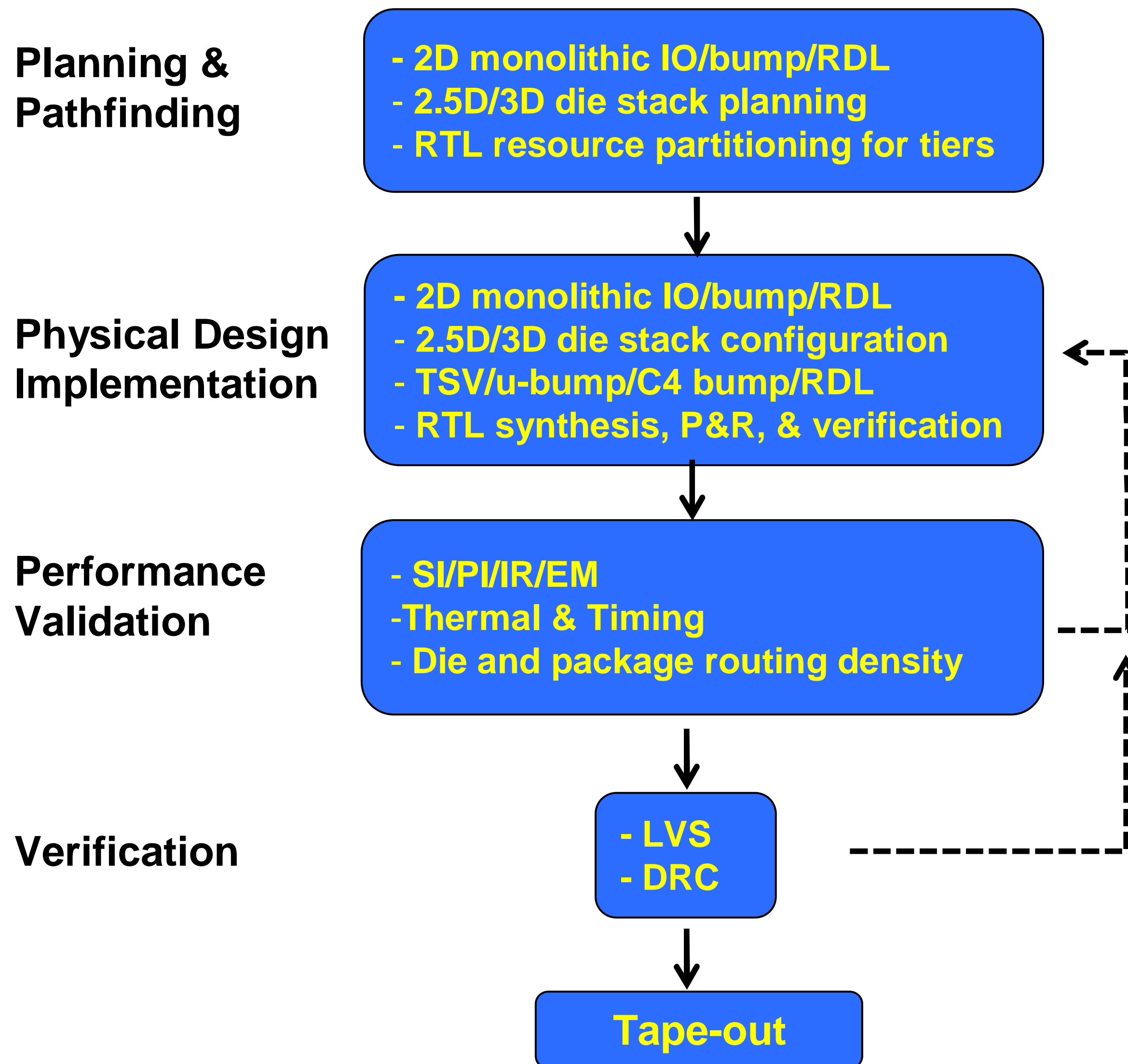
Desired EDA Flow for 3D Integration



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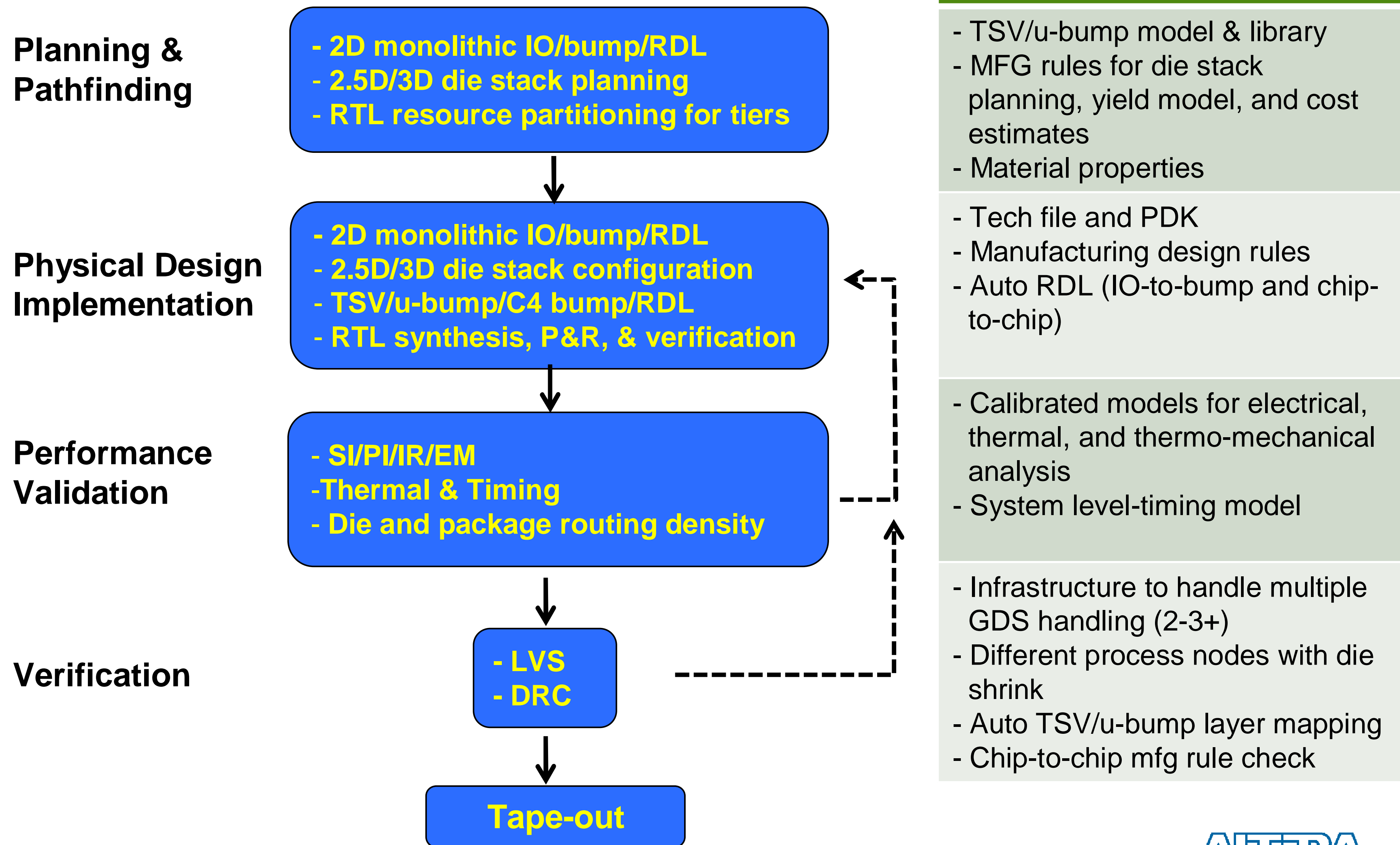
Desired EDA Flow for 3D Integration



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EDA Gaps

Flow exists | Existing flows can be adapted | Needs EDA support

Focus Areas	Path finding	Tier Design & Verification	Die Stack Verification and Perf. Validation
Design Partitioning & Chip-Package Co-Design			
Abstract Views			
Physical, Functional, and Timing Verification			
Connectivity Management			
SI/PI Analysis			
Thermal Analysis			
Thermo-mechanical Assessment			
Others: data exchange, scalability of database, etc.			

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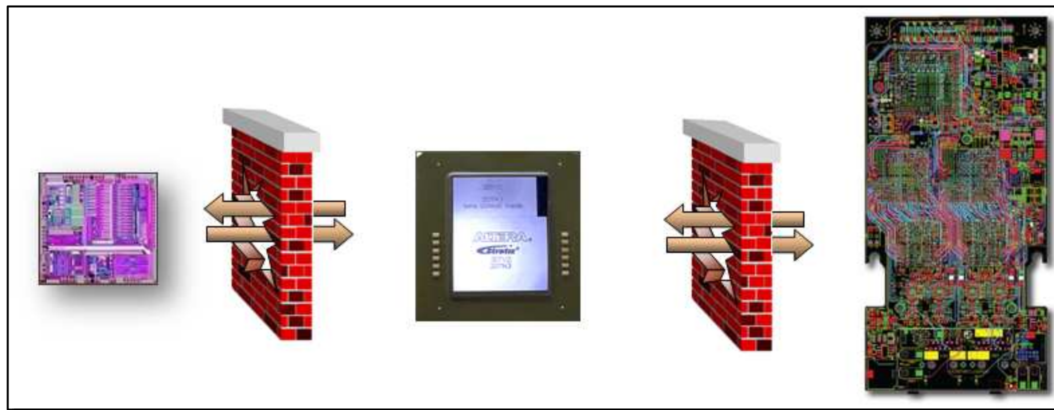
Pathfinding for Early Assessment

- Stacking configurations and chip-package interaction
  - System requirements => partitioning => tier requirements
  - Thermal and thermo-mechanical analysis based on macro models (effective material properties)



- 3D product specification
  - Architectural, functional, electrical, and test
  - Structural (intra-tier, inter-tier, and TSV/u-bump/bump planning)

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Pathfinding for Early Assessment (Gaps)

- Existing RTL-to-GDS and Die/Package co-design flows are too cumbersome for quick and cross-functional what if analysis

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Physical Design Implementation: Tier Planning

- Floor planning
  - Application mapping
  - Dependencies among application specific hard/soft IPs
  - Use model
- TSV, u-bump, and bump planning
  - Intra- and inter-tier connectivity and performance optimization
- Manufacturing and keep-out rules

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Physical Design Implementation (Gaps)

- DRC and LVS of individual tier and tier-to-tier interface (divide and conquer strategy)
  - Custom ad hoc methods invented on the fly vs. standard approach for tier-to-tier DRC/LVS
  - Challenges with multi-vendor or mixed-technology integration
- Visualization for debugging and FA
  - Navigating through different databases
- Managing database size and process shrinks

System Level Performance Validation (Gaps)

- Multi die power sign off is challenging due to large database sizes
  - Basic EDA infrastructure exists for abstracting die's (e.g CPM), but these are yet to evolve completely in mainstream flows
- Multi die STA is extremely challenging in 3D IC while complexity is manageable in 2.5D IC
- Multi die connectivity management for system level LVS
  - More convergence between IC schematics tools and SIP tools desired to bridge the gap between chip and system

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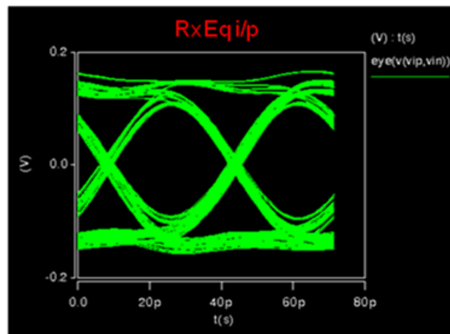
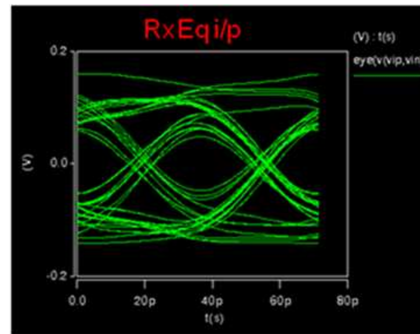
System Level Performance Validation (Gaps)

- Chip-to-chip timing closure: SPICE & STA
- Signal integrity analysis
  - TSV and chip-to-chip interconnect coupling and cross talk
  - High speed chip-to-chip signaling loss



High-speed IO – Monolithic Solution



High-speed IO – Through Interposer

- PDN and Thermal

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Future Trends

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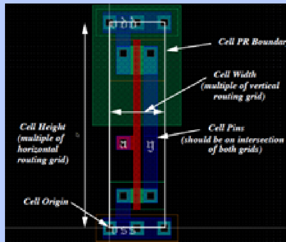
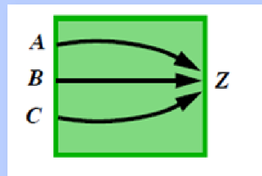
Extension of Existing Standards and Known Good Methods for Die-Stacking

Standard Cells

- ❑ Physical, Logical, & Abstract Views
- ❑ Timing, Power, & Parasitic
- ❑ GDSII, RTL,LEF, LIB, & TLF





Library Exchange Format (LEF)

Macro Pin Statement

```
PIN pinName
FOREIGN foreignPinName [STRUCTURE [pt [orient] ] ] ;
[DIRECTION {INPUT | OUTPUT [TRISTATE] | INOUT | FEEDTHRU} ;]
[USE { SIGNAL | ANALOG | POWER | GROUND | CLOCK } ;]
[SHAPE {ABUTMENT | RING | FEEDTHRU} ;]
[MUSTJOIN pinName ;]
{PORT
[CLASS {NONE | CORE} ;]
{layerGeometries} ...
END} ...
END pinName]
```

Macro Obstruction Statement

```
OBS
{ LAYER layerName [SPACING minSpacing | DESIGNRULEWIDTH value] ;
RECT pt pt ;
POLYGON pt pt pt pt ... ;
END
```

IP

- ❑ IP-XACT/IEEE Std 1685
  - Hardware information
  - Software views, file lists, protocol standardization
  - Describes the interface to IPs, but not functionality
- ❑ In many cases
  - tool centric
  - determined by customers

Stacked IC

- ❑ Design & verification of each tier & overall system
- ❑ Tier-to-tier interface
  - Electrical
  - Functional
  - Physical
  - Timing
- ❑ Data format
  - Verification
  - Thermal
  - Thermo-mechanical
  - Chip-package design

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Convergence in Manufacturing

- Die stacking approaches and design rules are converging
  - Flavors integration
  - TSV and micro-bump size and pitch
  - Wafer thickness, BEOL stack for 2.5D, RDL for 2.5D/3D, etc.
  - Standards: http://wiki.sematech.org/3D-Standards
- Enables economies of scale and faster adoption
  - EDA industry needs to be vocal

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Die Stacking is an Enabler for System-Level Integration

- FPGAs have been gradually incorporating system-level functions
- Die stacking provides unique business opportunities
  - Moving up in value chain
  - Time-to-market and product differentiations
- EDA tools need to evolve to support higher-level system integration enabled by die-stacking

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Thank You

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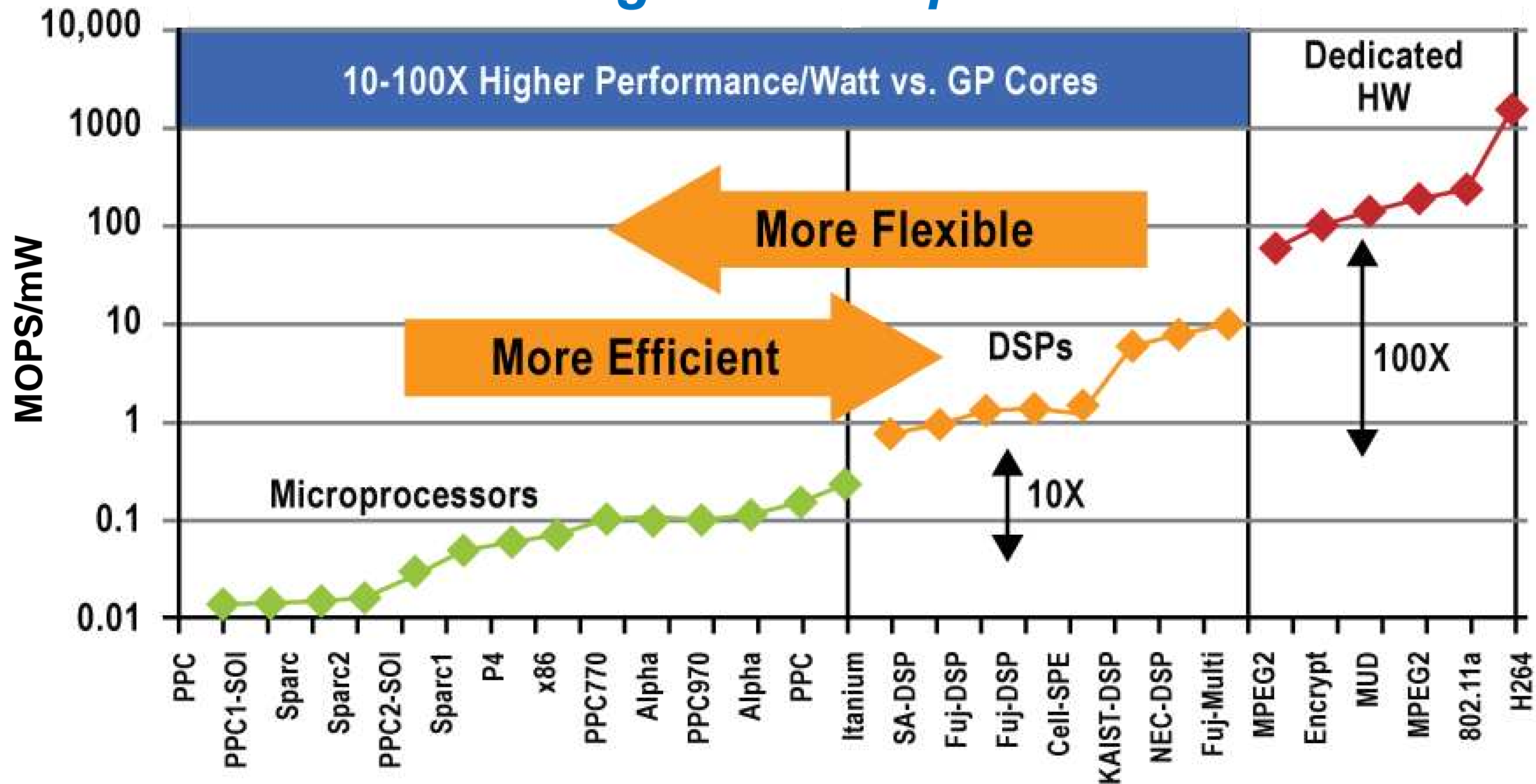
The Dilemma: Flexibility vs. Efficiency



Source: "High-performance Energy-Efficient Reconfigurable Accelerator Circuits for the Sub-45nm Era" July 2011 by Ram K. Krishnamurthy, Circuits Research Labs, Intel Corp.

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Altera at a Glance

Founded in Silicon Valley, California in 1983

Industry's first reprogrammable logic semiconductors

$1.95 billion in 2010 sales

2,600 employees

Leading supplier of FPGAs, ASICs and CPLDs

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