Power Aware Software: Is that all there is?

Electronic Design Process Symposium (EDPS) 2012

4-6 April 2012

Monterey

Thursday 5 April 2012: 1600

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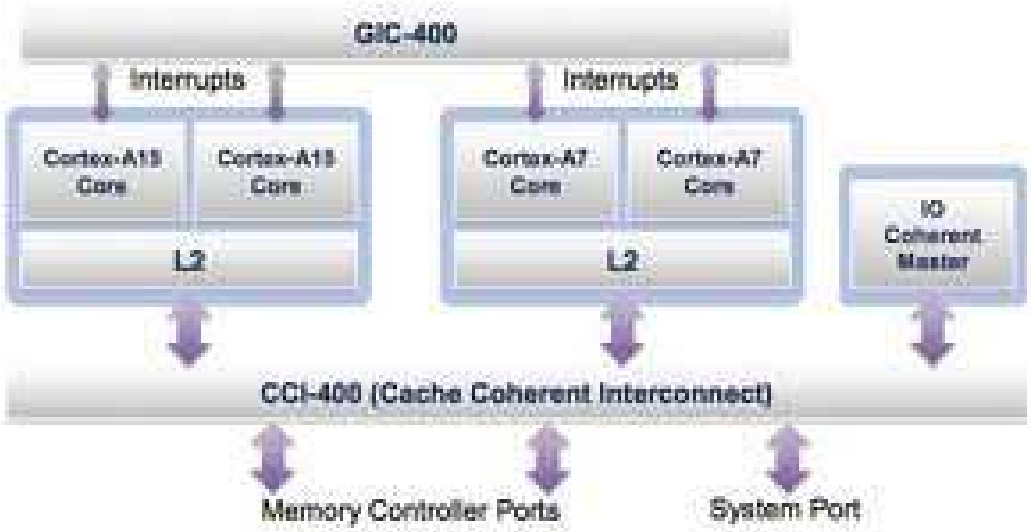
Outline

- Conventional Thinking
- Is that all there is?
- The Third Way
- Conclusions

Conventional Thinking



- ARM big.LITTLE, 2011

Conventional Thinking

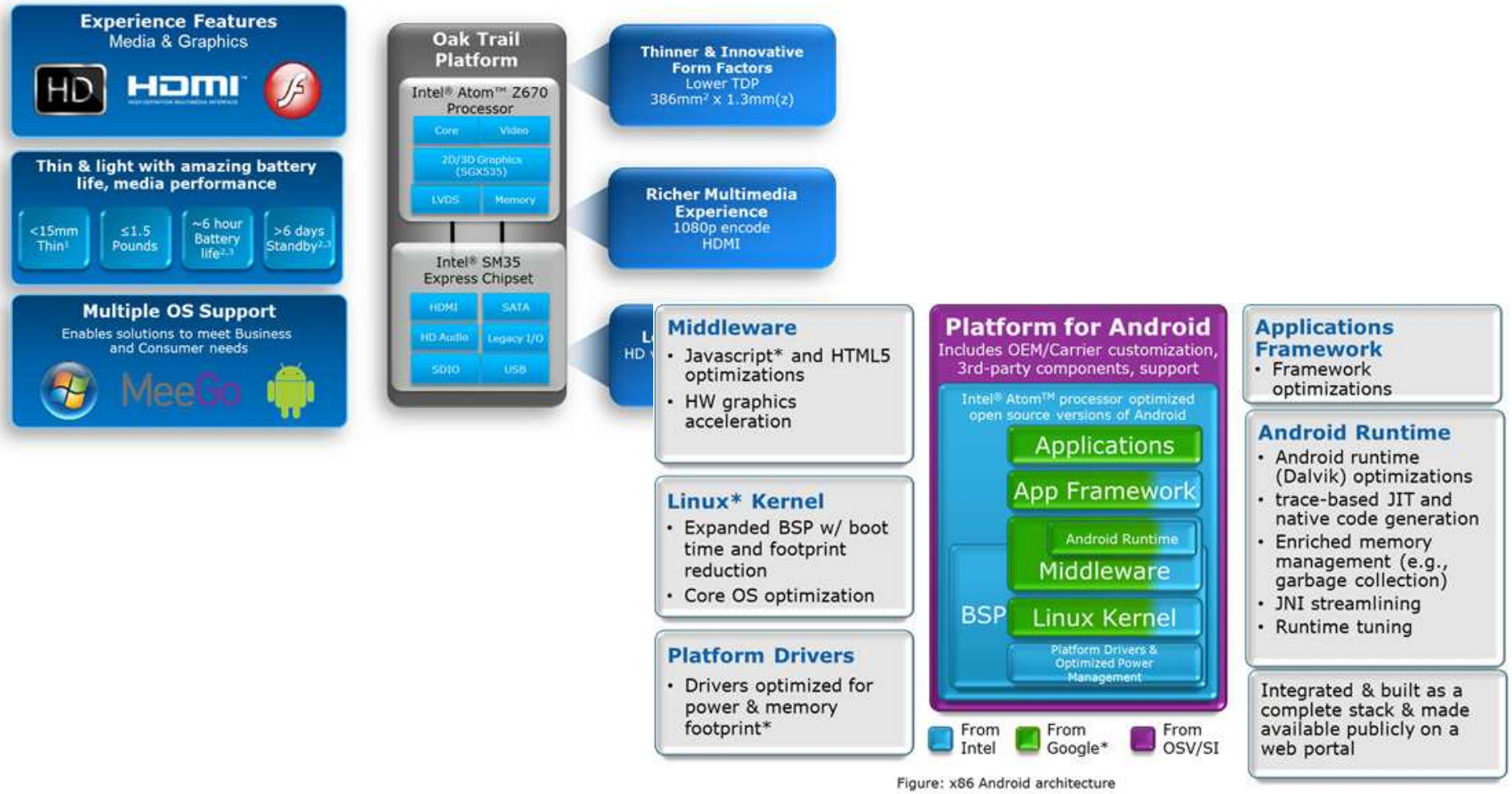
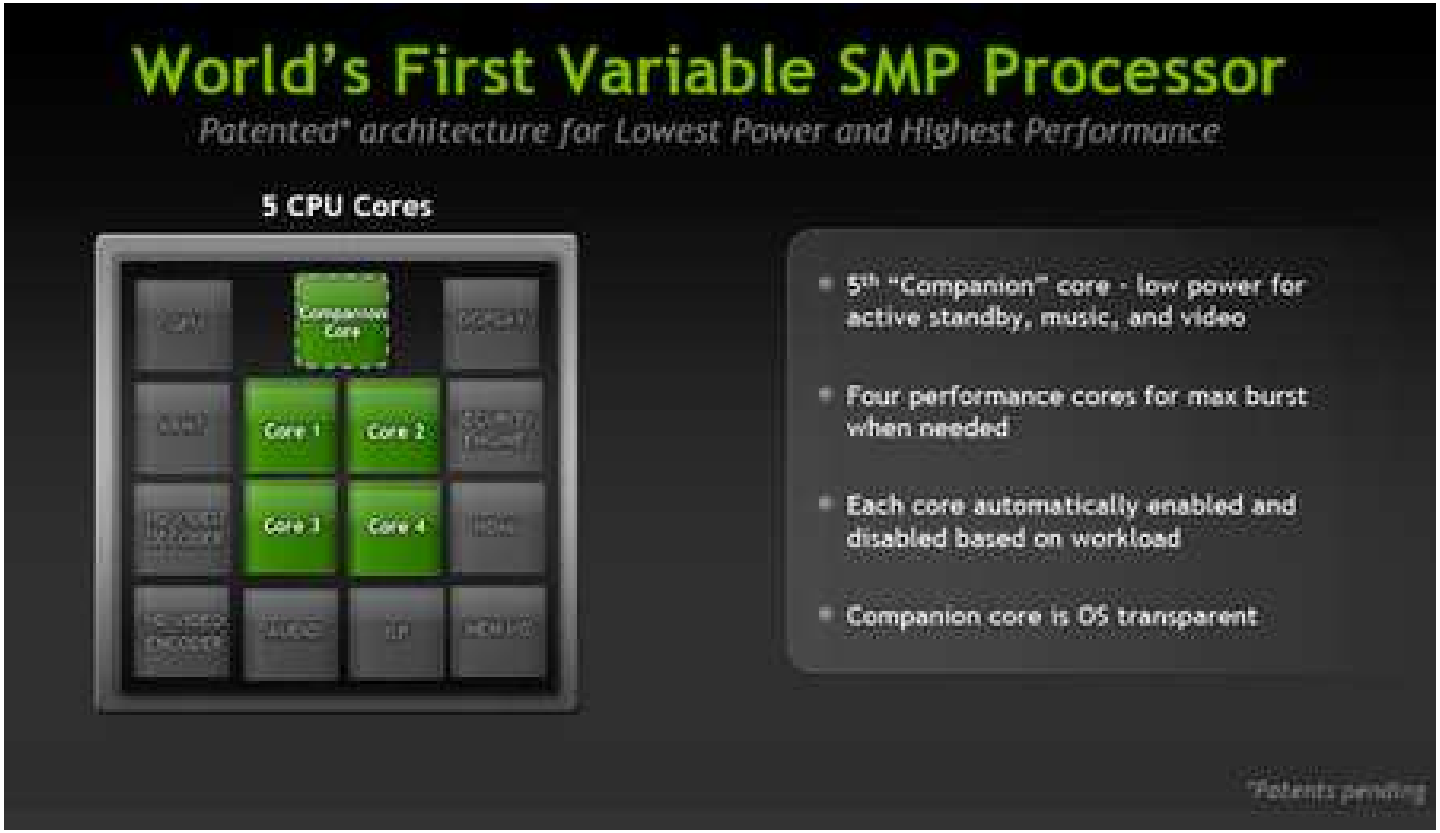


Figure: x86 Android architecture

- Intel Medfield processor tablet Atom-based platform, coming 2012

Unconventional Conventional Thinking



- Nvidia Tegra3 "Kal-El" (Krypton name for Superman)

Is that all there is?

……..

And so I sat there watching the marvelous spectacle.
I had the feeling that something was missing.
I don't know what, but when it was over,

Low-power

I said to myself, "is that all there is to a ▲ circus?

……..

-With apologies to Lieber and Stoller

-And Peggy Lee

Famille de Saltimbanques, Pablo Picasso, 1905

Stuck in the middle with you

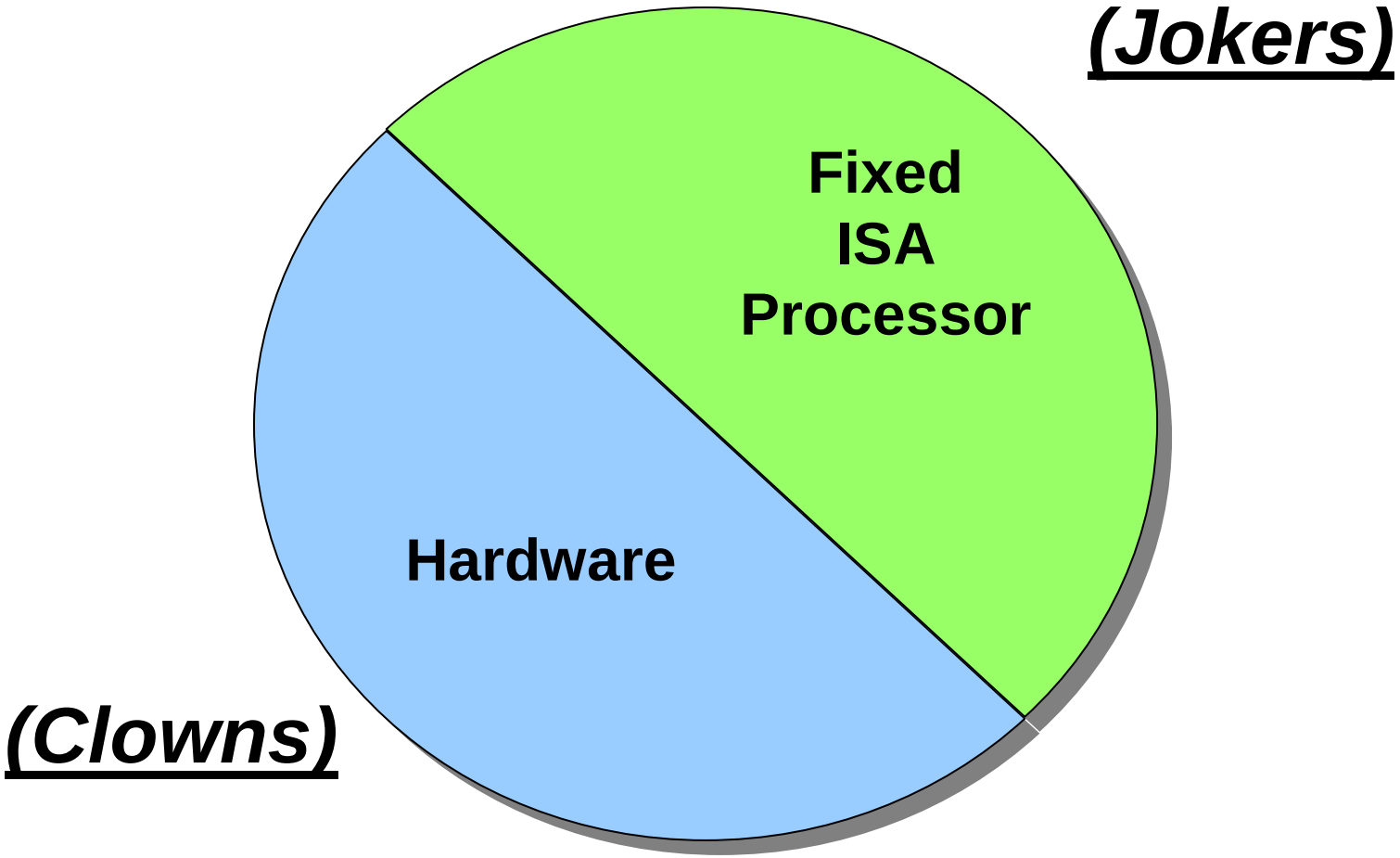
……

Clowns to the left of me,
Jokers to the right, here I am,
Stuck in the middle with you.

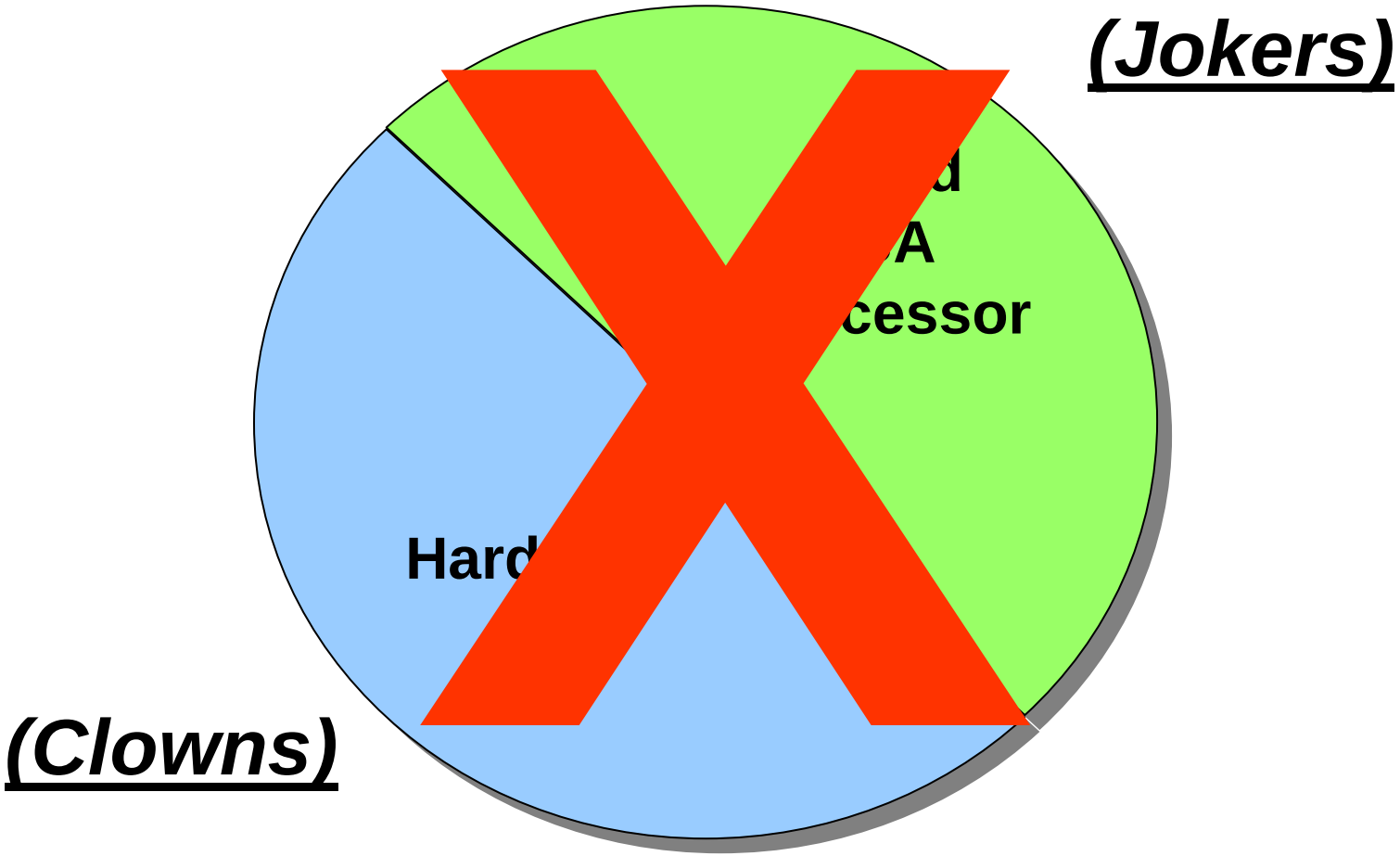
……..

- Gerry Rafferty and Joe Egan, *Stealers Wheel*

A false choice

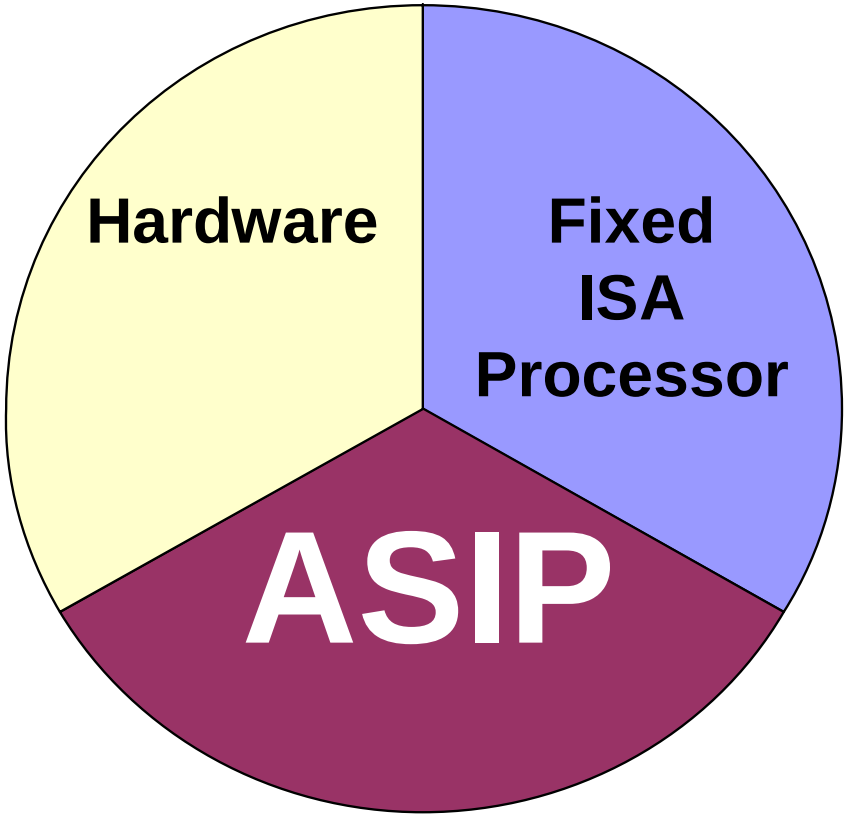


A false choice



Third Way:
Gallia Est Omnis Divisa in Partes Tres*

(Clowns)

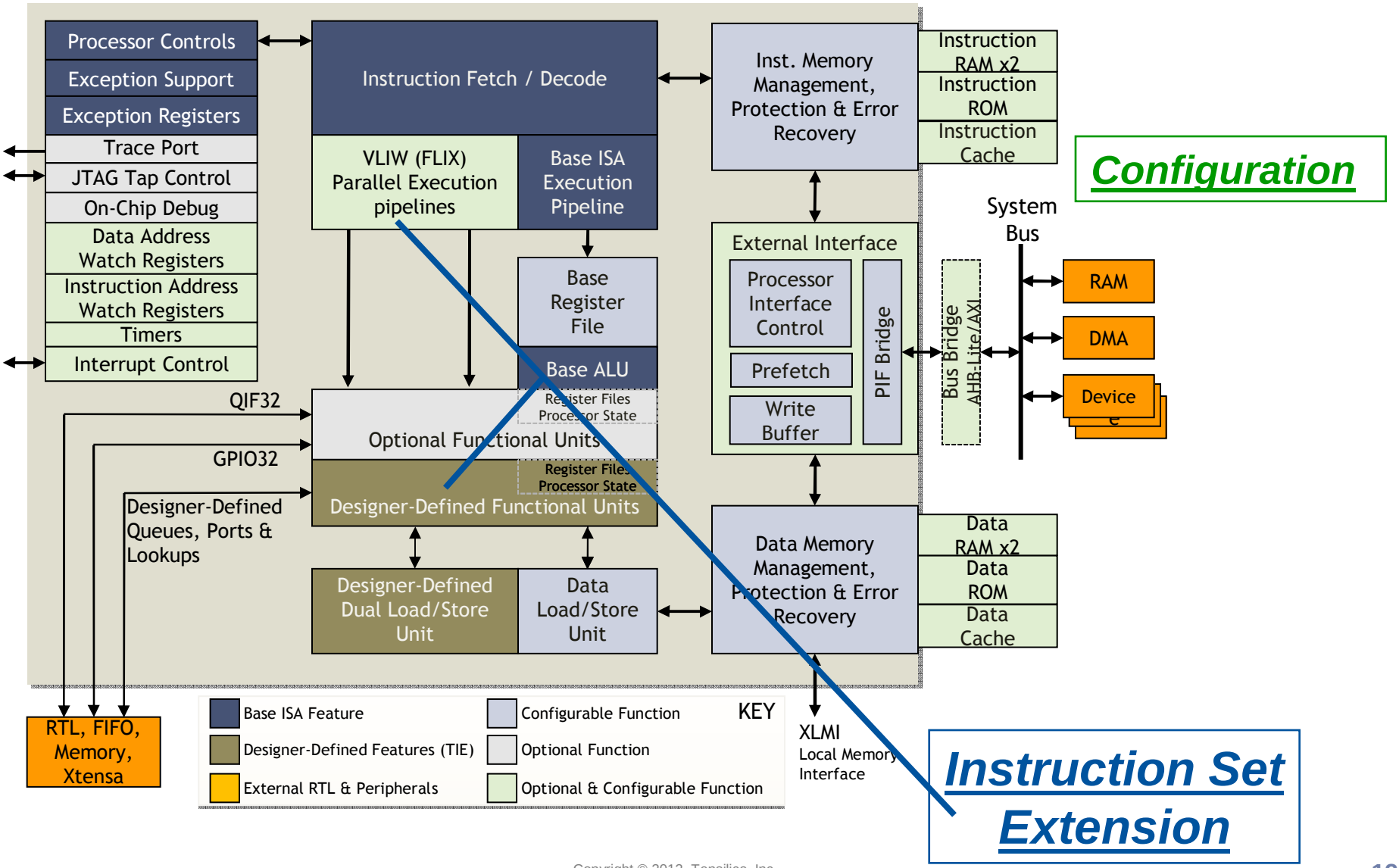


(Jokers)

(Stuck in the middle with you)

* ”All Gaul is divided into three parts”, Julius Caesar, *Commentarii de Bello Gallico*

ASIP: Application Specific Instruction set Processor Example



ASIP: Energy Saving via Application Specific Low Power Software

Application		Reference Processor Configuration	Optimized Processor Configuration	Energy Improvement
Dot-Product *2x2048 element vectors*	Area (mm2)	0.9	1.3	
	Cycles (K)	12	5.9	
	Power (mW/MHz)	0.3	0.3	
	Energy (µJ)	**3.3**	**1.6**	**2x**
AES *Advanced Encryption Standard*	Area (mm2)	0.4	0.8	
	Cycles (K)	283	2.8	
	Power (mW/MHz)	0.2	0.3	
	Energy (µJ)	**61.1**	**0.7**	**82x**
Viterbi *Trellis Decoding*	Area (mm2)	0.5	0.6	
	Cycles (K)	280	7.6	
	Power (mW/MHz)	0.2	0.3	
	Energy (µJ)	**65.7**	**2**	**33x**
FFT *256 point complex*	Area (mm2)	0.4	0.6	
	Cycles (K)	326	13.8	
	Power (mW/MHz)	0.2	0.2	
	Energy (µJ)	**56.6**	**2.5**	**22x**

Low Power Audio

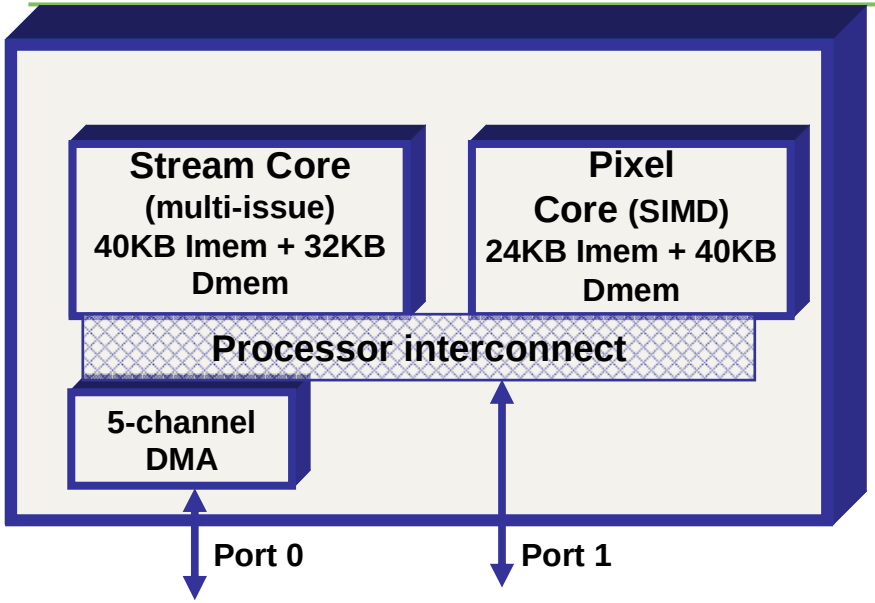
Codec	Average MHz	Measurement conditions
HiFi 2 MP3 Decoder	5.7	44.1 kHz / 128 kbps (stereo)
HiFi 2 MP3 Encoder	26	44.1 kHz / 128 kbps (stereo)
HiFi 2 AAC-LC Decoder	8.1	48 kHz / 128 kbps (stereo)
HiFi 2 AAC-LC Encoder	37.8	44.1 kHz / 128 kbps (stereo)
HiFi 2 WMA Decoder	10.3	44.1 kHz / 128 kbps (mid-rate, stereo)

Real-time MP3 decode power @ 5.7 MHz

Example Power = 0.13 mW

21 μW/MHz dynamic power running MP3 decode, gate-level simulation with post-layout RC. 7.5 μW leakage power. 40 LP process, Typ Op. Cond. 0.91 v; Core Area: 0.110 mm2 – logic area for a power-optimized Xtensa w/ HiFi 2

Low PowerVideo

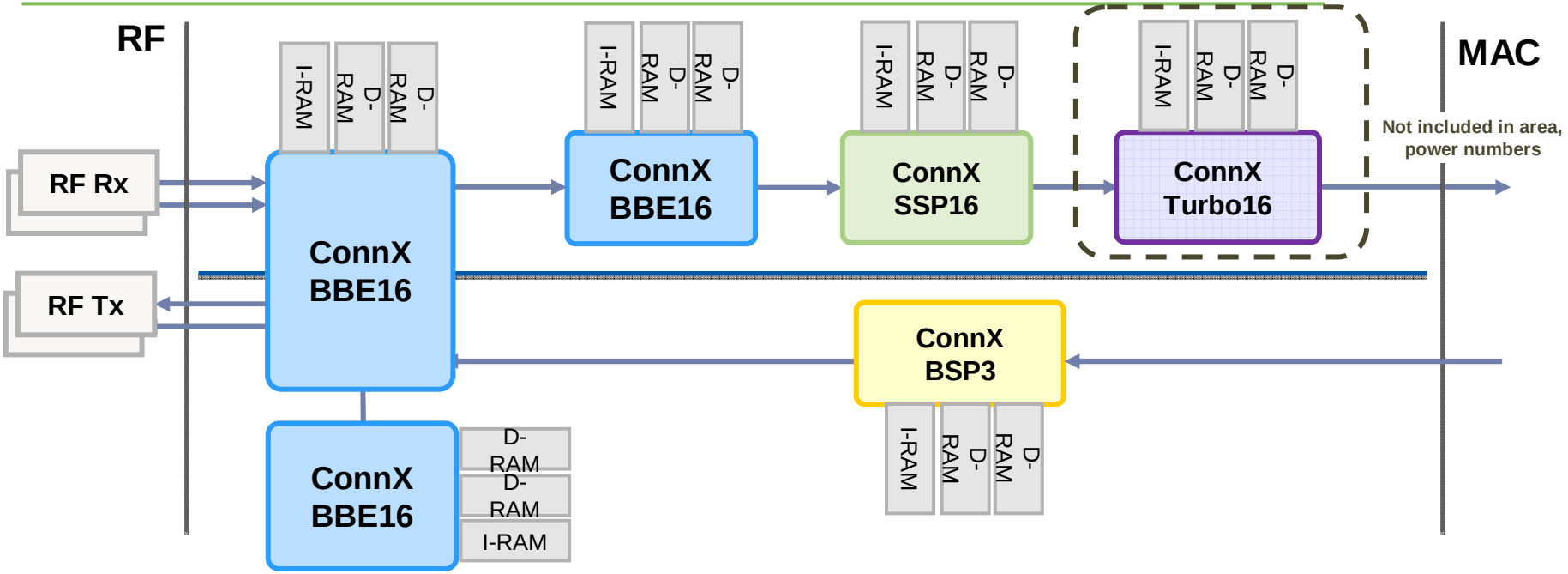


	Coding Standard	Pixel Rate	Bit Rate	Processor Power *
Decode	**H.264 Main and Baseline Profile**	**D1**	**5 Mbps**	**47 mW**
	VC-1/WMV9 Main Profile	**D1**	**6 Mbps**	**50 mW**
	MPEG-4 Advanced Simple Profile	**D1**	**6 Mbps**	**35 mW**
	MPEG-2 Main Profile	**D1**	**8 Mbps**	**38 mW**
Encode	**MPEG-4 Advanced Simple Profile**	**D1**		

* Includes all processor power sinks: logic, SRAM, clock tree, and leakage, measured with Synopsys Power Compiler on a TSMC 90G layout netlist generated with Virage standard cell and SRAM libraries for a simulation of decoding the Akiyo sequence with 32 cycles main memory access latency

Low Power Baseband: LTE UE PHY

LTE CAT4 150Mbps DL – 50Mbps UL (Actual Implementation)



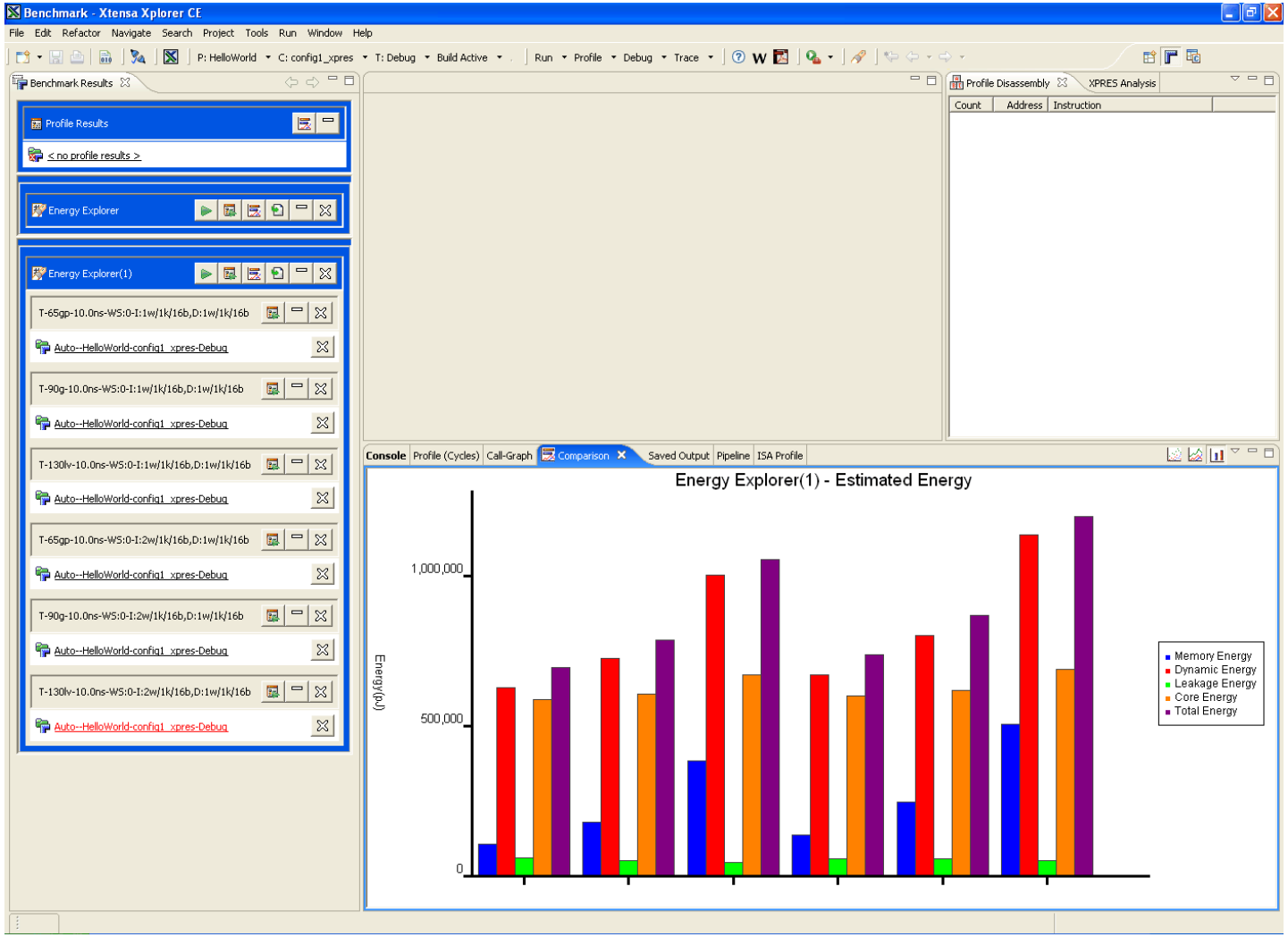
40LP AREA	Tensilica	
DSP's	2.262	2 x BBE16 @ 300MHz; 1 BBE16 @ 100MHz
Other Core's	0.492	SSP16 (@300MHz)
Other Core's	0.179	BSP3 (@200MHz)
DMA's	0	SSP16 does this
HW blocks	0	
Core Size mm2	**2.933**	
Total (Core + Memory)	**5.259**	

40LP POWER	Tensilica (Core + Memory)	
DSP's	182.89	2 x BBE16 @ 300MHz; 1 BBE16 @ 100MHz
Other Core's	36.97	SSP16 (@300MHz)
Other Core's	20.77	BSP3 (@200MHz)
DMA's	1.2	SSP16-DMA (@30MHz)
HW blocks	0	
Total power mW	**241.83**	

Core area is cell area

Area and power numbers do not include core memories, based upon average MHz numbers

Tools for low power software – ISA "energy space exploration"



Conclusions

- Conventional thinking about low power software and architectures is good as far as it goes
  - But it doesn't go far enough
- ASIPs bring new energy space tradeoffs for low power software
  - ASIPs can be mixed into conventional architectures
  - Especially useful for the low power software dataplane
  - Used strategically, ASIPs complement conventional Fixed ISA processors and hardware
- Advanced compiler technology on ASIPs reduce the work required to write low power software
  - Automatic instruction inference
  - Automatic vectorisation – SIMD instructions
  - Can work with conventional C datatypes
- ASIPs are a design technology that should be in every system architect, SW architect, HW architect and low power design team's toolkit