INVENTIVE

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Low Power Design: Is the Problem Solved?

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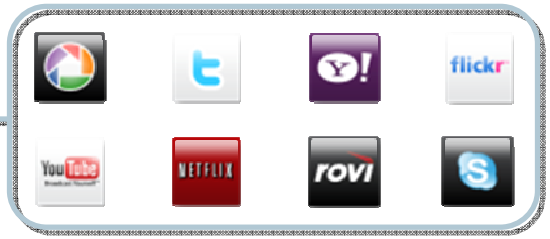
Key Drivers

- Apps
- Video
- Mobility
- Cloud
- Green Tech



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Low Power Design Issues Impact Profitability

Different Drivers in Different Verticals

Mobile/Hand-held

Battery Life
Unit Cost (chip package)

Consumer/Digital Home

Unit Cost (chip package)
Unit Cost (fans etc.)
Reliability

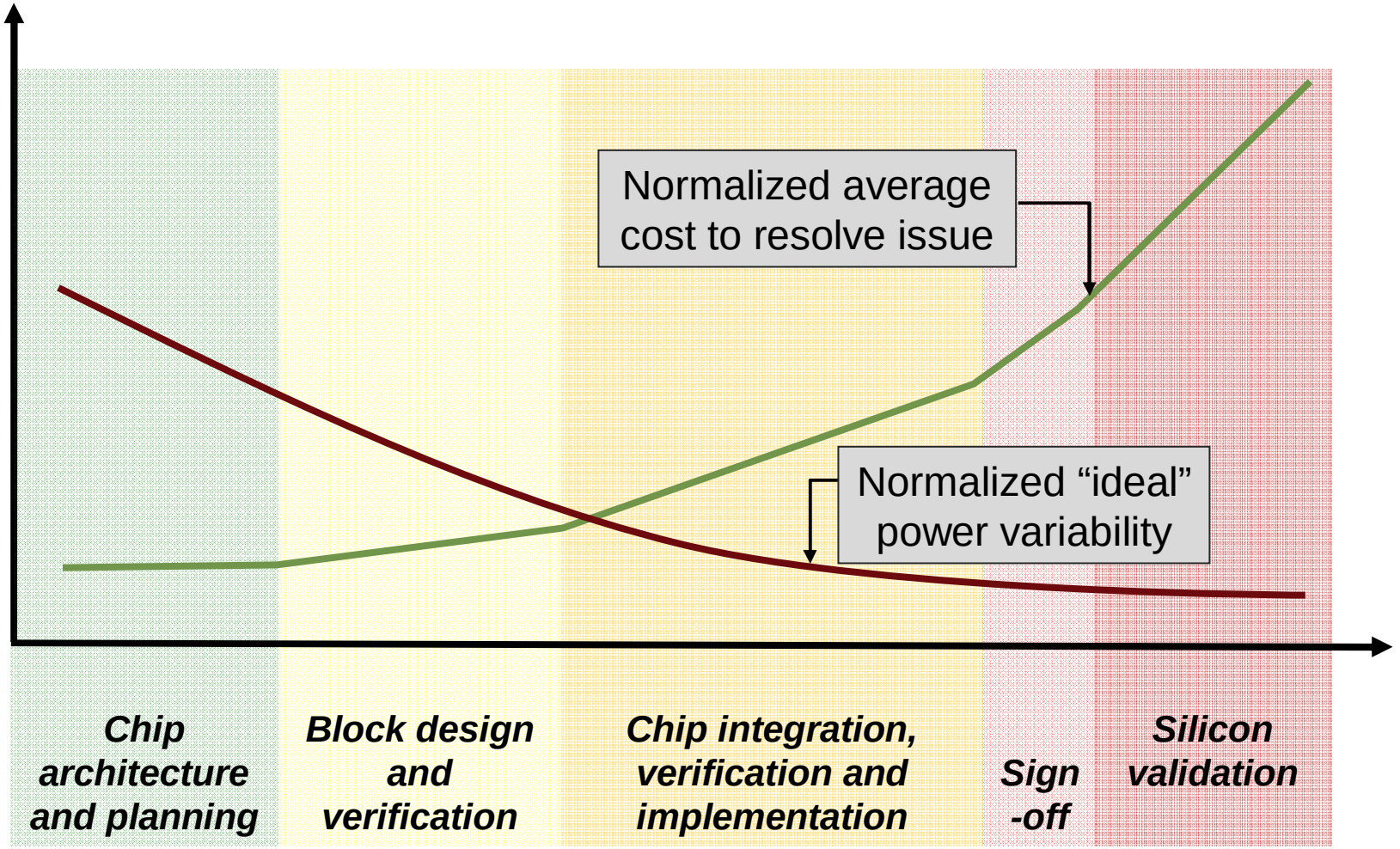
Network/Data Center

Power Efficiency
Total Cost of Ownership
Reliability
Green

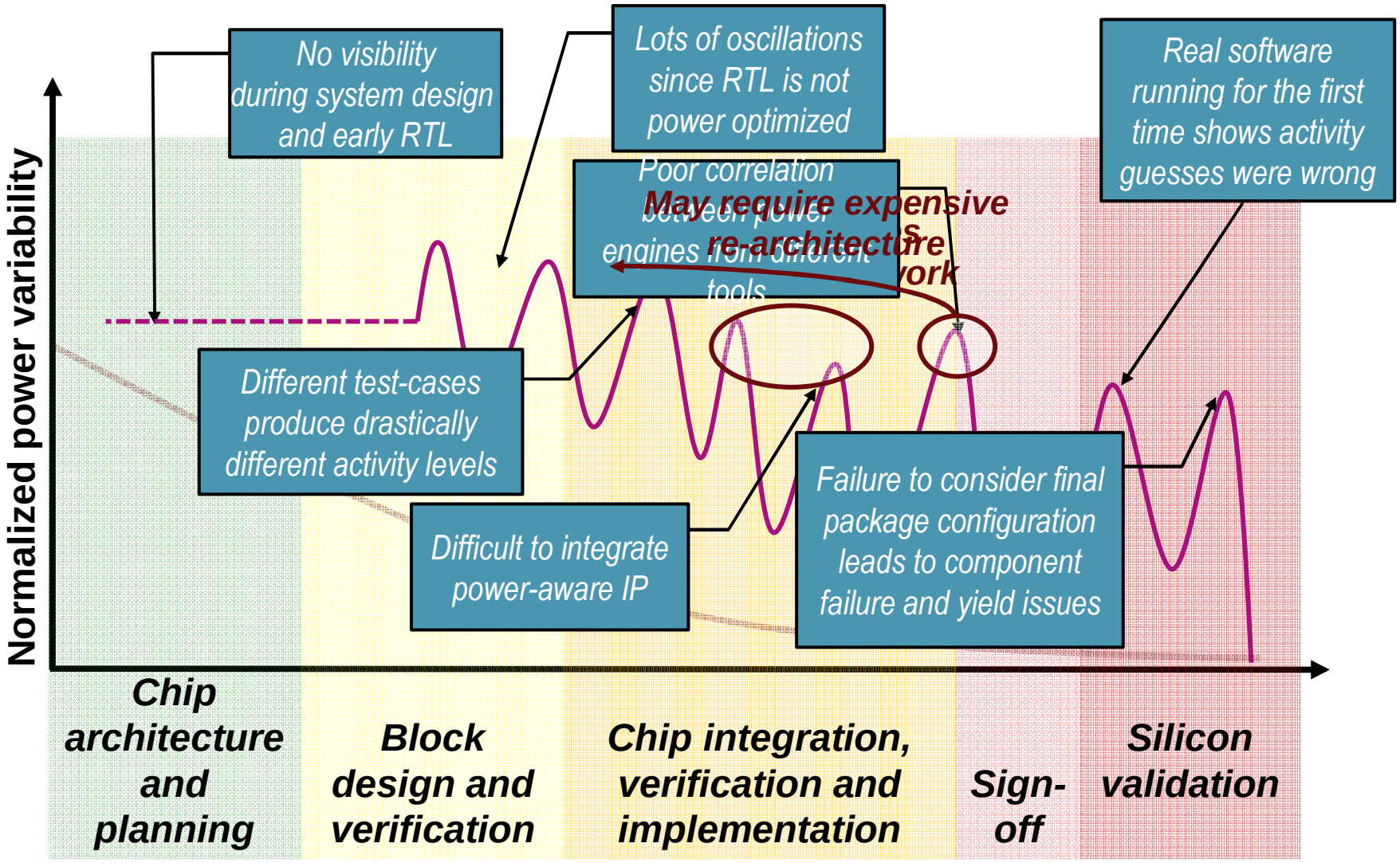
Low power requirements drive different design decisions:

- Product design architecture and integration decisions
- IP make versus reuse versus buy decisions
- Manufacturing process decisions

Power Closure in Design Flow

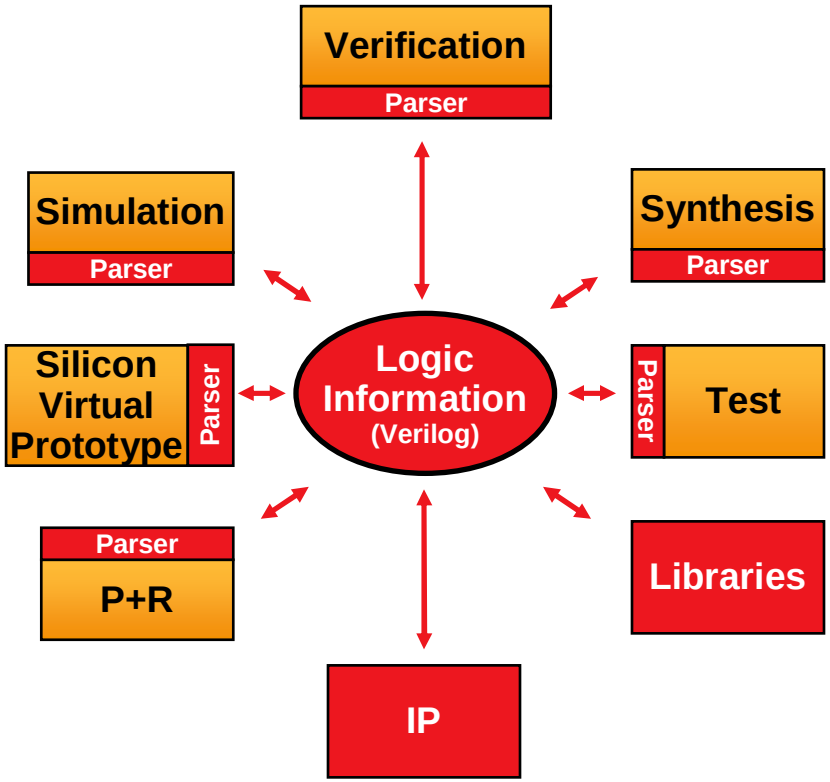


Power Closure Challenges



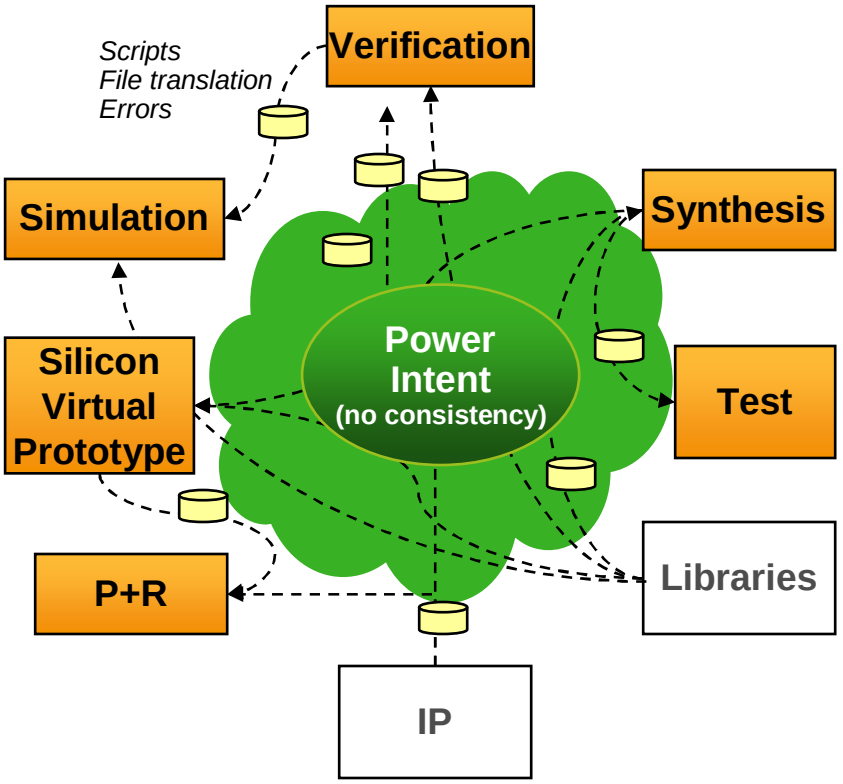
Low Power Design 5 Years Ago

Logic is "Connected"



Can be Automated

Power is Not "Connected"



Very Difficult to Automate

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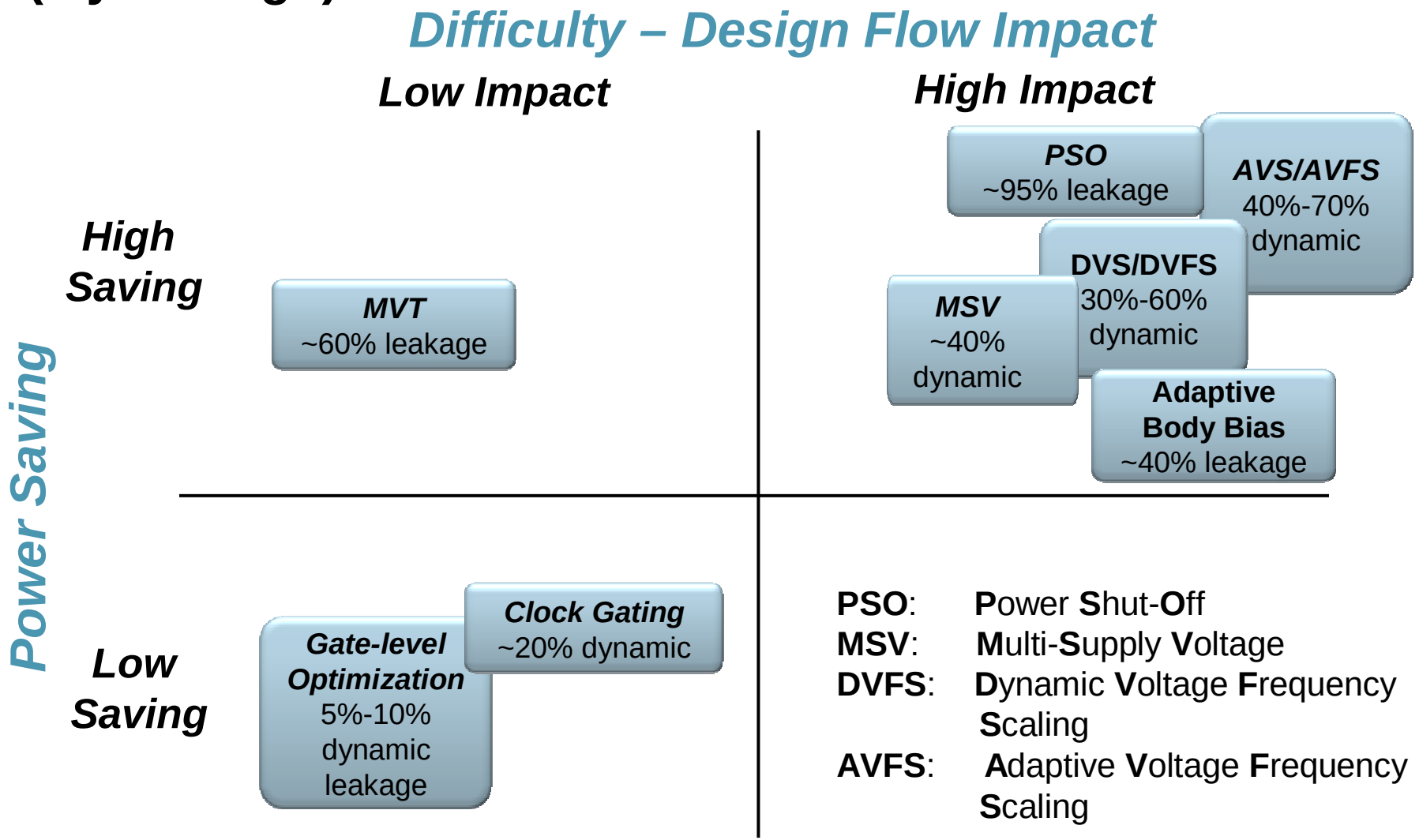
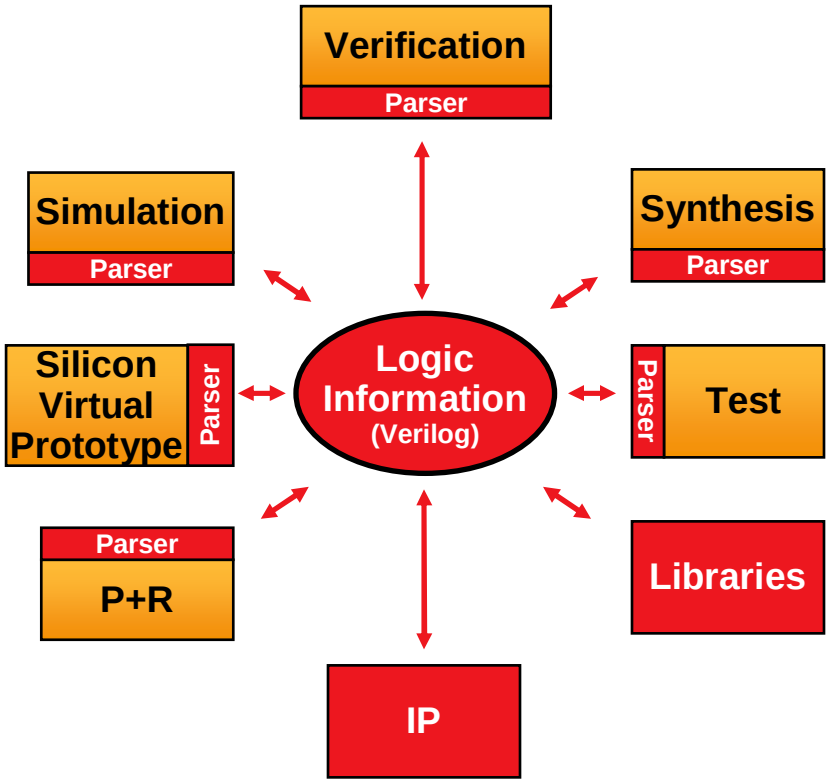
Popularity of Low Power Design Techniques
(5 years ago)



PSO: **P**ower **S**hut-**O**ff
MSV: **M**ulti-**S**upply **V**oltage
DVFS: **D**ynamic **V**oltage **F**requency **S**caling
AVFS: **A**daptive **V**oltage **F**requency **S**caling

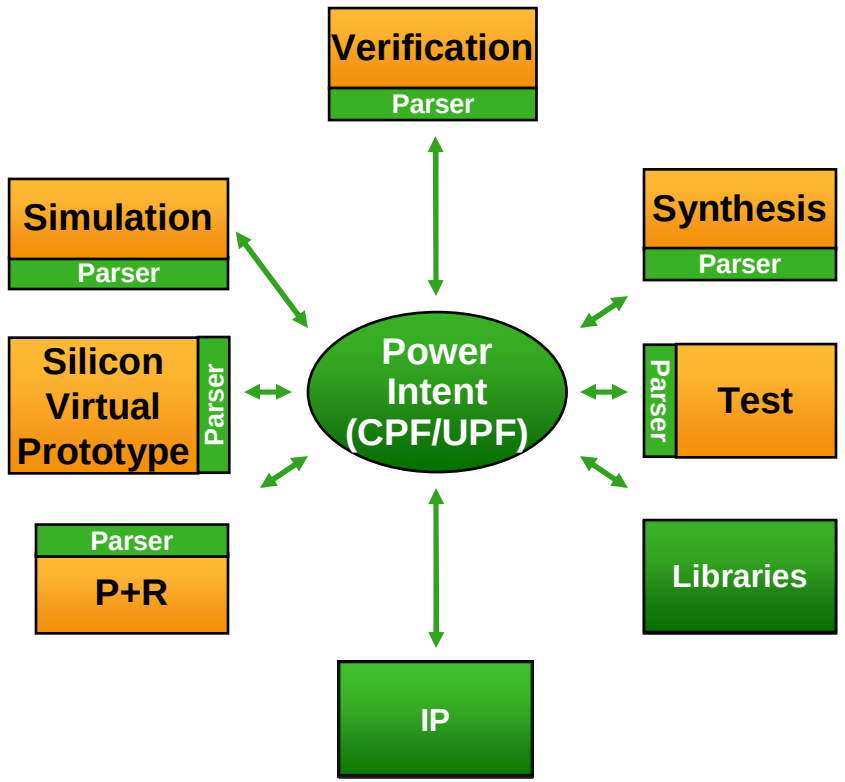
A New Low Power Design Methodology

Logic is "Connected"



Is Automated

Power is Connected



Is Automated

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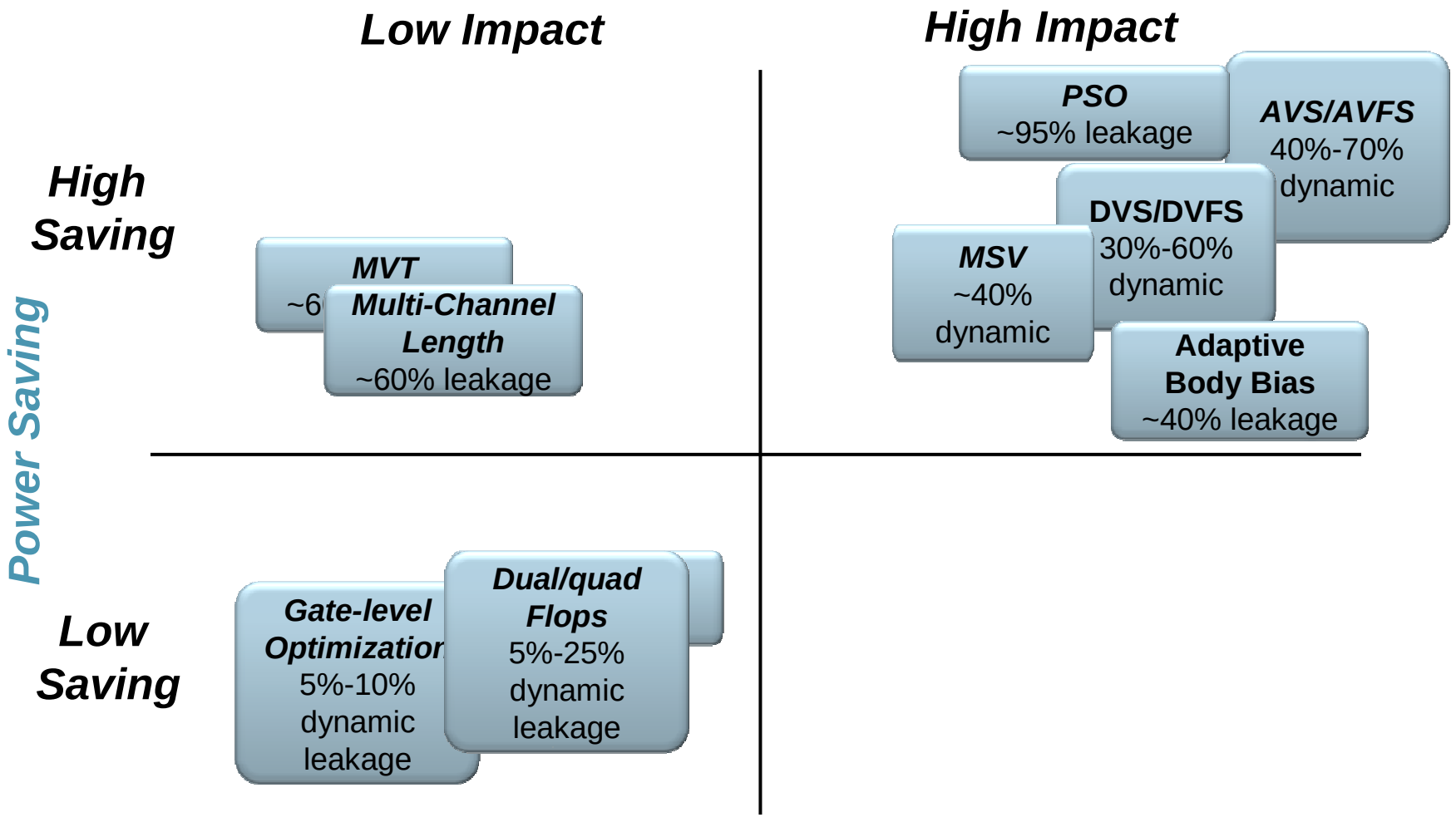
Popularity of Low Power Design Techniques (now)



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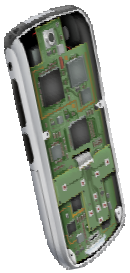
What's Next?

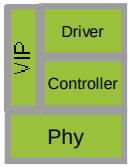
SYSTEM REALIZATION

TLM/SW Power
Modeling and Estimation



SOC REALIZATION

IP Macro Model
Integration Ready IP



SILICON REALIZATION

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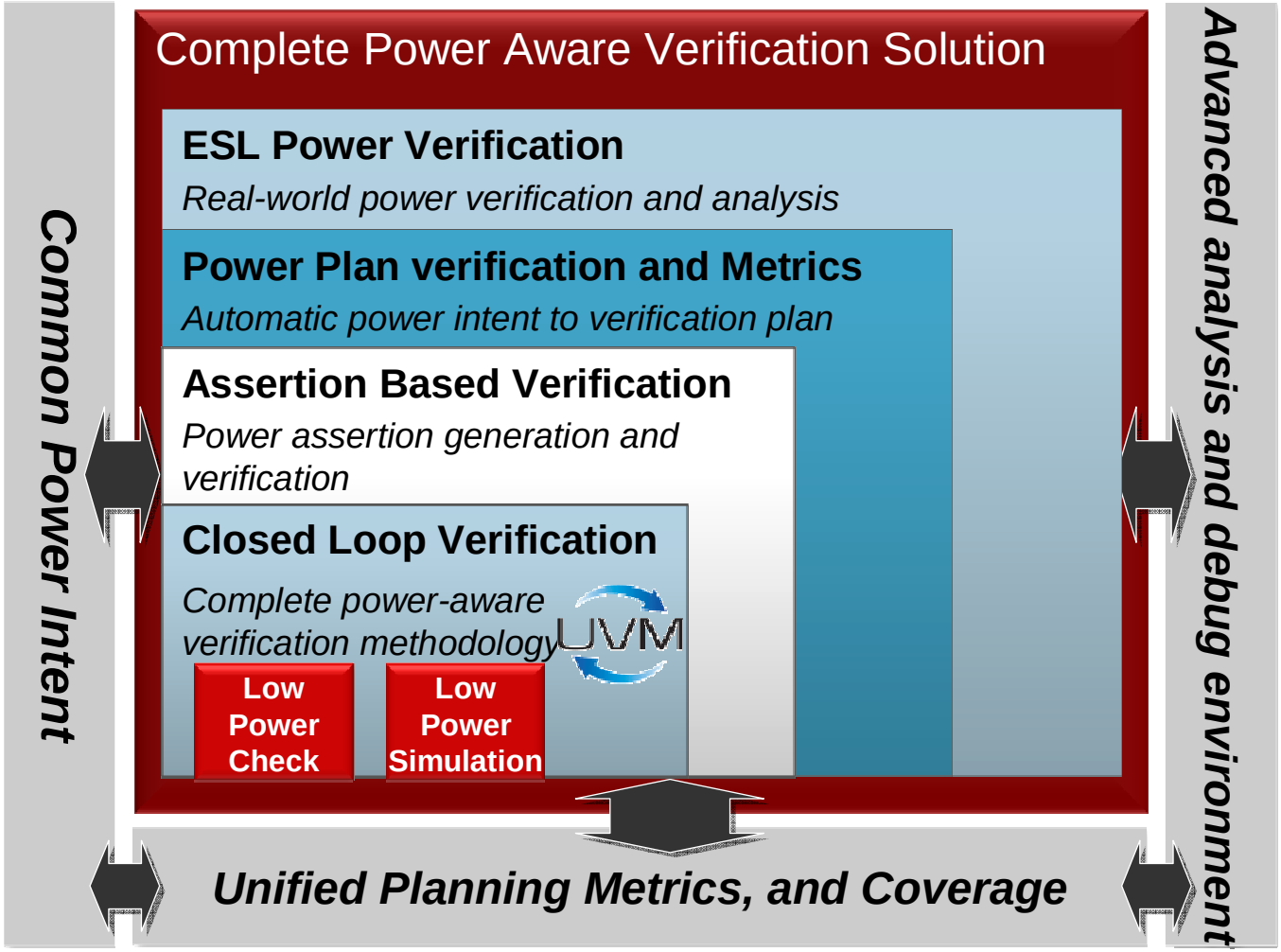
Methodology Is the Key

A Closer Look on Low Power Verification



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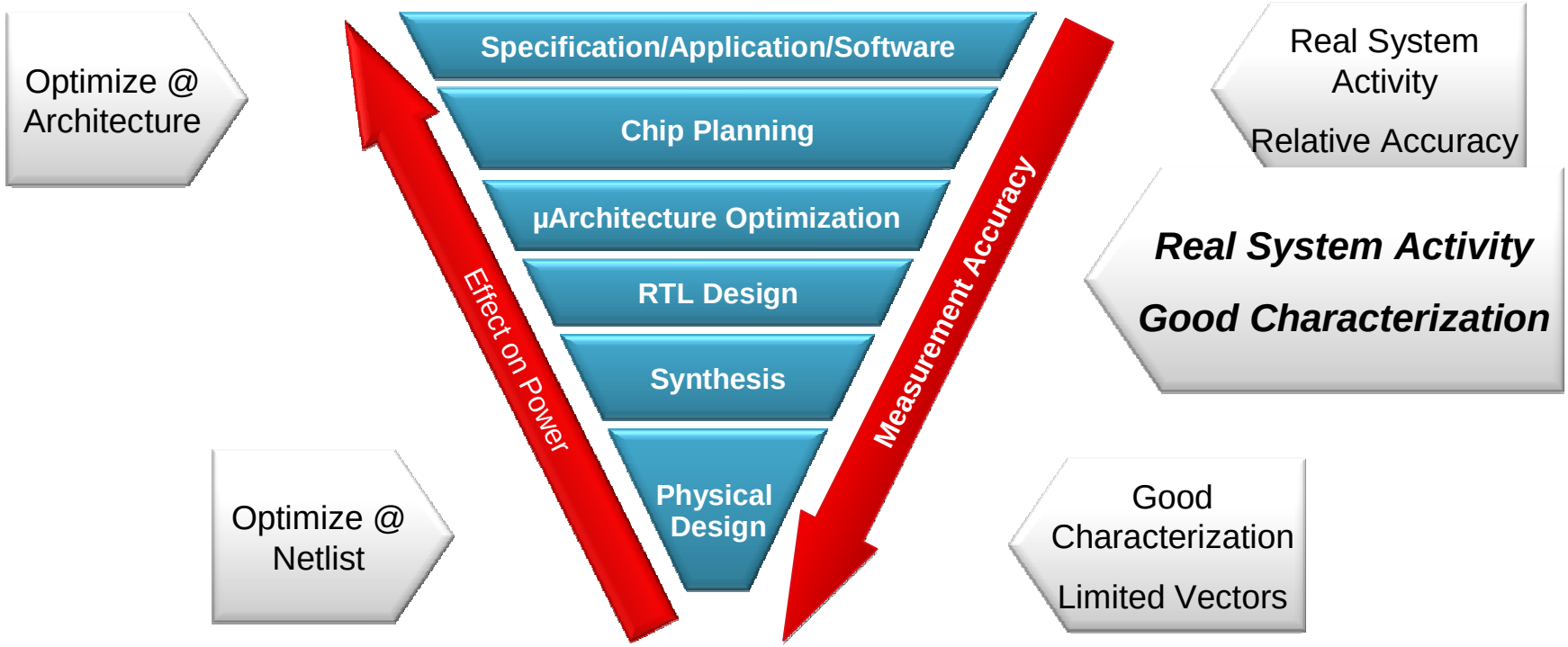
Early Architecture Challenge: Power Predictability

Predictable Estimation, Analysis & Optimization



How to ***predictably***

Estimate total power?

Optimize performance/watt?

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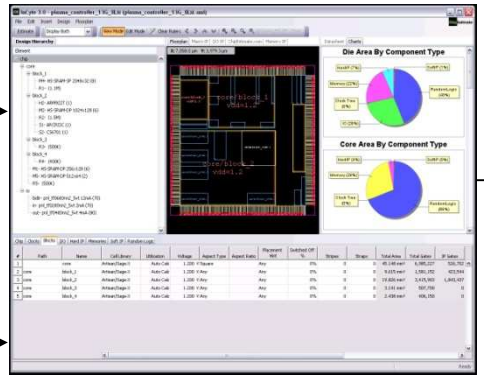
System-Level Low Power Solution

1. Power Exploration (Chip Planning Solutions)

Design Specification
- Power architecture
- Power domains
- Low-power plan
- Standby, talk

Technology Libraries



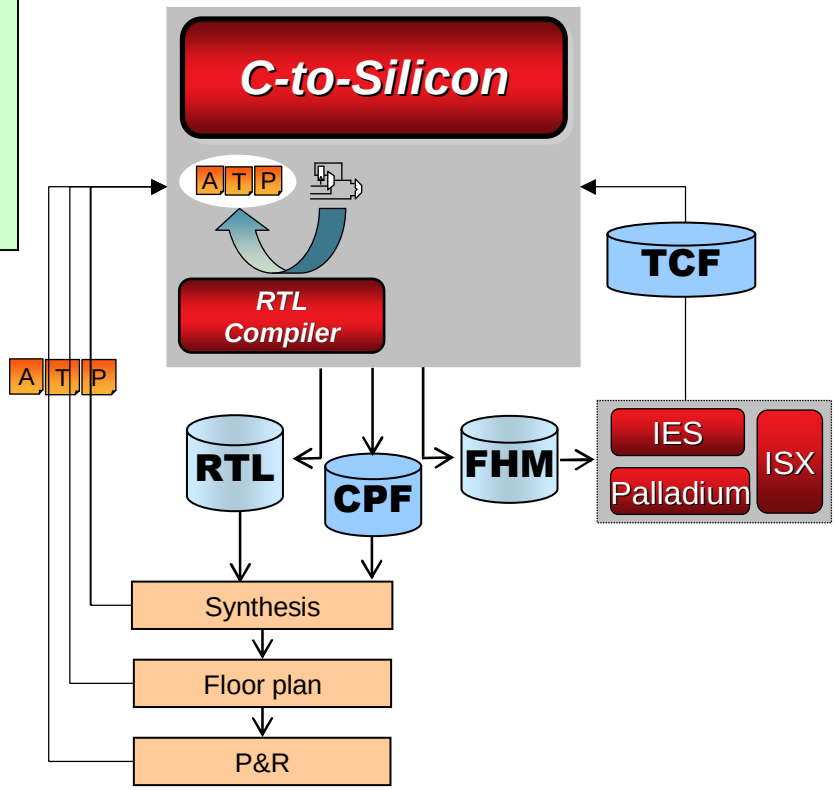
Estimation Results

Power (Dynamic, Static)

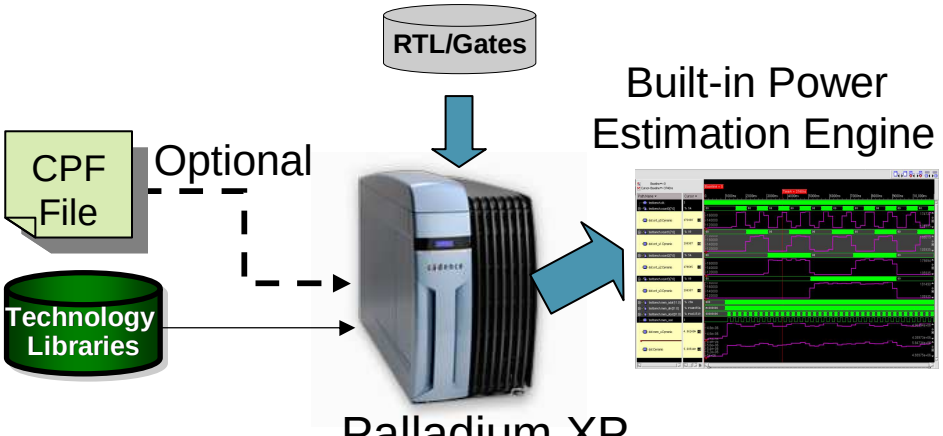
CPF Generation

Power planning (Exploration)

2. TLM IP Power estimation and optimization



3. Dynamic Power Analysis (SoC + SW) Average and peak power window



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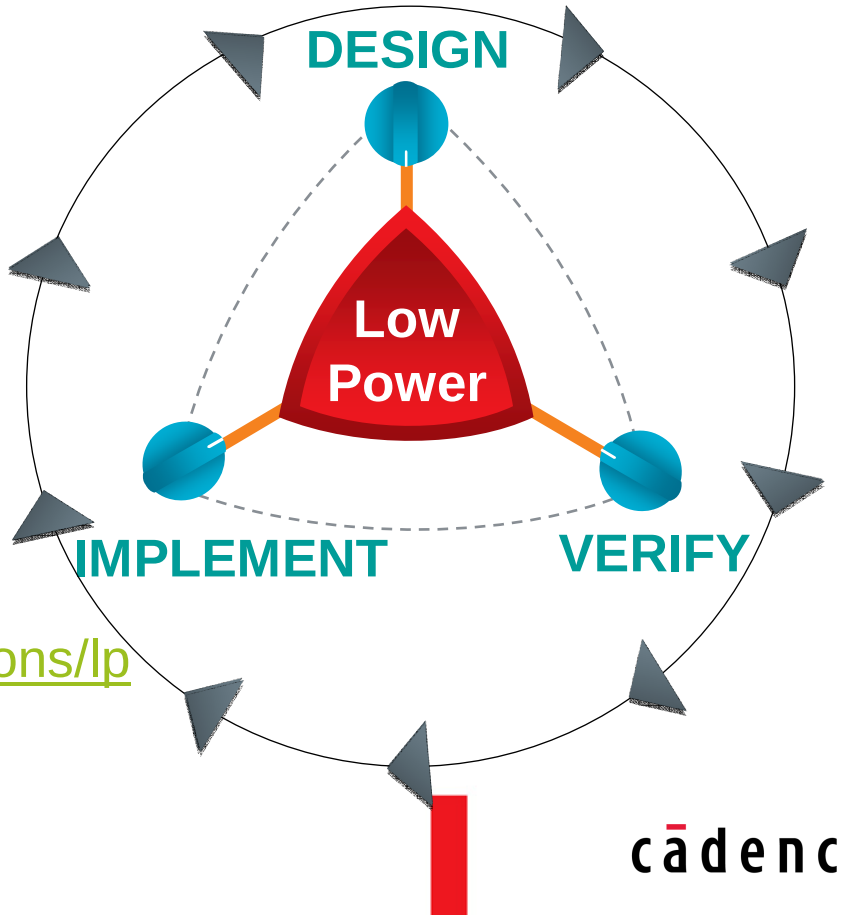
Conclusion

- Low power design is a “system” problem
- Methodology is key to successful low power design
  - Repeatable
  - Scalable
  - Predictable
- Future of low po ign
  - System/SoC Realization
  - Silicon Realization
- Resources
  - www.powerforward.org
  - www.eda360.com
  - http://www.cadence.com/solutions/lp

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