

EDP 2012  
The Power Chart

ELECTRONIC DESIGN STRATEGY & MARKET ANALYSIS

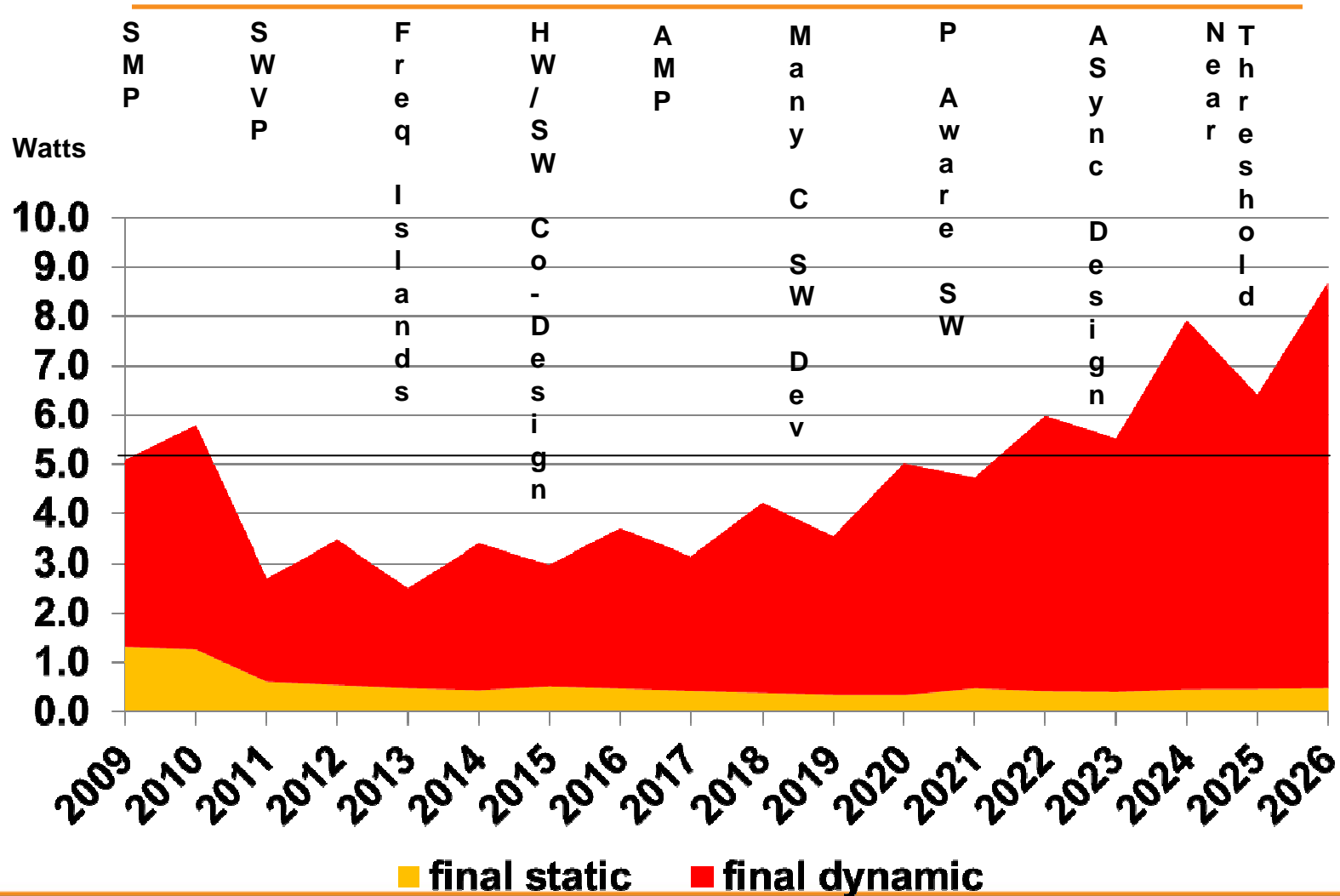
[www.garysmithEDA.com](http://www.garysmithEDA.com)

# 2011 Power Survey Results

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- Average high-end mobile SoC gate count was 104 million gates.
- The average frequency of a low-end cell phone was 400 MHz, for a high-end phone 800 MHz.
- Targeted Average frequency was 400 MHz, highest frequency was 1.2 GHz.
  - **Some reports of packaging limiting the frequency to 1.2 GHz.**

# Q1 2012 – Final Power Chart



SMP  
SWVP  
Freq  
HW / SW  
AMP  
Many  
P  
A  
N

Islands  
C  
-  
D  
e  
s  
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C  
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## ITRS Power Chart

<i>Power Improvement</i>	<i>Year</i>	<i>Power Improvement dynamic</i>	<i>Power Improvement Static</i>		<i>Description of Improvement</i>
Clock Gating (Macro Level)	1996	.04x	.20x		Turning off the SoC when not in use.
Low Power Libraries	1997	.09x	.09x		Physical Libraries for Low Power Design.
Frequency Scaling	1999	.19x	.09x		Lowering the frequency for logic outside the critical path.
Clock Gating (Micro Level)	1999	.09x	.09x		Turning off blocks in the SoC when not in use.
Body Biasing	2004	.05x	.20x		Setting up a positive or negative voltage below a transistor to reduce leakage.

## ITRS Power Chart

<i>Power Improvement</i>	<i>Year</i>	<i>Power Improvement dynamic</i>	<i>Power Improvement Static</i>		<i>Description of Improvement</i>
Power Gating	2004	.04x	.20x		Turning off the power to blocks of the SoC.
Power Islands	2006	.09x	.09x		Using different power levels for blocks of the SoC.
Voltage Scaling	2007	.19x	.09x		Decreasing the voltage on blocks during non-peak work loads.
Architecture for Low Power	2007	.09x	.09x		Minimizing power usage at the architectural level.
HW Accelerators	2007	.22x	0		Using Libraries of hard wired algorithms.

## ITRS Power Chart

<i>Power Improvement</i>	<i>Year</i>	<i>Power Improvement dynamic</i>	<i>Power Improvement Static</i>		<i>Description of Improvement</i>
RTL opt/D gating	2007	.22x	0		Minimizing power at the RT Level.
<b>Total 1996 Thru 2007</b>		<b>2.90x</b>	<b>2.20x</b>		

## ITRS Power Chart

<i>Power Improvement</i>	<i>Year</i>	<i>Power Improvement dynamic</i>	<i>Power Improvement Static</i>		<i>Description of Improvement</i>
Homogeneous (SMP) Parallel Processing	2009	1.50x	1.00x		Using multiple identical processors in a parallel computing architecture.
Software Virtual Prototyping	2011	1.23x	1.20x		Modeling the hardware for the early development of the Software.
Frequency Islands	2013	1.26x	1.00x		Designing blocks that operate at different frequencies.
HW/SW CO-Design	2015	1.18x	1.00x		HW/SW design at the behavioral level based on power.
Heterogeneous (AMP) Parallel Processing	2017	1.18x	1.00x		Using multiple types of processors in a parallel computing architecture.

## ITRS Power Chart

<i>Power Improvement</i>	<i>Year</i>	<i>Power Improvement dynamic</i>	<i>Power Improvement Static</i>		<i>Description of Improvement</i>
Multi-Core Software Development tools	2019	1.20x	1.00x		A set of embedded development tools built for multicore, power aware designs
Power aware Software	2021	1.21x	1.00x		Developing software using power consumption as a parameter.
Asynchronous Design	2023	1.21x	1.00x		Non-clock driven design.
Near Threshold Computing	2025	1.23x	0.80x		Lowering your supply voltage close to the theoretical minimum.
<b>Total 2009 Thru 2025</b>		<b>11.20x</b>	<b>9.00x</b>		



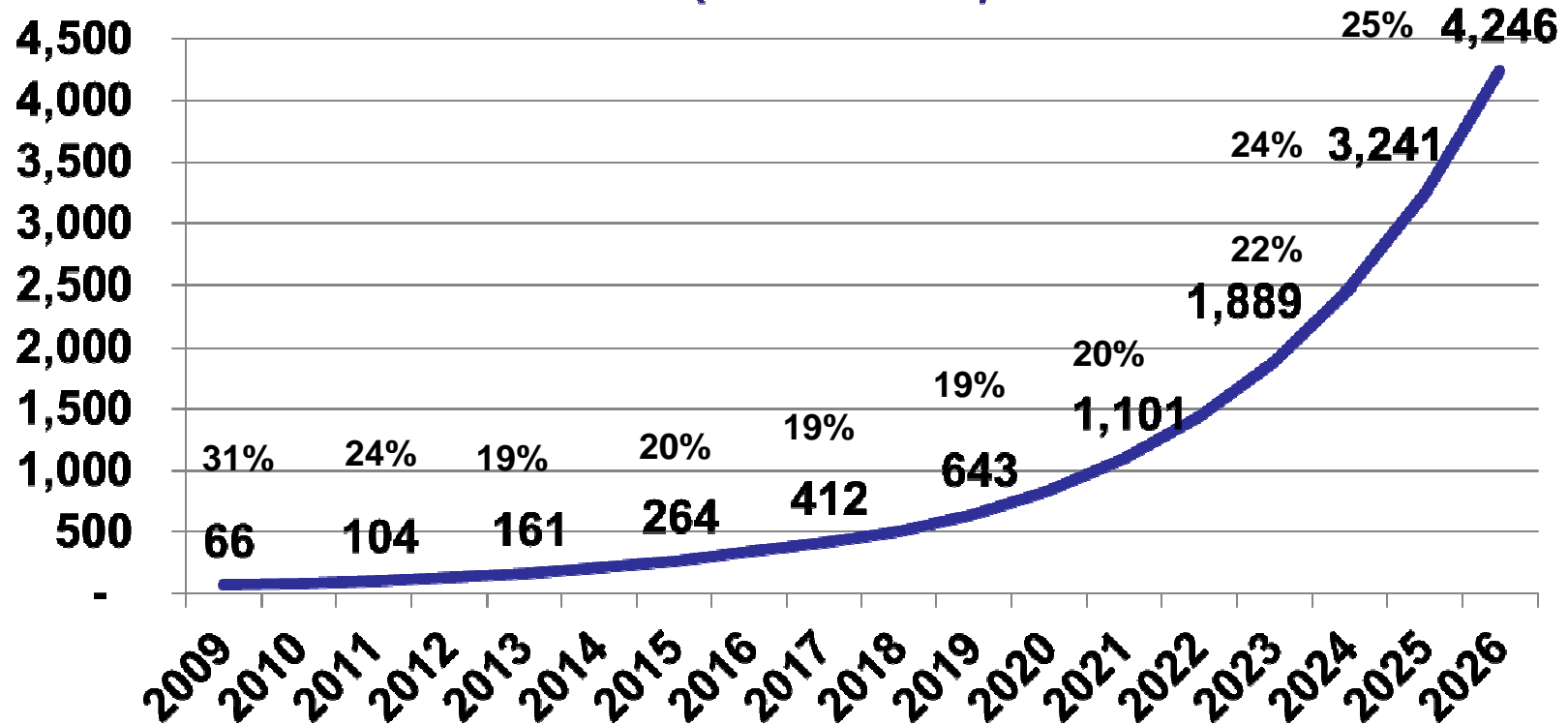
# The Five Design Constraints

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- Performance
- Power
- Design time
- Cost of design
- Cost of the packaged SoC

# Average High-End Mobile SoC

Total SoC Gates  
(in millions)

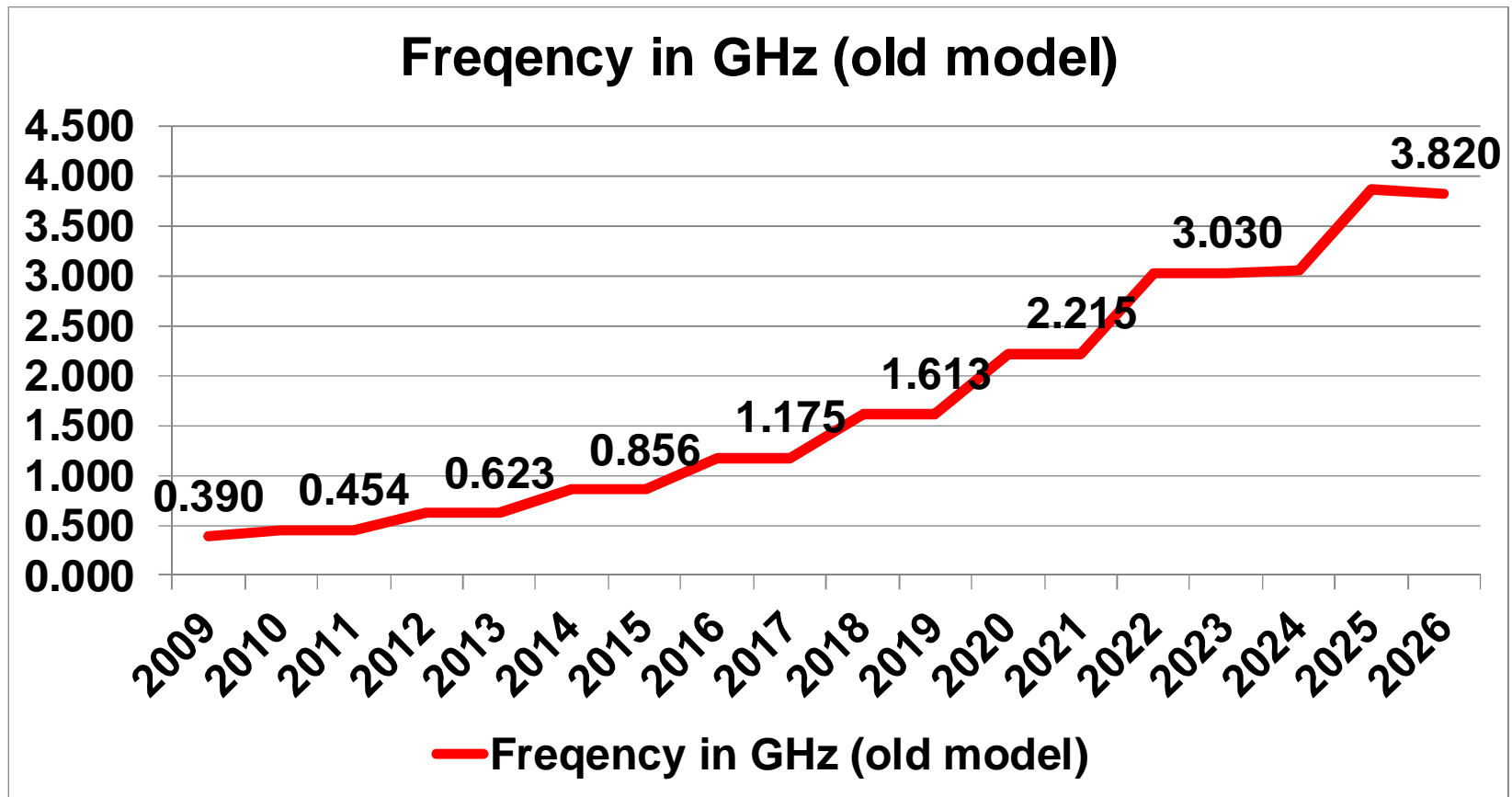


# Design Trade-Offs

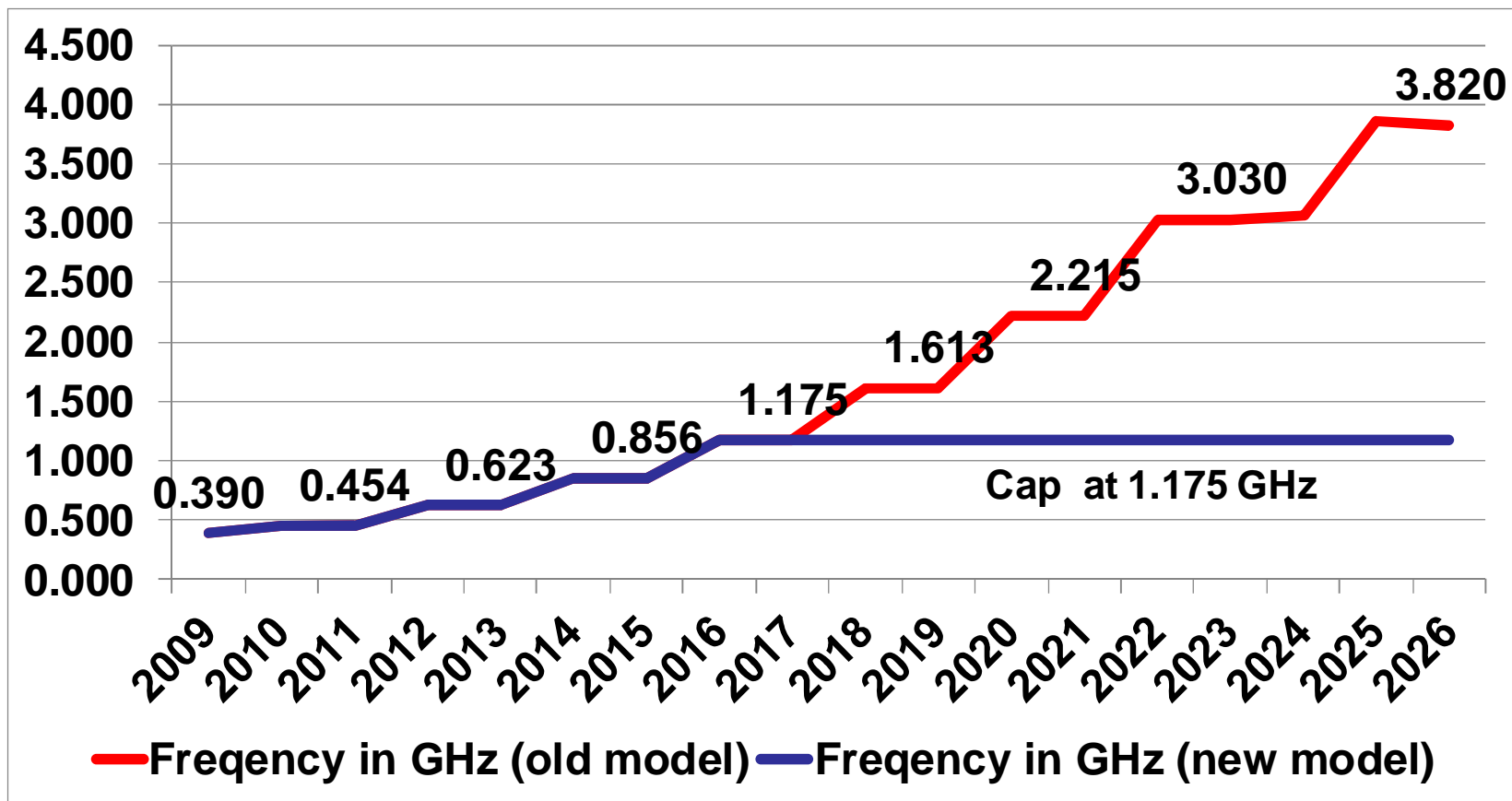
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- Average Power (Energy)
- Gate Count
- Frequency

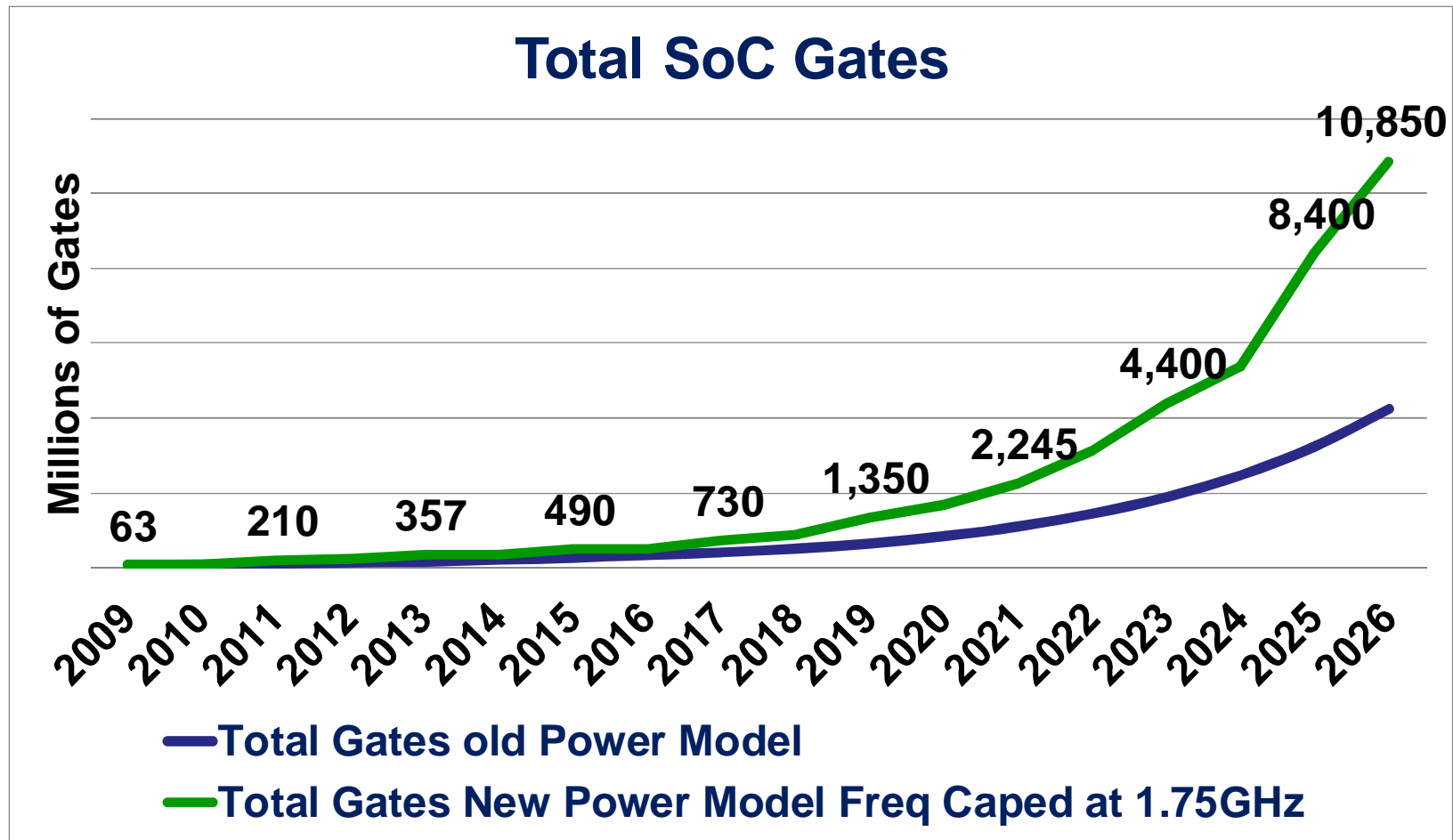
# Frequency Chart @ 5 Watts



# Frequency Chart @ 5 Watts



# Average High-End Mobile SoC



In 2013 we hit the max gate point.