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INVENTIVE

System-Level EDA 2015

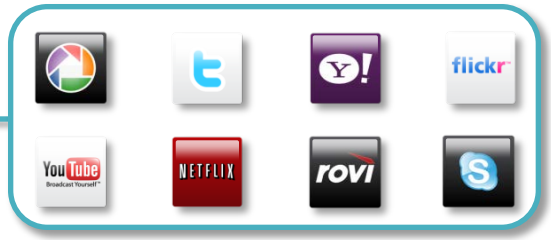
Who's Problem is Software Anyway?

Frank Schirrmeister, March 2012
EDPS, Monterey

Market Drivers

Driving disruptive change in product realization

- Apps
- Video
- Mobility
- Cloud
- Green Tech



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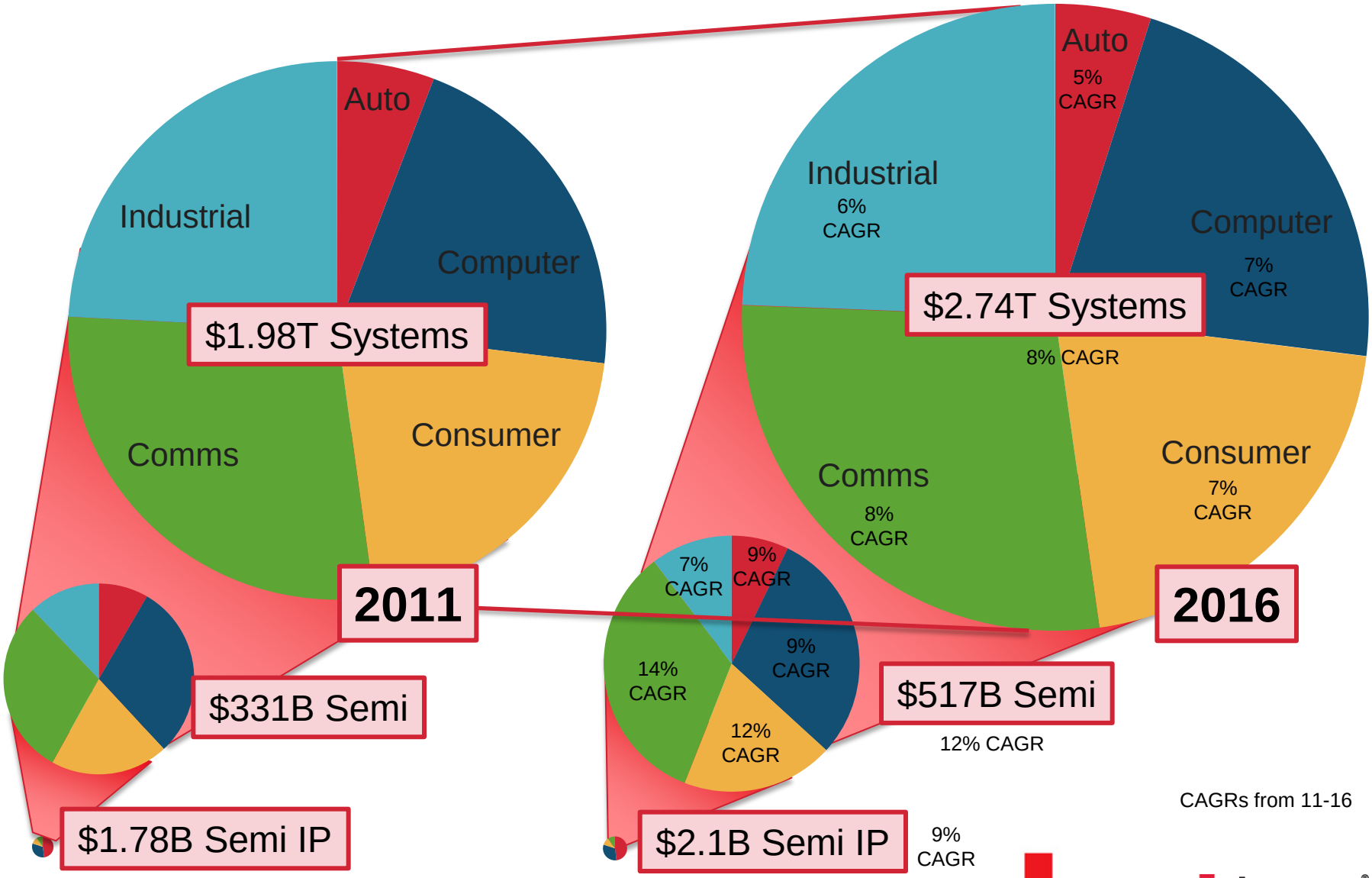
The Electronics Value Stack



CAGRs from 11-16

Sources: dataBeans, Gartner

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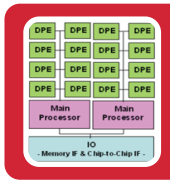
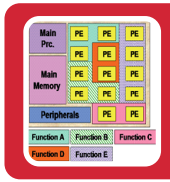
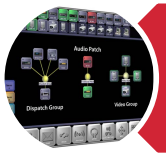
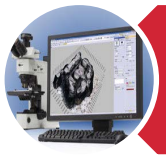
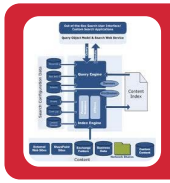
Software Defines User Experiences

	Automotive	AUTOSAR, Microsoft Embedded (Ford Sync), Linux (GENIVI)	 Infotainment
	Computers	Windows, OSX, Linux, …	 Consumer Stationary
	Consumer, Wireless Comms	IOS, Win 7 Mobile, Android (HTC Sense, Marvell Kinoma)	 Consumer Portable
	Communications	Linux, Windows, OSX, NOS	 Network
	Industrial	Integrity, VxWorks	 Compute

Sources: Cadence, ITRS

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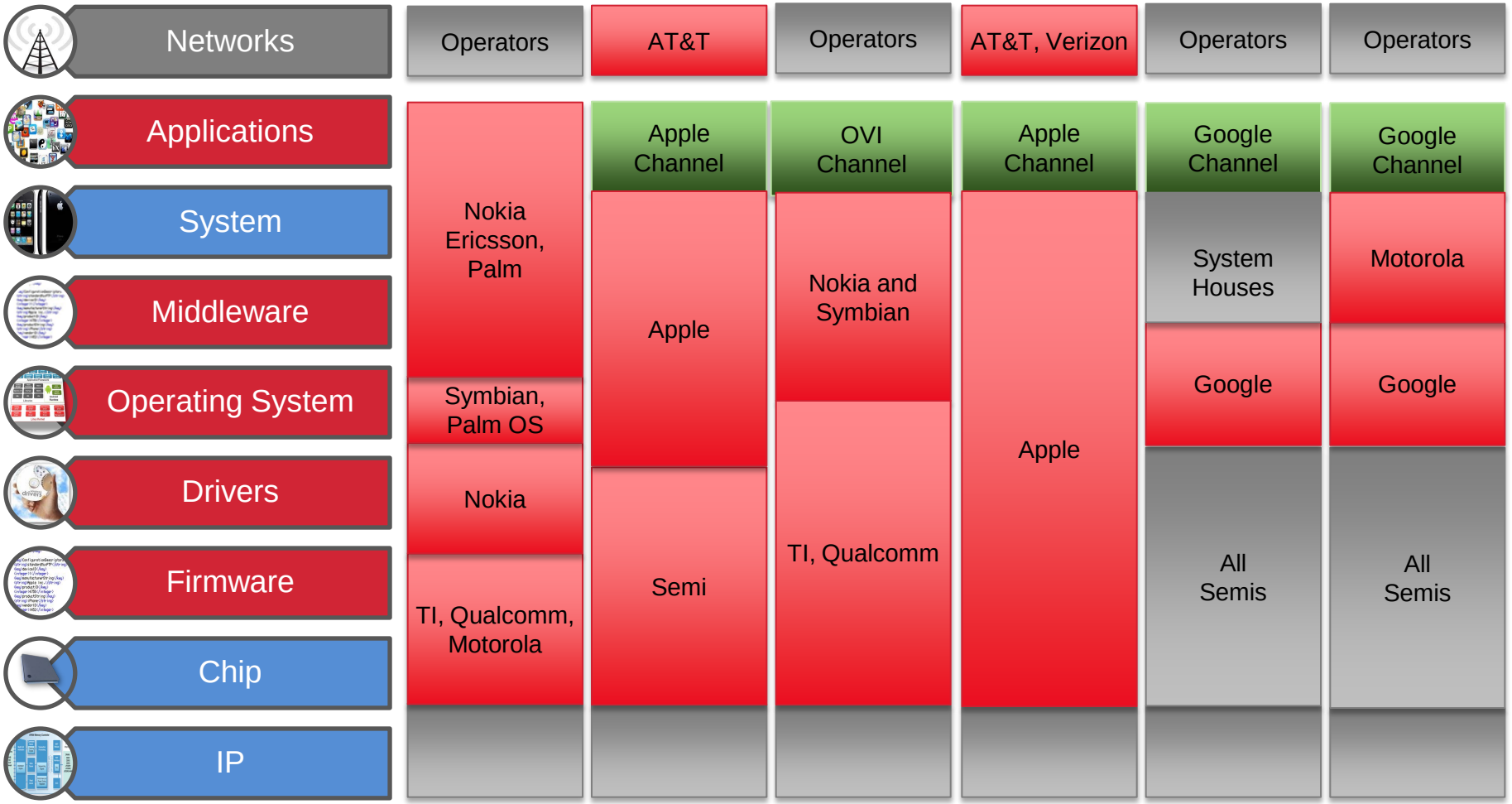
Mobile Wireless Design Chain

Aggregation vs. Disaggregation



Inspired by Prof. Barke

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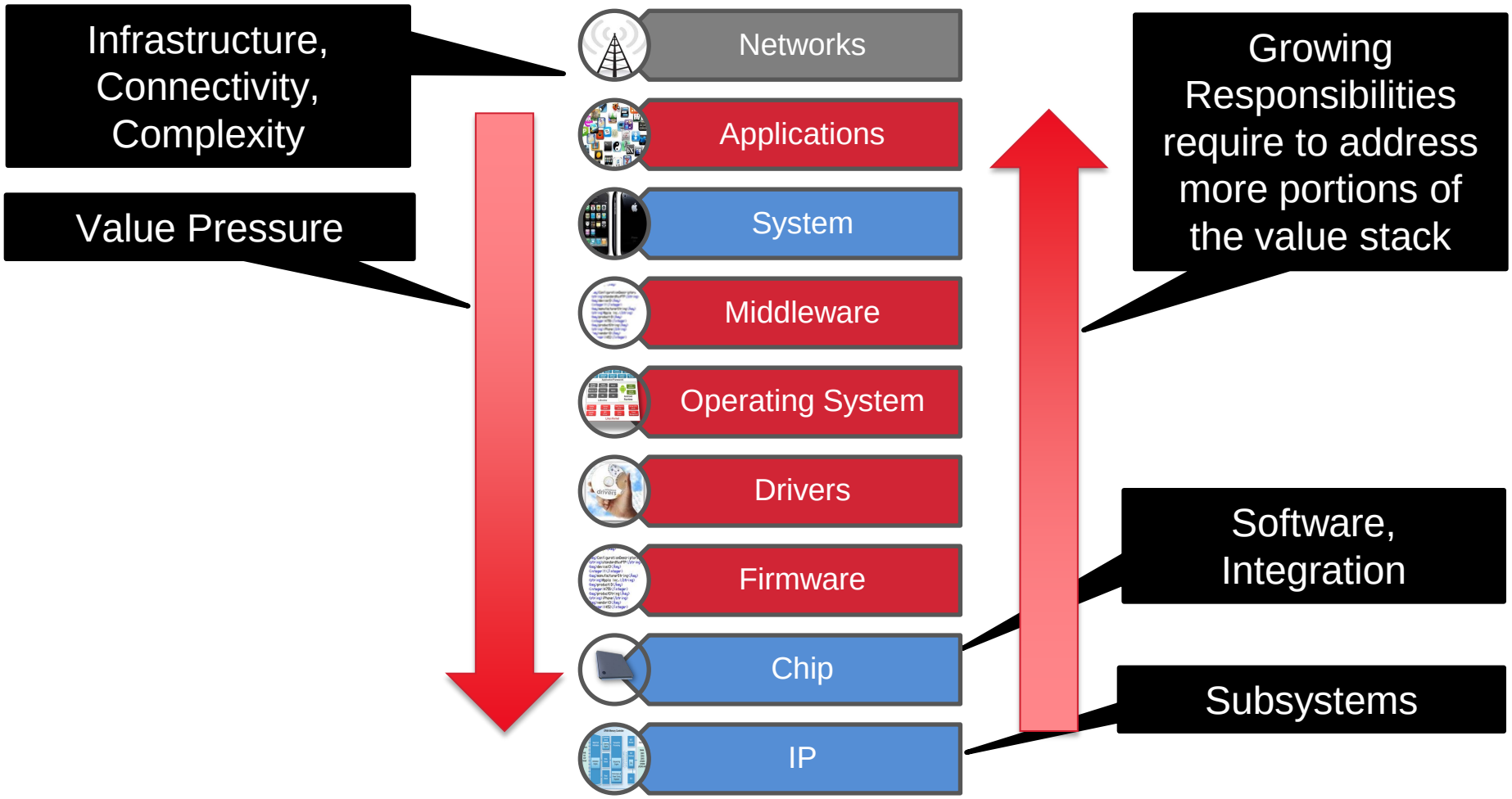
Changing Industry Dynamic



Inspired by Prof. Barke
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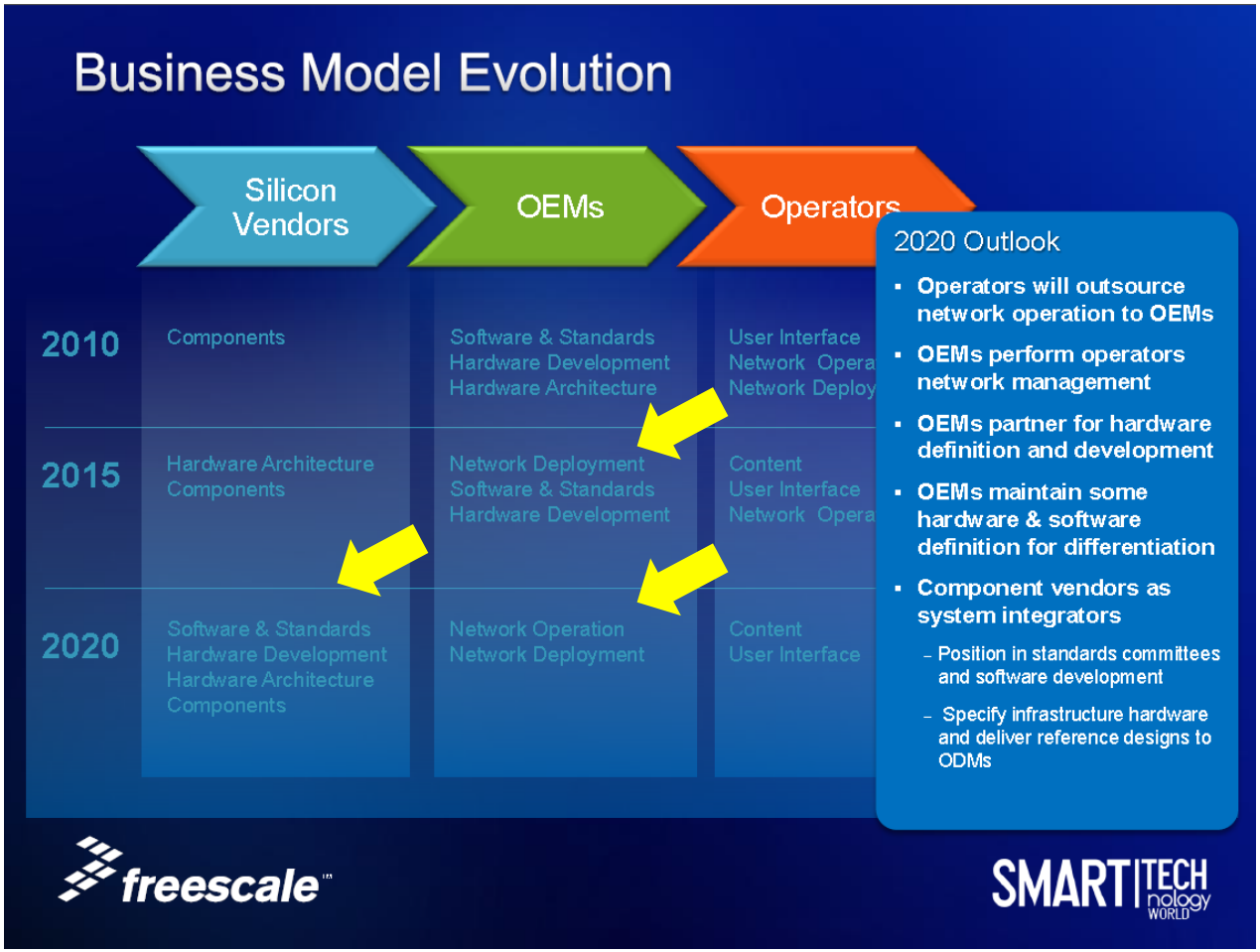
Infrastucture Design Chain

Aggregation vs. Disaggregation



Electronic Landscape is Changing

Software development is causing disruptive changes

Design Chains

IP – Semiconductor – Systems

Vendors are interconnected and dependent
Value pressure drives top down
Responsibilities grow bottom up

User Experience

System vendors own the user experience

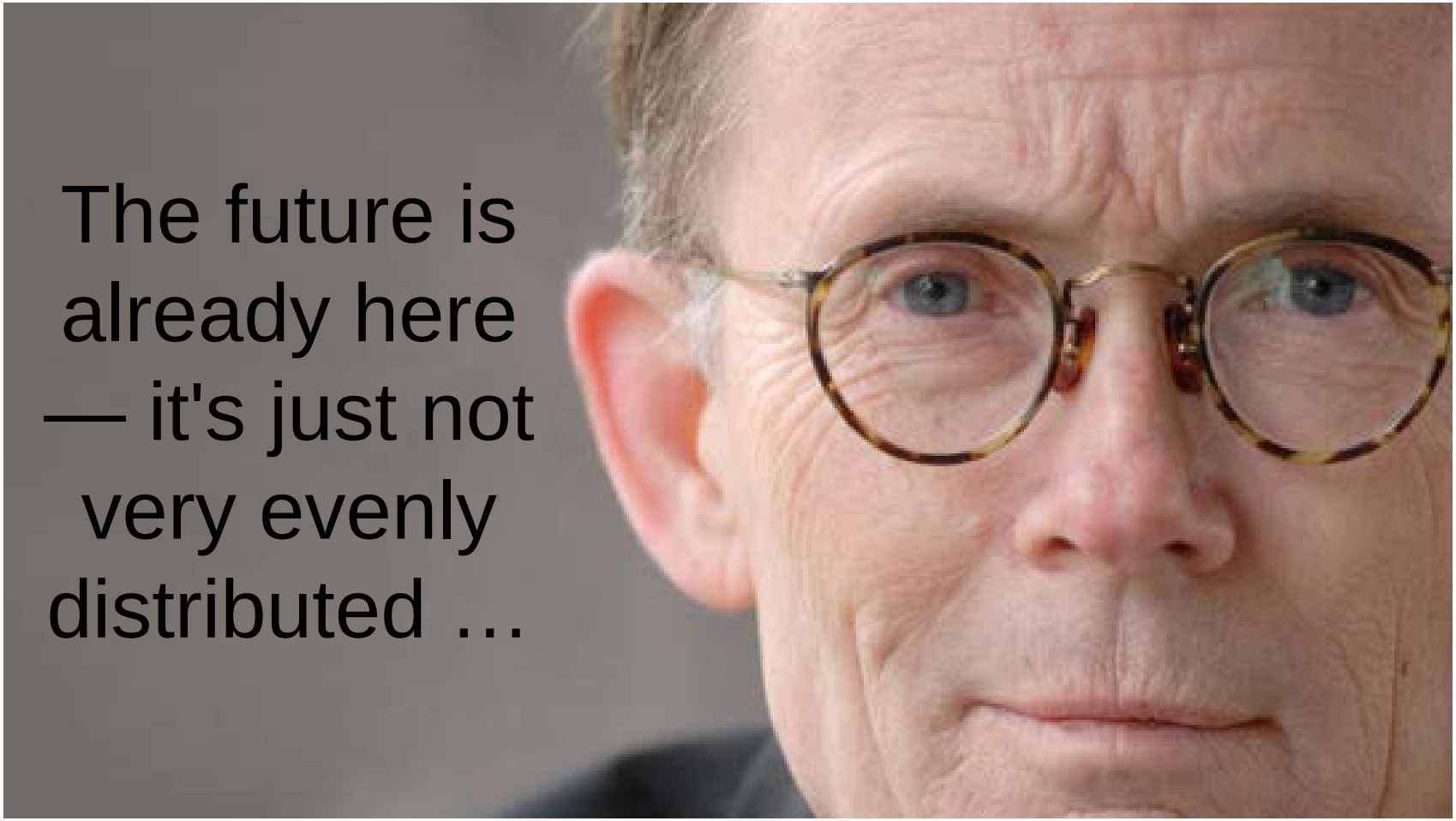
User experience is driven by software – Apps
Hardware platforms consolidate application specific

HW/SW Convergence

Software changes HW/SW development processes

Changing responsibilities between vendors and new role of software needs to be addressed

So what does this mean for EDA?

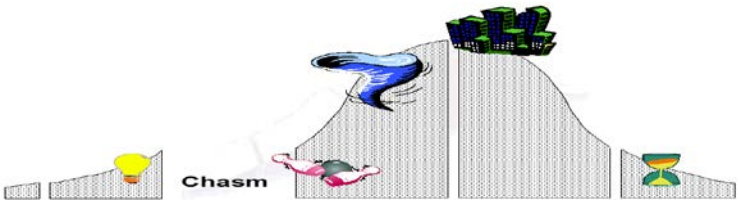


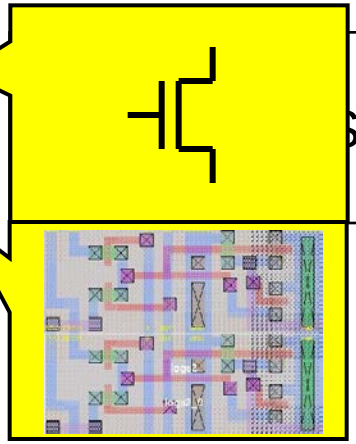
"The Science in Science Fiction" on *Talk of the Nation*, NPR (30 November 1999, Timecode 11:55), William Gibson

A Brief History in Abstraction
Layout to Transistors

Hardware	*Software*

Technology	Transistors	SM
	Layout	





1980 1985 1990 1995 2000 2005 2010 2015 2020 2025

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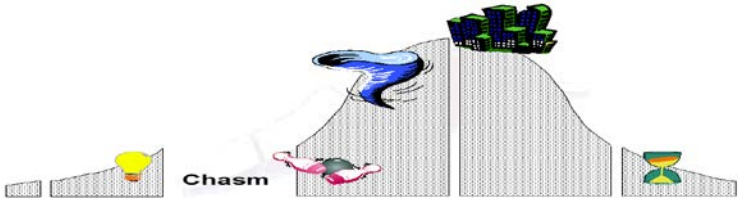
A Brief History in Abstraction
Transistors to Gates

	Hardware	*Software*
Signal	{**Verilog**,VHDL} RTL, SystemC 1.0	
	{**Verilog**,VHDL} Gate, Schematic	
Technology	Transistors	
	Layout	



1980 1985 1990 1995 2000 2005 2010 2015 2020 2025

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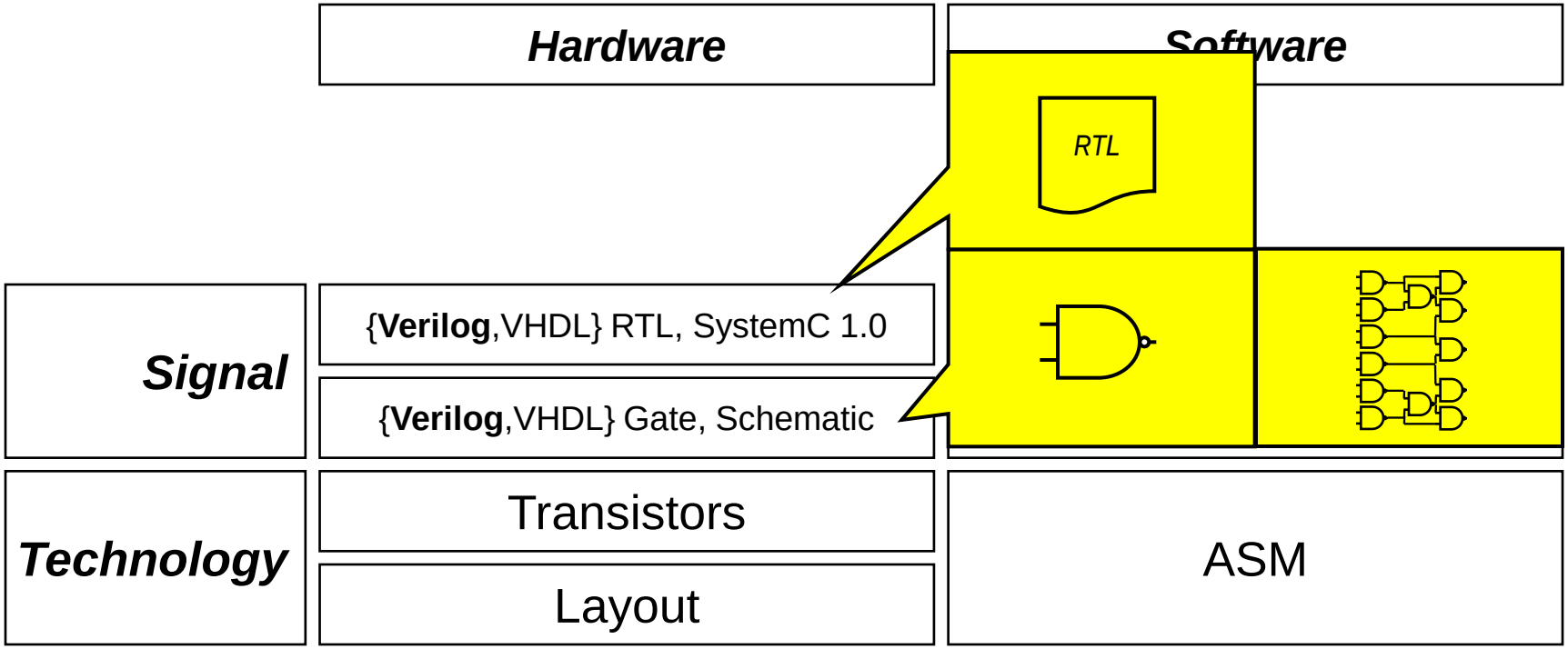
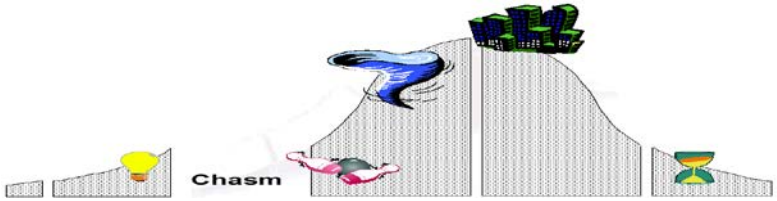
A Brief History in Abstraction
Gates to RTL





1980 1985 1990 1995 2000 2005 2010 2015 2020 2025

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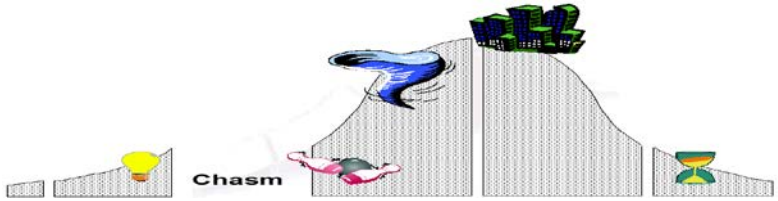
A Brief History in Abstraction
RTL, Transactions

	Hardware	Software
Transaction	Verilog, VHDL, **SystemC TLM 2.0**	RTL, TLM Clusters, SW Models
Signal	{**Verilog**,VHDL} RTL, SystemC 1.0	C
	{**Verilog**,VHDL} Gate, Schematic	
Technology	Transistors	ASM
	Layout	



1980 1985 1990 1995 2000 2005 2010 2015 2020 2025

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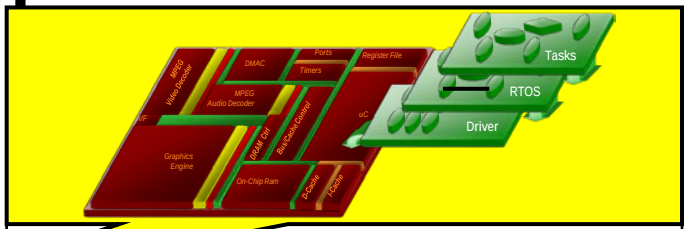
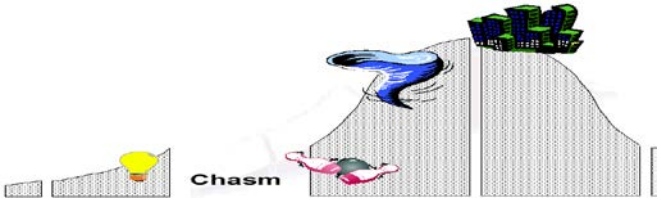
A Brief History in Abstraction

"The HW/SW Independent Level"



	Hardware	Software
Token	**Different Proprietary MoCs**, Ptolemy, SystemC TLM 2.0, C++, UML, **SysML**	
Transaction	Verilog, VHDL, **SystemC TLM 2.0**	C, C++
Signal	{**Verilog**,VHDL} RTL, SystemC 1.0	C
	{**Verilog**,VHDL} Gate, Schematic	
Technology	Transistors	ASM
	Layout	



1980 1985 1990 1995 2000 2005 2010 2015 2020 2025

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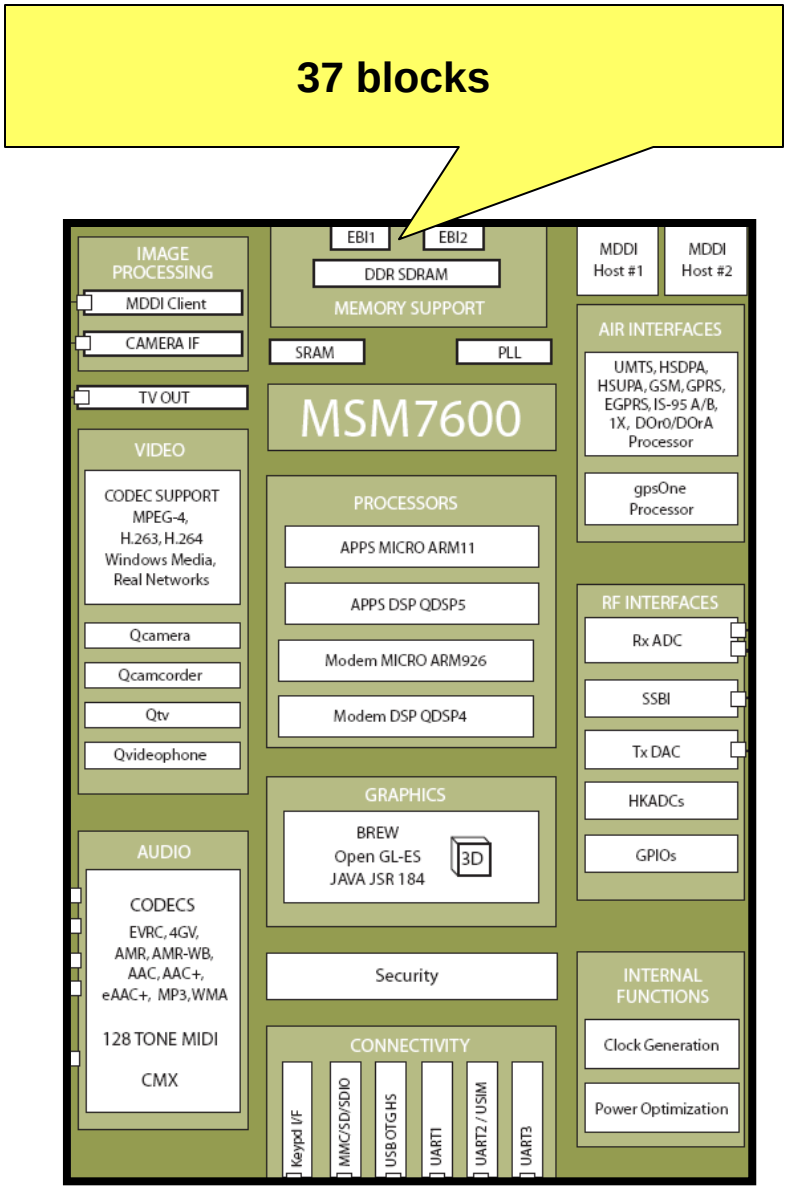
A Chip in 2015

- **Software, Software, Software**
- More complex designs
- … but less of them
- More than 110 IP Blocks
- More than 70% re-use
- More than 60% of effort in software
- Multi-core
- Software distributed across cores
- Low power issues
- Application specific issues
- High analog mixed signal content
- Changing team dynamics
- Changing Industry Dynamics



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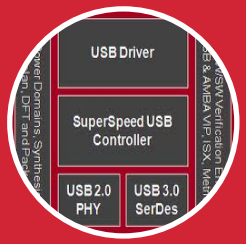
Design Chain Needs to Collaborate

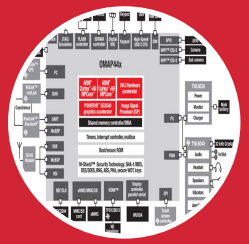
IP Vendor | Semi Vendor | System Vendor | Software Vendor | Operator

Value Pressure - Requirements

Responsibility - Enablement



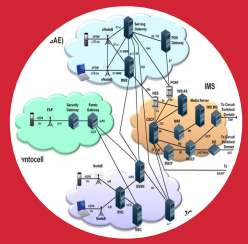
Semi IP Models



Chip Models

System Models

SW Dev Kits



Performance Models

Concerns: costs, automatic model creation, validation, ECO management

Challenges: integration, qualification, supplier management

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There is no “One Size Fits All”

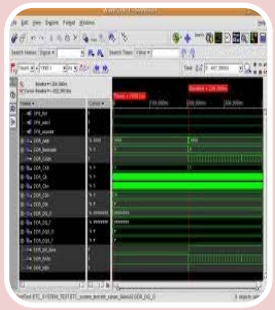
Software Enablement Platforms need to interoperate

SDK

- Highest speed
- Ignore hardware
- Earliest in the flow

Virtual Platform

- Amost at speed
- Less accurate (or slower)
- Before RTL
- Great to debug (but less detail)
- Easy replication



RTL Simulation

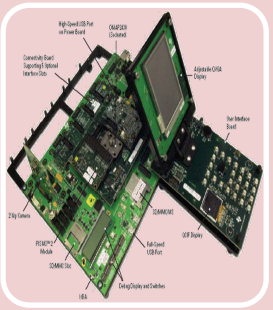
- KHz range
- Accurate
- Excellent HW debug
- Little SW execution

Acceleration Emulation

- MHz Range
- RTL accurate
- After RTL is available
- Good to debug with full detail
- Expensive to replicate

FPGA Prototype

- 10’s of MHz
- RTL accurate
- After stable RTL is available
- OK to debug
- More expensive than software to replicate



Prototyping Board

- Real time speed
- Fully accurate
- Post Silicon
- Difficult to debug
- Sometimes hard to replicate

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EDA Transformation

Towards Electronic System Design Automation

The Imminent EDA Transformation

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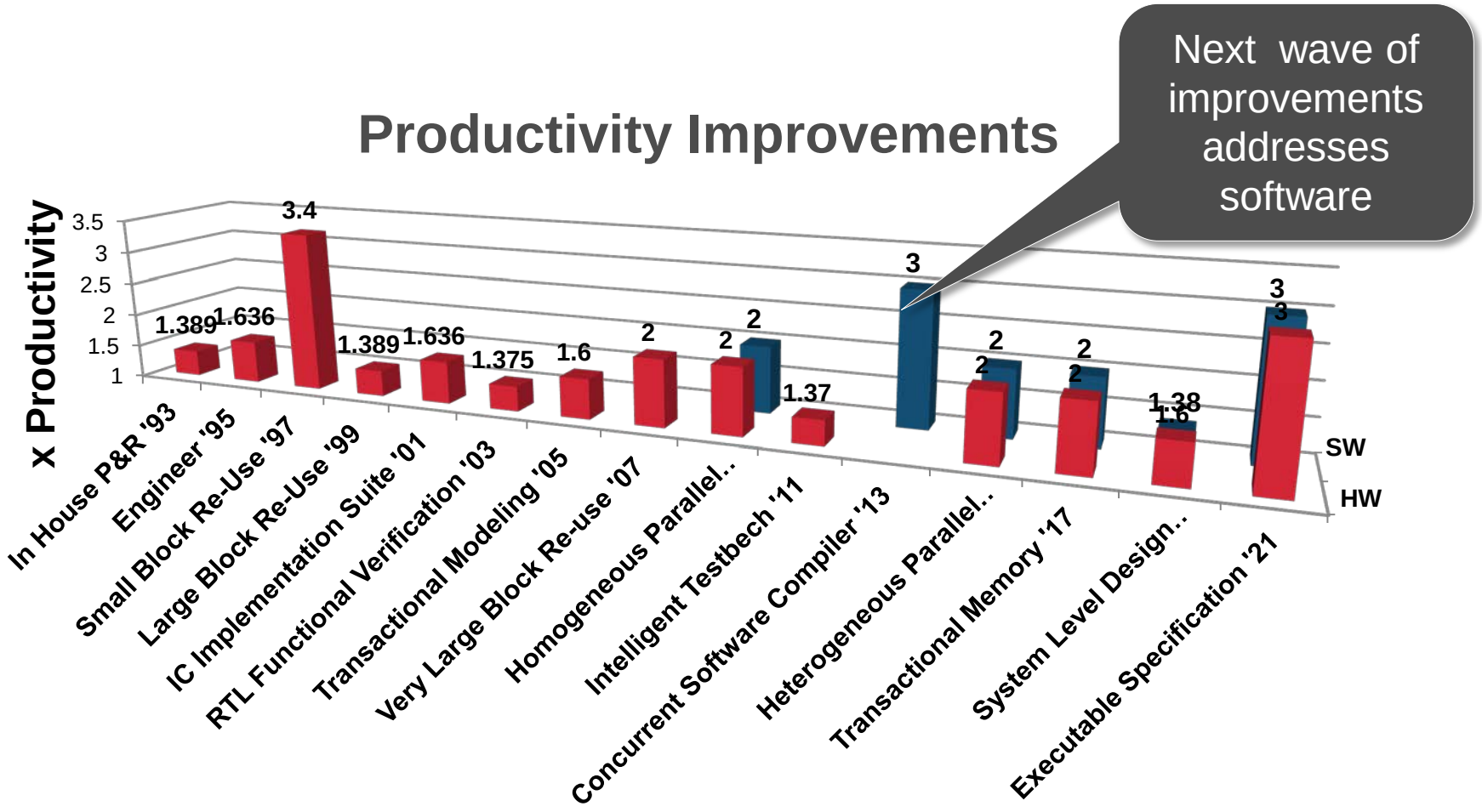
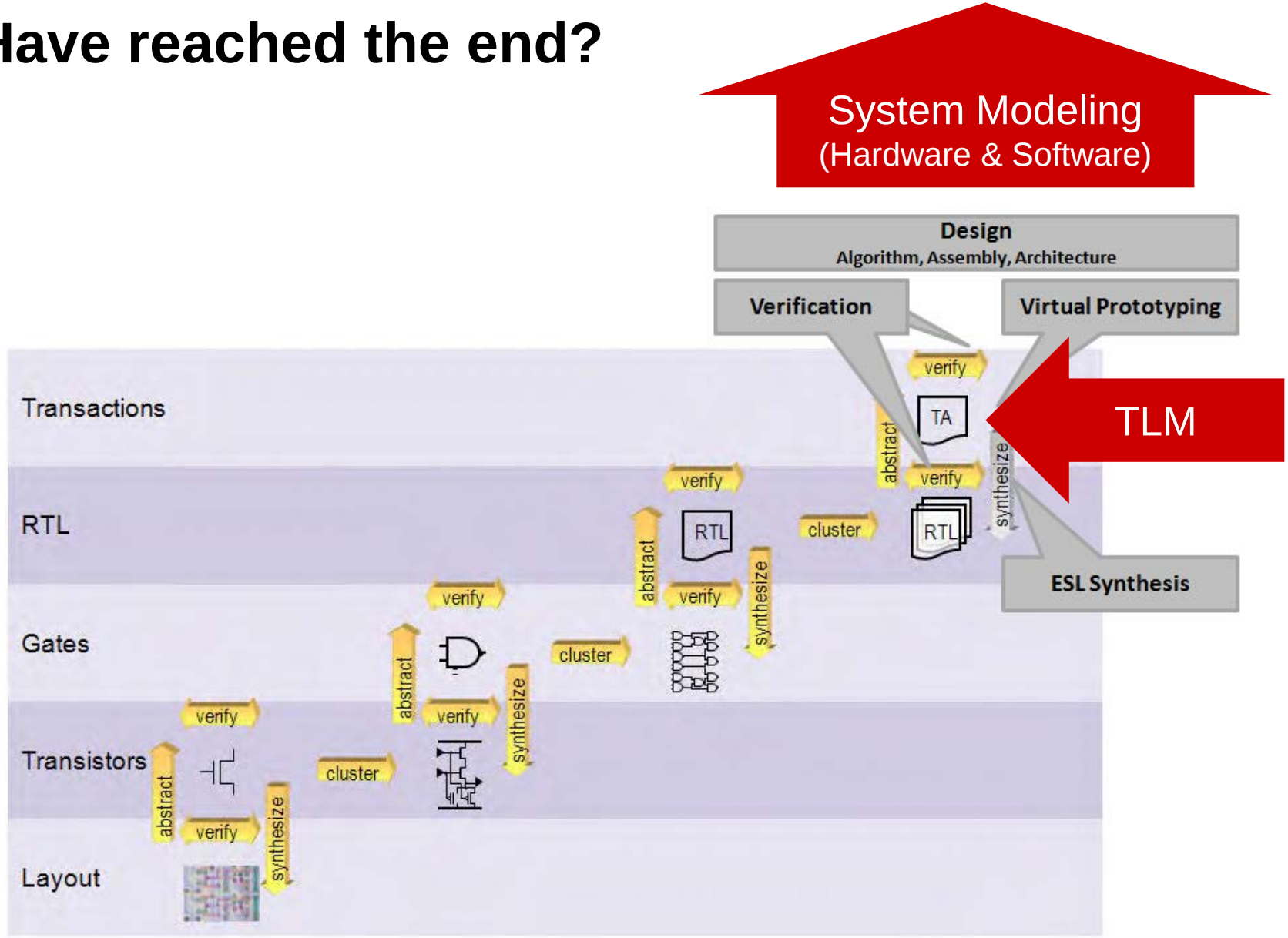
EDA Productivity Improvements



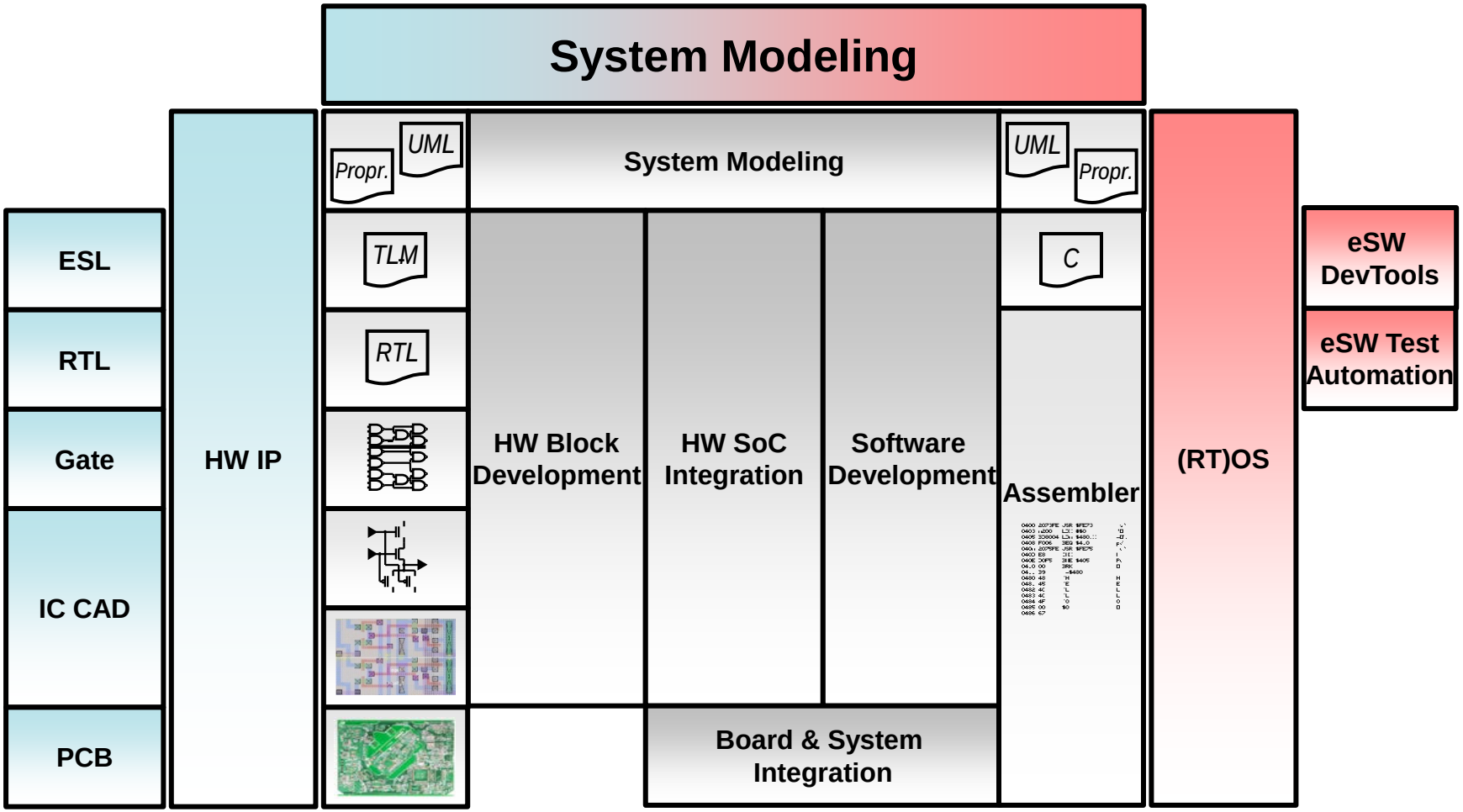
Source: ITRS

Have reached the end?



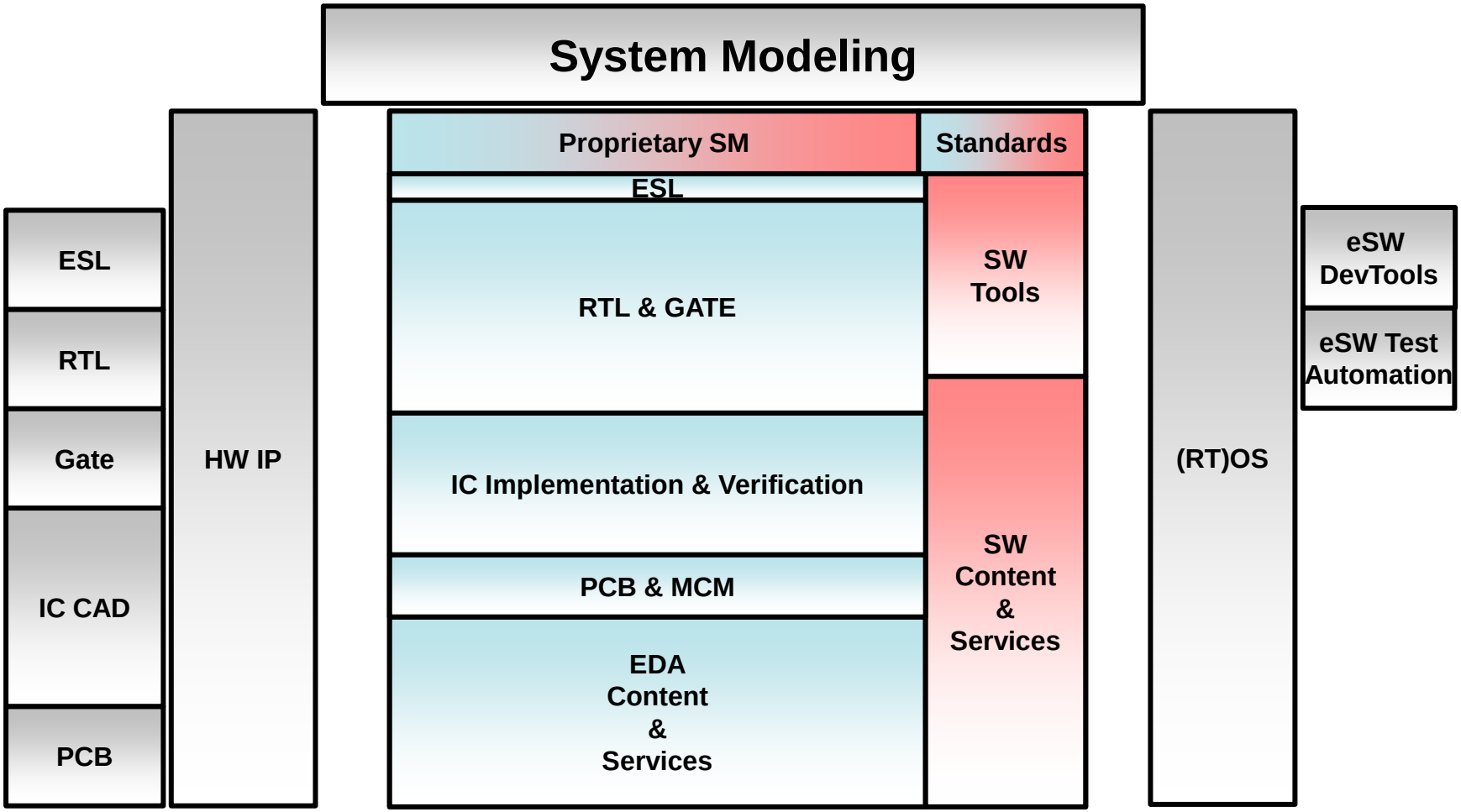
System Modeling is a natural next level …

Modeling independent from Hardware and Software



System Modeling is a natural next level …

Modeling independent from Hardware and Software



Source: EDAC, VDC, Cadence

… who will be servicing it is the question!

Source: http://showmeyourindies.com/indieflix/indieflix-blog/the-tortoise-and-the-hare-being-a-filmmaker-in-an-ever-changing-world/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