

Early DFT Exploration and Verification

By

Sri R Ganta, MWG Group,
Broadcom



4th April, 2012

Agenda



- Introduction
- Compelling Reasons
- How to Address the Issue
- Conclusion

Some FACTS about DFT



- DFT is NOT about stuck-at faults and ATPG generation ONLY
- DFT is NOT just a post-netlist task
- DFT is measuring gauge for functional modes and features
- DFT is KEY to volume production

Some Features of Modern Complex ASICs



- DVFS (Dynamic Voltage Frequency Scaling)
 - Voltages and Freq. are scaled based on modes of operation
- Variable and Fixed Voltage Domains
 - Some regions are on variable and some are on fixed voltage domains
- Switchable Power Domains
 - Power switches to shut off/on regions
- Retention Capabilities
 - Memory arrays and Std. Cells with retention capabilities
- AVS(Adaptive Voltage Scaling)
 - Voltage is varied on-chip based on silicon performance
- Speed Binning
 - Be able to speed-bin certain cores (mostly processors)

All these features add additional challenges for DFT

DFT Challenges To Test Functional Features

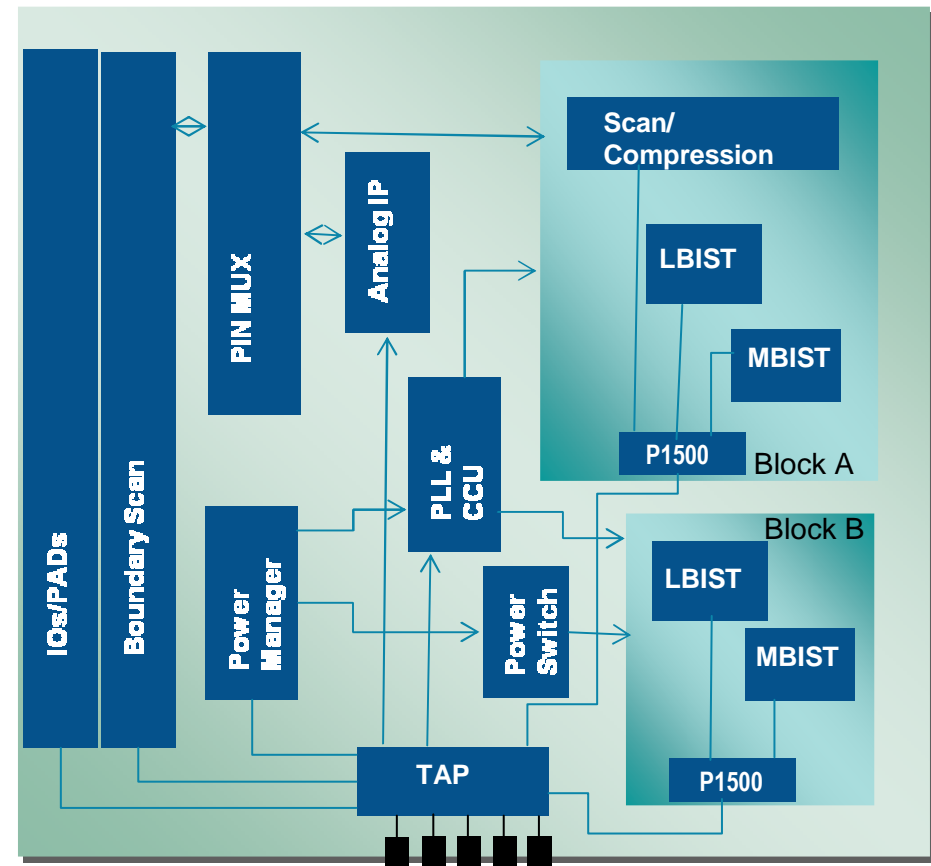


- DFT should test true At-speed behavior of circuit
 - Need to use on-chip functional clock control units in Test Mode also
- DFT Should test all DVFS Modes of Operation
 - Clocks controls and dividers should be controllable in Test Mode
 - LBIST/MBIST/Scan tests should run at scaled freq. of DVFS modes
- DFT Should test Variable and Fixed Voltage Domain Isolations
 - ISO cells and LevelShifters should be tested
 - Necessary control signals should be controllable in TestMode
- DFT should test Power Domain Infrastructure
 - Power Switches and Distributed Power Switches need to be tested
- DFT should test Memory and Std Cell Retention
 - MBIST, Lbist/Scan structures should be built to test retention capability
- DFT Test Vectors should test critical paths for speed-binning of certain cores
- DFT should provide interface to Analog IP testing

Representative Chip



- TAP: Main interface to all DFT structures
 - provides controls and status signals in TestMode
- PIN MUX: Provides pin muxing to share functional IOs for different modes
 - Ex., Analog, Scan etc modes
- Power Manager: Provides control signals to power structures
 - identifies DVFS modes, Sleep, Normal, Turbo etc.
- PLL & ClockControlUnit: Provides clocks to all blocks
 - provides scaled down/up clocks based on DVFS modes



Early DFT Planning and Validation is Required



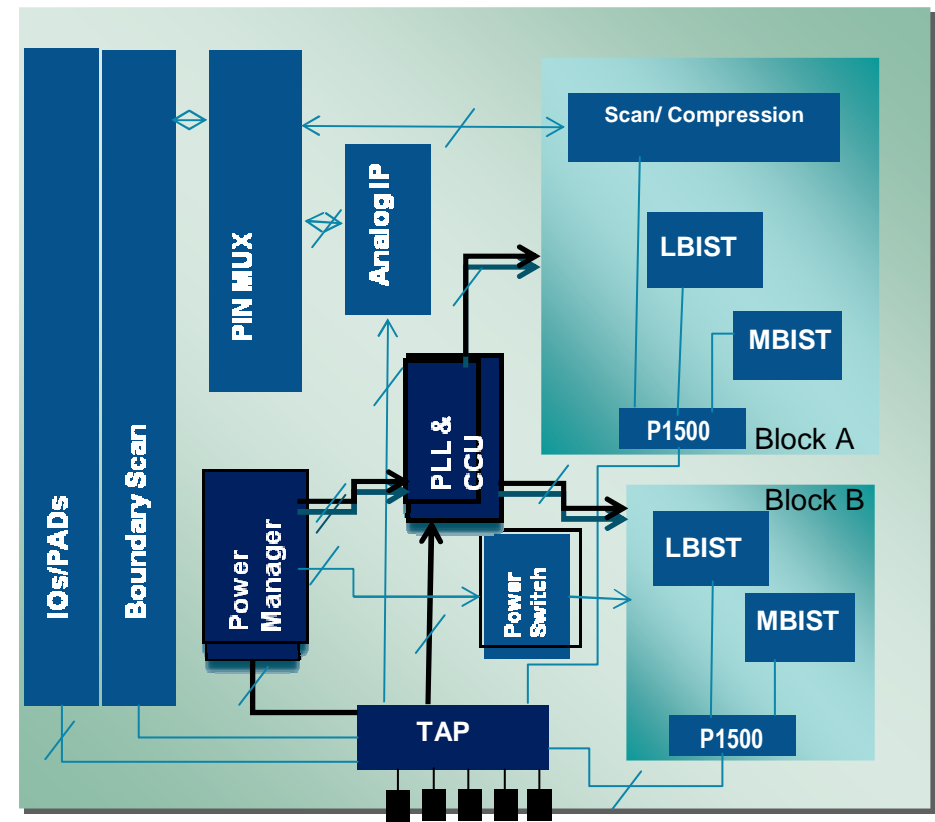
- Early DFT Planning is required
 - Identify necessary control signals and test features
 - Add required test infrastructures in RTL itself
 - TAP controller with necessary UDR controls can be generated in RTL
 - BoundaryScan to test all IOs can be generated and added in RTL
 - DFT controls and muxes to control PinMuxing, Clock Controls, Power Manager, Analog IP, etc can be added RTL itself
- Early DFT Validation in RTL is required
 - Run IEEE 1149.1 tests to validate TAP and Bscan logic
 - Validate all clocks and their frequencies in different DVFS modes
 - Validate PinMuxing for different modes, Analog, Scan, Monitoring etc.
 - Validate Pad control signals
 - Validate control signals for Analog Testing
 - Validate power control signals
- Failure to do early DFT planning and validation will result in major schedule impact
 - DO NOT wait for netlist

Fix the Problem Before It Becomes a Problem

Clock Verification at RTL



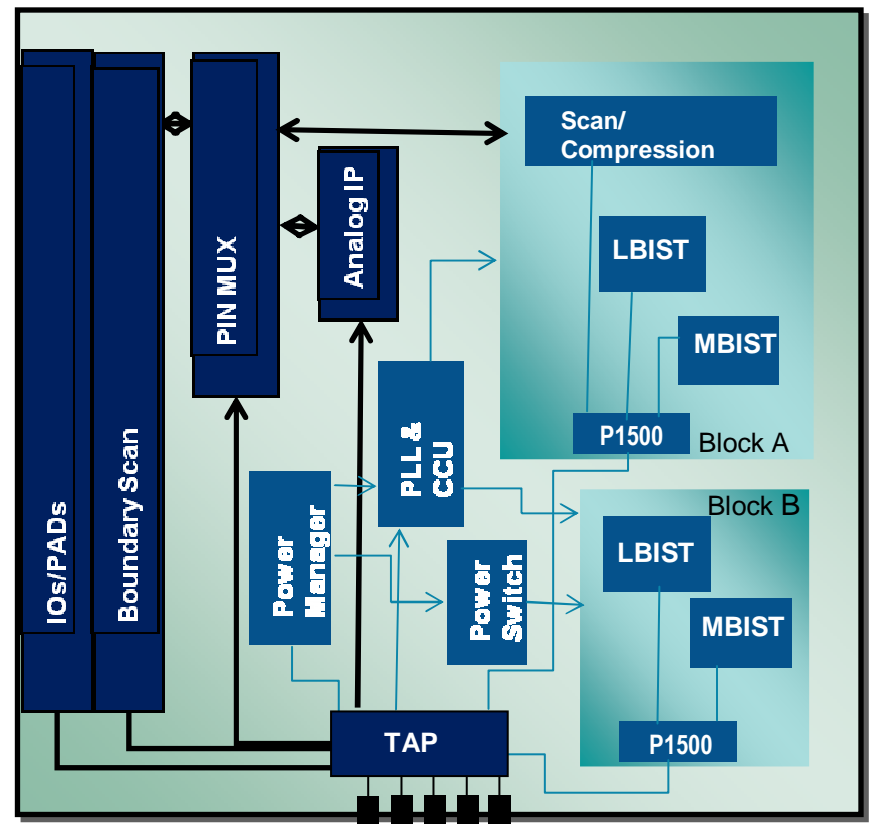
- Master/Generated clock paths can be traced under different DVFS modes in TestMode
- DRC for path blockage, unexpected driver, period, waveform can be checked
- Blocking points can be debugged
- Testbenches can be generated and simulated



Pin-pin Connectivity Check in RTL



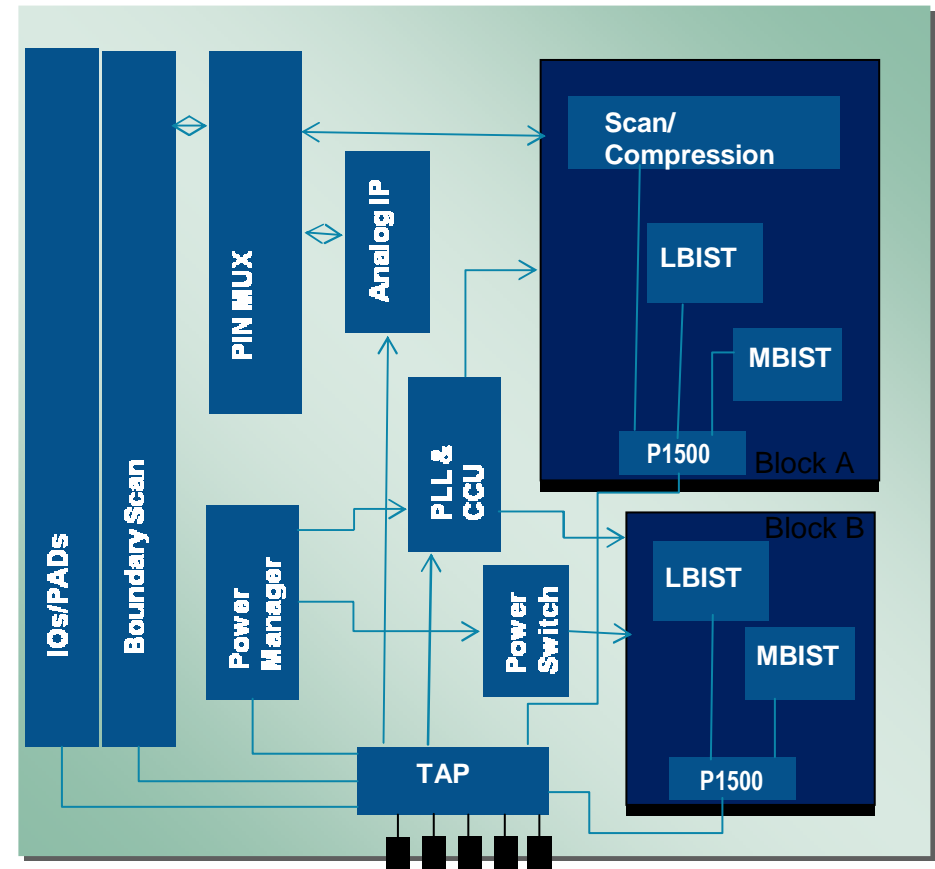
- Pin Muxing connectivity check can be done in RTL for different modes, Scan, Analog etc
- Loads/Drivers can be traced
- Constants and JTAG UDRs can be propagated



DFT DRC checks in RTL



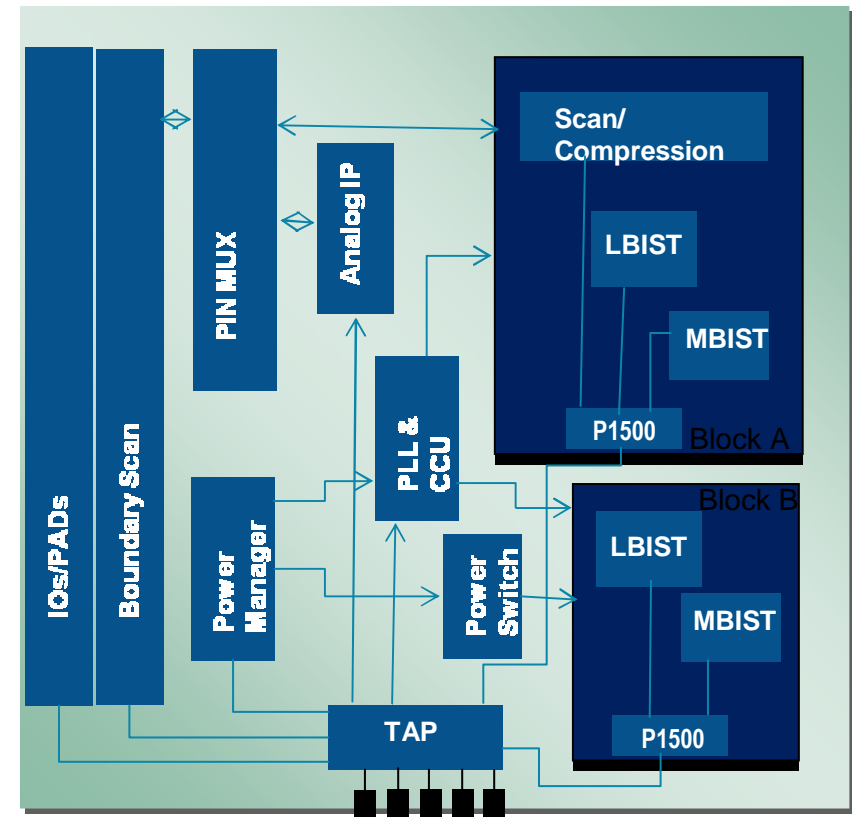
- Run DFT rule checks at RTL
- Identify and fix testability issues early on



DFT Test Coverage at RTL



- Evaluate and Debug Test Coverage in RTL
- Hierarchical and per module coverage can be debugged
- Provide test coverage enhancements/fixes
 - Clk/Reset controllability fixes
 - Control and Observe points for shadow logic around black-box/nonscan instances



Conclusion



- Fix The Problem Before It Becomes A Problem
- DFT is NOT about stuck-at faults and ATPG generation only
- DFT is NOT just a post-netlist task
- DFT is measuring gauge for functional modes and failures
- DFT is KEY to volume production
- Early DFT planning and verification is compelling
- Failure to do Early DFT would result in major schedule impacts

Fix the Problem Before It Becomes a Problem

Thank You

