3D-ICs
Real or Imaginary

Dusan Petranovic

Marketing, Design to Silicon Division

April 2011

Mentor Graphics®

Status of TSV based 3D-IC

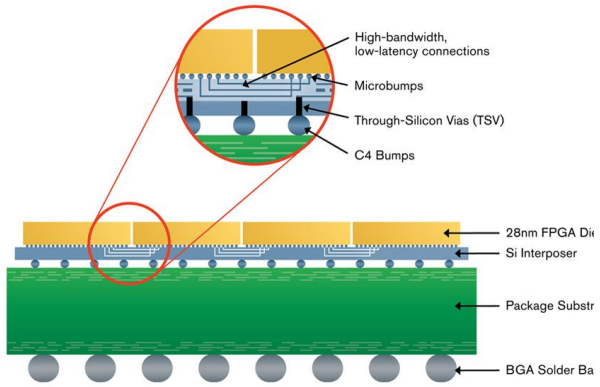
- 3D ICs are real. Lot of recent announcements →
  + Intel, TI, ST,… might come with the product sooner?
- Driven by the customer demands for more functionality, larger bandwidth, lower power, smaller size;
  Driven by technical advancement more then cost
- … and inability of 2D SoC to respond to the customer demands in cost efficient and timely manner

Company	Interposers		3D with TSV	
TSMC	2H 2011	[2]	2012-2013	[3]
UMC			2H 2011	[4]
GlobalFoundries			2013	[5]
IBM	2011	[6]		
Samsung			2012	[7]
Elpida			2H 2011	[4]
Micron			2012	[8]
Nanya			2011-2012	[9]
ASE	2012-2013	[10]		
STATSChipPAC			2013	[11]
Amkor	2H 2011	[3]		
SPIL	2011	[12]	2012	[12]
Qualcomm			2013	[12]
Nokia			2012-2013	[12]
Xilinx	2H 2011	[2]		
Dell			2012	[13]

Source: P.Garrou, Micronews, Jan.2011.

- No technological show stoppers; Need more work or compatibility between the TSVs and CMOS devices

- Various configurations -- 2.5 D and 3D
- Interposers came as a relief, will stay around long, but might not be sufficiently good for all applications

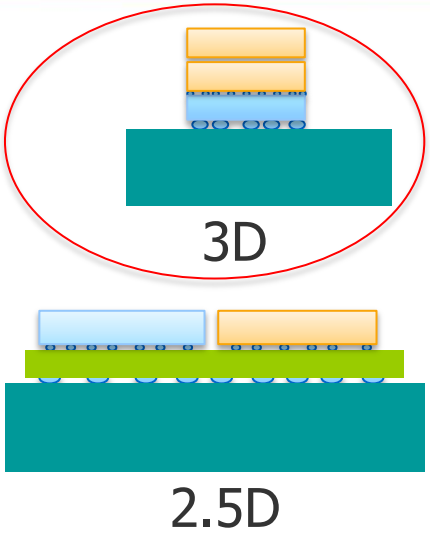


Source: www.xilinx.com/technology/roadmap/ssi-technology.htm

EDA Challenges

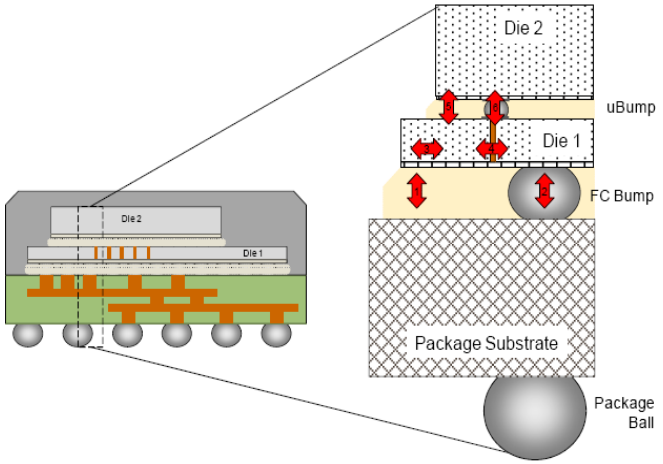
DESIGN

- Major challenges are in the design space , in 3D more then 2.5D
- Physically aware architectural exploration of increasing number of system level options (provided by new degrees of freedom)
- Determination of optimal 3D granularity and number of stack levels to achieve performance/power/size benefits through 3D integration
- Optimal TSV allocation and congestion management through 3D floor-planning, placement and routing
- Power grid design to avoid IR drop and electro-migration problems
- Thermal management and thermally aware physical des



VERIFICATION

- Determination of modeling/extraction accuracy needed to analyze TSV and intra dies interactions
- Efficient model integration in the verification flows
- Thermal and stress aware 3D-IC verification and testing
- Analysis with Inter chip process variability



What is needed for wider adaptation

- Killer application(s)
  - New functionalities with high volume,
  - High volume, cost effective solutions

- Effective EcoSystem
  - Cooperation and Standards in fabrication and data exchange
  - Standardization vs. Customization; Standards for wider adaptation
  - Business model should be clear
  - 2.5D assembly by OSAT, 3D by Foundries

- EDA tools must be ready.
  - We have to begin investing in the design and verification tools.
  - It is chicken and egg problem, but can not wait for the wide adaptation and high volume to start investing in the tools.
  - 2.5D system design and verification can be done by extending proven 2D tools
  - Start-ups could play important role in 3D-IC and Monolithic 3D-ICs

D.Petranovic: TSV-based 3D-IC: Real or Imaginary