

3D-ICs – Real or Imaginary: And what would speed up adoption?

Herb Reiter, eda2asic Consulting Chair of GSA 3D TSV Programs EDPS, Monterrey, April 2011



- Introduction
- Panelists' Positioning Statements
 - 5 minutes each
- Q & A with the Audience
- Summary





- **2D economical challenges:** NRE's, Risk, Time-to-Market,...
- 2D technical challenges: Variability, leakage, noise,...
- 3D (and 2.5D) offer

 - Lower power
 - Higher bandwidth
 - Shorter latency
 - Smaller form-factor
 - Heterogeneous integration
 - Architectural flexibility
 - In lower cost



- Moderator: Herb Reiter, GSA & eda 2 asic Consulting
- Panelists:
 - Dusan Petranovic, Mentor Graphics
 - Technical Marketing Engineer
 - Bill Martin, E-System Design
 - Vice President
 - Rudy Hernandez, Texas Instruments
 - TSV SoC Readiness Program Manager
 - Rahul Deokar, Cadence Design Systems
 - Product Director